Complaint

IN THE MATTER OF

RAMBUS INCORPORATED

OPINION OF THE COMMISSION AND ORDER IN REGARD TO ALLEGED VIOLATIONS OF SECTION 2 OF THE SHERMAN ACT AND SECTION 5 OF THE FEDERAL TRADE COMMISSION ACT

Docket 9302; File No. 011 0017
Opinion, July 31, 2006 – Order, July 31, 2006
Complaint, June 18, 2002 – Initial Decision, February 23, 2004

This opinion addresses allegations that Rambus Incorporated ("Rambus") violated federal antitrust laws by deliberately deceiving an industry-wide standard-setting organization. The complaint alleged that Rambus participated in the Joint Electron Device Engineering Council ("JEDEC") standard-setting activities for years without disclosing to JEDEC or its members that it was actively working to develop, and possessed, a patent and several pending patent applications involving technologies ultimately adopted in the industry standards for SDRAM and DDR SDRAM. Following an administrative trial, Chief Administrative Law Judge Stephen J. McGuire dismissed the charges, ruling that Complaint Counsel had filed to sustain its burden to establish liability for the violations alleged. On appeal, the Commission overturned the Initial Decision. In a unanimous opinion, the Commission ruled that Rambus withheld material information and that its conduct was calculated to mislead JEDEC members and constituted deception under Section 5 of the FTC Act. The Commission further ruled that Rambus engaged in exclusionary conduct in violation of Section 2 of the Sherman Act, finding that Rambus's conduct significantly contributed to its acquisition of monopoly power. The Commission also issued an order requesting additional briefing to determine an appropriate remedy for Rambus's violations.

Participants

For the *Commission: Malcolm L. Catt, Robert P. Davis, Alice W. Derwiler, Michael A. Franchak, Theodore A. Gebhard, Andrew J. Heimert, Charlotte Manning, Suzanne T. Michel, Geoffrey D. Oliver, Lisa D. Rosenthal, M. Sean Royall, Sarah E. Schroeder, Jerome A. Swindell, John C. Weber, Michael A. Zito* and *Cary E. Zuk.*

For the *Respondent: Sean C. Cunningham, John M. Guaragna, Gary, Cary, Ware & Freidenrich LLP; Peter A. Detre, Sean P. Gates, Steven M. Perry,* and *Gregory P. Stone, Munger Tolles & Olson LLP*; and *Kenneth A. Bamberger, Robert B. Bell* and *A. Douglas Melamed, Wilmer Cutler & Pickering.*

COMPLAINT

Pursuant to the provisions of the Federal Trade Commission Act, and by virtue of the authority vested in it by said Act, the Federal Trade Commission ("Commission"), having reason to believe that Rambus Incorporated (hereinafter, "Rambus" or "Respondent") has violated Section 5 of the Federal Trade Commission ("FTC") Act, as amended, 15 U.S.C. § 45, and it appearing to the Commission that a proceeding in respect thereof would be in the public interest, hereby issues its complaint, stating its charges as follows:

Nature of the Case

1. Through this action, the Commission challenges a pattern of anticompetitive acts and practices, undertaken by Rambus over the course of the past decade, and continuing even today, whereby Rambus, through deliberate and intentional means, has illegally monopolized, attempted to monopolize, or otherwise engaged in unfair methods of competition in certain markets relating to technological features necessary for the design and manufacture of a common form of digital computer memory, known as dynamic random access memory, or "DRAM."

2. Rambus's anticompetitive scheme involved participating in the work of an industry standard-setting organization, known as JEDEC, without making it known to JEDEC or to its members that Rambus was actively working to develop, and did in fact possess, a patent and several pending patent applications that involved specific technologies proposed for and ultimately adopted in the relevant standards. By concealing this information

– in violation of JEDEC's own operating rules and procedures – and through other bad-faith, deceptive conduct, Rambus purposefully sought to and did convey to JEDEC the materially false and misleading impression that it possessed no relevant intellectual property rights. Rambus's anticompetitive scheme further entailed perfecting its patent rights over these same technologies and then, once the standards had become widely adopted within the DRAM industry, enforcing such patents worldwide against companies manufacturing memory products in compliance with the standards.

3. The pattern of anticompetitive conduct by Rambus that is at issue in this action has materially caused or threatened to cause substantial harm to competition, and will in the future materially cause or threaten to cause further substantial injury to competition and to consumers, absent the issuance of appropriate relief in the manner set forth below.

The Respondent

4. Rambus is a public corporation organized, existing, and doing business under and by virtue of the laws of the State of Delaware, with its office and principal place of business located at 9440 El Camino Real, Los Altos, California 94022.

5. Rambus designs, develops, licenses, and markets high-speed chip-connection technology to enhance the performance of computers, consumer electronics, and communications systems. The company licenses semiconductor companies to manufacture and sell memory and logic integrated circuits incorporating Rambus chip-connection technology and markets its solutions to systems companies to encourage them to design this technology into their products. For the fiscal year that ended on September 30, 2001, Rambus reported revenues of approximately $117 million.

6. Rambus is, and at all relevant times has been, a corporation as "corporation" is defined by Section 4 of the Federal Trade Commission Act, 15 U.S.C. § 44; and at all times relevant herein, Rambus has been, and is now, engaged in commerce as "commerce" is defined in the same provision.

Background on the DRAM Industry

7. Within the array of components that together comprise a typical computer, the computer's "memory" functions to store digitally recorded information such that it is available to be accessed when needed by the central processing unit ("CPU"). Computer memory is produced in the form of semiconductor "chips," which are connected with other computer components – such as the CPU and the chipset – via a collection of circuit lines, or a "bus," that routes electronic signals and, in this way, communicates commands and transports data.

8. DRAM is the most common form of computer memory in use today. Another form of memory is known as static random access memory, or "SRAM." DRAM and SRAM differ principally in the following ways: SRAM, unlike DRAM, is able to continuously hold information while power is being supplied to memory. With DRAM, on the other hand, the electronic charges that serve to hold the stored information in place dissipate over time, causing information to "leak" out of memory. To counteract this phenomenon, DRAM memory chips must be constantly "refreshed" with new electronic pulses. DRAM and SRAM also differ in that the latter generally is both faster and more expensive.

9. DRAM is an essential input into a variety of downstream products, including a wide variety of computers, such as personal computers, work stations, and servers, as well as various other types of electronic devices, such as fax machines, printers, digital video recorders, video game equipment, and personal digital assistants. Total sales of DRAM in the United States exceeded

$12 billion in 2000, and for the same year worldwide DRAM sales exceeded $28 billion.

10. Over the years, a series of different architectures for designing DRAM chips has been introduced. As in most other aspects of the computer industry, over time older-generation designs have given way to newer-generation designs or to improvements on existing architectures. A driving force behind this continual process of evolution in DRAM design is the quest for improved computer performance. In particular, as the performance of other computer components and subsystems is enhanced, the marketplace demands equivalent improvements in the speed and other performance characteristics of computer memory.

11. During the late 1980s and early 1990s, developments and improvements in the performance of CPUs and other computer components were moving forward at a rapid clip. It was perceived, however, that developments in DRAM technology had not kept pace, and that performance constraints inherent in the available DRAM architectures were hindering technological progress in the computer industry, creating a virtual "memory bottleneck."

12. It was in this environment that "synchronous" DRAM was developed. The essential innovation underlying synchronous DRAM – as compared to the prior generation of DRAM, also known as "asynchronous" DRAM – was to link memory functions to a "system clock," allowing for more rapid sequencing of communications between the CPU and memory, thereby improving overall system performance. The system clock, in effect, consists of a continuous series of evenly spaced electronic pulses. The period of time (measured in nanoseconds) elapsing between the initiation of two succeeding pulses is referred to as a single "clock cycle."

13. The introduction of synchronous DRAM offered a potentially promising solution to the memory bottleneck. Yet the success of synchronous DRAM depended importantly upon the ability of the computer industry to adopt standards governing the design and implementation of synchronous DRAM.

JEDEC

14. The JEDEC Solid State Technology Association ("JEDEC") – originally known as the Joint Electron Device Engineering Council, from which the acronym JEDEC derives – is one of several standard-setting bodies affiliated with the Electronic Industries Alliance ("EIA"), a trade association representing all segments of the electronics industry. As explained in JEDEC's Manual of Organization and Procedure (hereinafter, the "JEDEC Manual"), the organization's primary purpose and function is to "promote the development and standardization of terms, definitions, product characterization, test methods, manufacturing support functions and mechanical standards for solid state products."

15. According to the JEDEC Manual, membership in JEDEC is freely available to "[a]ny company, organization, or individual conducting business in the USA that … manufactures electronic equipment or electronics-related products, or provides electronics or electronics-related services." To become a JEDEC member, an eligible company need only submit an application, pay membership fees, and agree to abide by JEDEC's rules. JEDEC members, currently numbering in excess of 200, include many of the world's top designers and manufacturers of semiconductors and related products, as well as many of the largest purchasers of such products.

16. JEDEC's internal structure consists of a Board of Directors (formerly known as the JEDEC "Council") and numerous operational committees, subcommittees, and task groups. Standards typically are proposed, evaluated, and

formalized at the committee or subcommittee level and then presented for approval to the Board of Directors, which has final authority to approve or disapprove all proposed standards.

JEDEC Policies and Procedures

17. At all times relevant herein, JEDEC has steadfastly maintained a commitment to promoting free competition within the semiconductor industry. Thus, JEDEC has insisted that its members abide by all applicable laws, including but not limited to laws prohibiting anticompetitive conduct.

18. The JEDEC Manual provides that all JEDEC meetings "shall comply with the current edition of EIA Legal Guides." These Legal Guides – which are explicitly "incorporated … by reference" into JEDEC's own governing rules, and currently are posted on JEDEC's own website under the heading "Manuals" – provide that standardization programs must be "conducted under strict policies designed to promote and stimulate our free enterprise system and to make sure that laws for maintaining and preserving this system are vigorously followed."

19. The EIA/JEDEC Legal Guides establish a "basic rule" that standardization programs conducted by the organization "shall not be proposed for or indirectly result in … restricting competition, giving a competitive advantage to any manufacturer, [or] excluding competitors from the market."

20. Consistent with its commitment to promoting unfettered competition, at all times relevant herein JEDEC also has maintained a commitment to avoid, where possible, the incorporation of patented technologies into its published standards, or at a minimum to ensure that such technologies, if incorporated, will be available to be licensed on royalty-free or otherwise reasonable and non-discriminatory terms. Toward this end, JEDEC has implemented procedures designed to ensure that members disclose any patents, or pending patent applications,

involving the standard-setting work being undertaken by the organization.

21. At all times relevant herein, meetings of the pertinent JEDEC subcommittee routinely were opened with a statement by the chairperson underscoring the existence of such disclosure obligations. This practice is in conformity with requirements set forth in the JEDEC Manual, the current edition of which provides:

> "The chairperson of any JEDEC committee [expressly defined to include, among other things, subcommittees] must call to the attention of all those present the requirements contained in EIA Legal Guides, and the obligation of all participants to inform the meeting of any knowledge they may have of any patents, or pending patents, that might be involved in the work they are undertaking."

Although the above provision was first added to the JEDEC Manual in October 1993, the existence and scope of these disclosure obligations were commonly known within JEDEC before that time, and indeed throughout the entirety of Rambus's involvement in the organization, from late 1991 through mid-1996.

22. While JEDEC does not altogether prohibit the use of patented items in the standards that it promulgates, the JEDEC Manual does mandate that the use of such items "be considered with great care." Indeed, consistent with procedures and practices followed within JEDEC throughout the relevant time period, the JEDEC Manual, at least since October 1993, has required that no standard be drafted to include "patented items" – or "items and processes for which a patent has been applied" – absent both

(1) a well-supported technical justification for inclusion of the patented item; and

(2) express written assurance from the patent holder that a license to the patented technology will be made available either "without compensation" or under "reasonable terms and conditions that are demonstrably free of any unfair discrimination."

23. The JEDEC Manual, at least since October 1993, has expressly provided that the disclosure and licensing obligations discussed above apply "with equal force" when JEDEC members, subsequent to the adoption of a standard, discover new information about existing patent rights – or otherwise obtain new patent rights – involving that standard. In such situations, the JEDEC member must make the same disclosures and provide the same assurances as would be required if the member knew of such patent rights prior to adoption of the relevant standard.

24. Fairly interpreted, the policies, procedures, and practices existing within JEDEC throughout all times relevant herein imposed upon JEDEC members certain basic duties with regard to the disclosure of relevant patent-related information and the licensing of relevant patent rights:

a. First, to the extent any JEDEC member knew or believed that it possessed patents or pending patent applications that might involve the standard-setting work that JEDEC was undertaking, the member was required to disclose the existence of the relevant patents or patent applications and to identify the aspect of JEDEC's work to which they related.

b. Second, in the event that technologies covered by a member's known patents or patent applications were proposed for inclusion in a JEDEC standard, the member was required to state whether the technology would be made available either "without compensation" or under "reasonable terms and conditions that are demonstrably free of any unfair discrimination." Absent the member's agreement to one of

these two conditions, the JEDEC rules would not allow the technology to be incorporated into a proposed standard.

JEDEC Work Involving SDRAM Standards

25. The JEDEC committee responsible for overseeing the development of standards relating to memory devices is known as the JC-42 Committee on Solid State Memories ("JC-42"), which has several subcommittees, one of which is particularly relevant for purposes of the instant complaint: the JC-42.3 Subcommittee on RAM Devices ("JC-42.3").

26. Beginning in or around 1990, JC-42.3 commenced work on standards relating to the design and architecture of synchronous DRAM, referred to within JC-42.3 as "SDRAM." JEDEC members involved in the SDRAM-related work of JC-42.3 have over time included virtually all leading memory designers, manufacturers, and users, whether based in the U.S. or abroad.

27. During the 1990s, JEDEC issued several SDRAM-related standards, the first of which was published in November 1993 and was identified as Release 4 of the 21-C Standard. Subsequent releases of the 21-C Standard followed after that, only small portions of which related to SDRAM, as opposed to other memory-related technologies. In August 1999, however, JEDEC published a substantially augmented SDRAM standard – Release 9 of the 21-C Standard – which introduced a second generation of SDRAM. This second-generation standard became known as "double data rate," or "DDR," SDRAM.

28. Although the second-generation SDRAM standard was not issued until 1999, the work that culminated in that standard commenced, at the very latest, shortly after the first-generation SDRAM standard was adopted in 1993. Indeed, it may have commenced even earlier than that, inasmuch as at least one of the technological features initially considered (but ultimately rejected) for the first-generation SDRAM standard was later

adopted in the second-generation standard. In addition, most, if not all, of the technologies encompassed in the first SDRAM standard were carried forward in the second-generation standard as well.

29. The process through which JEDEC adopted and published these standards proceeded essentially as follows:

a. At regularly scheduled meetings of the JC-42.3 Subcommittee, which typically occurred on a quarterly basis – as well as affiliated committee and task group meetings, which were scheduled as needed – members were allowed to make presentations concerning specific concepts or technologies they proposed for inclusion in a standard under development.

b. Such presentations generally were accompanied by written materials, which, in addition to being shared with all members present at the meeting, were reproduced and attached to the official meeting minutes.

c. Before any proposal could be considered for adoption, it was necessary that it be presented a second time at a later subcommittee meeting.

d. At that point, a member could move that the proposal be presented to the subcommittee membership for approval through a formal balloting process, pursuant to which written ballots were distributed and received by mail.

e. Votes were then tabulated at the subsequent meeting of the subcommittee, at which time members voting "No" were required to explain their reasons for opposing the proposal.

f. Technically, a two-thirds majority was required, but in practice proposals rarely passed without a consensus of all voting members.

g. Individual proposals, once approved by JC-42.3, were often held at the subcommittee level until a complete package of related proposals was ready to be forwarded to the Council for final ratification.

30. JEDEC's – specifically, the JC-42.3 Subcommittee's – work on SDRAM standards continues today, and a third-generation SDRAM standard, known as "DDR II," is expected to be completed later this year.

Rambus and Its Proprietary RDRAM Technology

31. Rambus was founded in 1990 by two electrical engineers, Mark Horowitz and Michael Farmwald, who together developed their own, proprietary synchronous DRAM architecture. They named the new architecture Rambus DRAM, or simply "RDRAM," and contributed the technology to the new corporation upon its formation.

32. RDRAM, as originally designed, differed from traditional DRAM architectures in several ways, including but not limited to the following:

a. First, the RDRAM architecture specified the use of many fewer bus lines than was common in traditional DRAM designs. Thus, RDRAM was said to be a "narrow-bus" architecture. By comparison to RDRAM, traditional DRAM incorporated what was referred to as a "wide-bus" or "broad-bus" design.

b. Second, in the RDRAM architecture, each bus line was capable of carrying three types of information essential to memory functionality: (1) data; (2) "address" information, specifying the location where needed data could be found, or should be placed, in memory; and (3) "control" information, specifying, among other things, the relevant command (*e.g.*,

whether the computer should "read" data from memory or "write" new data to memory). By comparison, in traditional DRAM architectures, each bus line was generally dedicated to carrying only one of these three types of information. Thus, the RDRAM bus was sometimes said to be "multiplexed" or "triply multiplexed."

c. Third, rather than transmitting data, address, and control information separately, as was common in a traditional DRAM architecture, RDRAM transmitted such information together in groupings, called "packets." For this reason, RDRAM is also sometimes referred to as a "packetized" system.

33. Though Rambus has designed, and obtained patents on, various DRAM-related technological concepts or features, Rambus does not itself manufacture such technologies, choosing instead to license its designs for a fee to downstream memory manufacturers. Beginning in the early 1990s and continuing through the present, Rambus has sought to market and license its proprietary RDRAM technology to manufacturers of computer memory and related products, including a number of companies holding membership in JEDEC.

Rambus's '898 Patent Application and Its Progeny

34. On April 18, 1990, Rambus filed its first DRAM-related patent application with the United States Patent and Trademark Office ("PTO") – Application No. 07/510,898 (hereinafter, "the '898 application"). The application contained a 62-page specification and 15 drawings, all purporting to describe Rambus's DRAM-related inventions. In addition, the '898 application contained 150 separate claims, each of which was limited to a narrow-bus, multiplexed, packetized DRAM design.

35. Patents and patent applications consist of two principal parts. The first part is a written description, whereby the patent

applicant (or, if the application issues as a patent, the patent holder) describes the invention, through technical specifications and drawings, in a manner that would allow a person skilled in the art to which the invention applies to understand and practice the invention without undue experimentation. The second part of the patent or patent application consists of one or more "claims" defining, or delineating, the scope – or outer bounds – of the patent holder's exclusive rights (or, in the case of an application, the exclusive rights the applicant seeks to obtain).

36. Because all 150 claims contained in Rambus's '898 patent application were limited to a narrow-bus, multiplexed, packetized DRAM design, through this application Rambus was not seeking – nor, absent amendment to the application, could it obtain – any patent rights exceeding those limitations.

37. In March 1992, Rambus broke out portions of its '898 application into 10 divisional patent applications, each of which "claimed priority back" to the '898 application and to its April 1990 filing date. The original '898 application and these 10 divisional applications, in turn, gave rise to numerous other amended, divisional, or continuation patent applications – all technically the "progeny" of the '898 application – and eventually resulted in the issuance of numerous Rambus patents.

a. The process of obtaining patents or "perfecting" patent claims, otherwise known as patent prosecution, often involves amending, dividing, or continuing patent applications on file with the PTO.

b. Through an "amendment" to a pending patent application, a patent applicant may delete or alter certain claims contained in the pending application, or may add new claims, while at the same time retaining the same specification, drawings, and (to the extent not amended or deleted) claims of the previously pending application.

c. A "divisional" application is one that carves out one of multiple distinct inventions from a prior application and seeks to obtain patent rights over that distinct invention, without adding any new matter to the written description of the invention described in the earlier application.

d. A "continuation" application is a second application, covering the same invention described in a prior application, that is filed before the earlier application either issues as a patent or is abandoned and, again, adds no new matter to the written description of the invention described in the earlier application.

e. Before issuing any patent, the PTO first seeks to determine whether the invention claimed in the relevant patent application is preceded by "prior art" – that is, by preexisting inventions or other publicly known facts or information that demonstrates the lack of novelty in the invention for which a patent is sought.

f. Generally speaking, determinations of whether prior art exists in a given case are made by reference to the date on which the patent application is filed, otherwise known as the "priority date."

g. When a patent application is amended, divided, or continued in the manner described above, the patent applicant may "claim priority back" to an earlier-filed application – thus benefitting from the earlier filing date – but only if the amended, divisional, or continuation application "adds no new matter" to the written description of the invention described in the earlier application. As noted above, divisional and continuation applications, by definition, include no new matter not contained within the earlier-referenced application.

h. Subsequent amendments, divisionals, or continuations claiming priority back to an earlier-filed patent application are

sometimes said to be within the same "family" as the earlier-filed application, or otherwise are said to be the prior application's "progeny."

i. Thus, the fact that, as stated above, each Rambus patent application in the '898 "family" – or each of the '898 application's "progeny" – claimed priority back to the '898 application, means that all of the patent applications in the '898 family contained the same specification and drawings as were contained in the '898 application itself. In fact, in each amended, divisional, and continuation patent application Rambus filed claiming priority back to the '898 application's April 1990 filing date, Rambus was required to – and did – expressly warrant to the PTO that the application added "no new matter" beyond what was contained in the '898 application's 62-page specification and 15 drawings.

38. Though all of the Rambus patent applications in the '898 family contained the same specification and drawings as the '898 application itself, over time Rambus sought to expand the claims contained within these applications in order to obtain patent rights extending beyond the narrow-bus, multiplexed, packetized design inherent in the RDRAM design. In other words, in the course of prosecuting the '898 family of patent applications, Rambus made a conscious effort to withdraw the narrow-bus limitations contained in the original application's claims, and thereby sought to significantly expand the scope of its potential patent rights, while still clinging to the '898 application's April 1990 priority date.

Rambus's Initial Involvement in JEDEC

39. Even before Rambus was formally incorporated in early 1990, its founders outlined a strategy whereby, in an effort to obtain high royalties for RDRAM, they would seek to establish RDRAM as the actual or *de facto* industry standard.

40. Partly with this goal in mind, Rambus attended its first JEDEC meeting in December 1991, and it officially joined the organization shortly thereafter. Although JEDEC was conducting other potentially relevant work at that time, of particular relevance to Rambus was the work then underway within the JC-42.3 Subcommittee, which was in the process of developing a first generation of standards for SDRAM. From December 1991 through December 1995, Rambus representatives regularly attended JC-42.3 meetings.

41. Though Rambus attended its last JC-42.3 meeting in December 1995, it remained a member of JEDEC, and continued to receive official mailings and other information from JEDEC, until June 1996, when it formally withdrew from the organization.

Rambus's Scheme to Capture the SDRAM Standards

42. Shortly after becoming involved in JEDEC, it became apparent to Rambus that JC-42.3 was committed to developing SDRAM standards based on the traditional wide-bus, non-packetized DRAM architecture, relying to the extent possible on non-proprietary technologies. In other words, it was highly unlikely JC-42.3 would be interested in standardizing RDRAM, an architecture that was both proprietary and distinctly non-traditional.

43. Rambus, of course, would have preferred that its own RDRAM technology be adopted as the industry standard. Failing that, Rambus might have preferred to see any efforts at adopting an industry-wide SDRAM standard fail, inasmuch as industry adoption of such a standard would make it more difficult for Rambus to market its proprietary RDRAM technology. By mid-1992, however, Rambus had seized upon an alternative business plan – one that, if successful, might allow Rambus to achieve the goal of charging high royalties even if the DRAM industry were to adopt as its standard something other than RDRAM. Rambus's

CEO, Geoff Tate, laid out this scheme in a June 18, 1992 draft of the Rambus 1992-1997 Business Plan:

> "For about 2+ years a JEDEC committee has been working on the specifications for a Synchronous DRAM. No standard has yet been approved by JEDEC. Our expectation is a standard will not be reached until end of 1992 at the earliest.
>
> * * *
>
> [W]e believe that Sync DRAMs infringe on some claims in our filed patents; and that there are additional claims we can file for our patents that cover features of Sync DRAMs. Then we will be in position to request patent licensing (fees and royalties) from any manufacturer of Sync DRAMs. Our action plan is to determine the exact claims and file the additional claims by the end of Q3/92. Then to advise Sync DRAM manufacturers in Q4/92."

44. In what appears to be the final draft of the same Rambus Business Plan, dated September 1992, Tate further elaborated on the scheme:

> "Rambus expects the patents will be issued largely as filed and that companies will not be able to develop Rambus-compatible or Rambus-like technology without infringing on multiple fundamental claims of the patents …. Rambus' patents are likely to have significant applications other than for the Rambus Interface."

In the same document, Tate also wrote: "Sync DRAMs infringe claims in Rambus's filed patents and other claims that Rambus will file in updates later in 1992."

45. In actuality, events unfolded somewhat differently than Rambus's CEO envisioned in these statements, in a manner that affected the timing, but not the core substance, of Rambus's scheme. For instance, although Rambus's '898 application was pending at the time these statements were written, not until 1996 was Rambus – through a separate application claiming priority back to the '898 application – able to obtain its first patent broad enough to arguably cover aspects of the wide-bus DRAM architecture incorporated into the JEDEC standards. In addition, Rambus ultimately elected to wait until late 1999, after DRAM manufacturers and their customers had become "locked in" to the JEDEC standards, before seeking to enforce its patents against memory manufacturers producing JEDEC-compliant SDRAM.

46. Aside from such timing issues, the Rambus business plans quoted in Paragraphs 43 and 44 set forth quite accurately the basic scheme upon which the company would embark – that is, a scheme whereby Rambus would actively seek to perfect patent rights covering technologies that were the subject of an ongoing, industry-wide standardization process, in which Rambus itself was a regular participant, without disclosing the existence of such patent rights (or the pertinent patent applications) to other participants, many of whom, by producing products compliant with the standards, would later be charged with infringing Rambus's patents.

Implementation of Rambus's Scheme

47. During the course of its participation in JEDEC, from late 1991 through mid-1996, Rambus observed multiple presentations regarding technologies, proposed for (and later included in) JEDEC's SDRAM standards, that Rambus either (1) knew or believed to be covered by claims contained in its then-pending patent applications, or (2) believed could be covered through amendments to those applications expanding the scope of the

patent claims while adding no new matter to the underlying technical specification.

48. That is, at all times relevant herein, Rambus believed that a number of the specific technologies that were proposed for, and later incorporated in, the relevant JEDEC standards were encompassed by the 62-page technical specification and 15 related drawings common to Rambus's '898 application (filed in 1990) and the numerous amended, divisional, and continuation applications that stemmed from the '898 application. Rambus further believed that, to the extent the pending claims of the '898 application and its later-filed progeny failed to cover these technologies as proposed to be used in JEDEC's SDRAM standards, such claims could be amended to cover these technologies, while still claiming priority back to the '898 application's April 1990 filing date.

49. As Rambus's CEO described in the company's internal planning documents in mid-1992 (*see* Paragraphs 43-44 above), the initial phase of Rambus's "action plan" required that it first "determine the exact claims" in its pending applications that covered technologies being incorporated into the JEDEC standards, and then, as needed, "file … additional claims" to perfect Rambus's patent rights over such technologies. In executing these steps, Rambus placed heavy reliance upon two individuals: Richard Crisp, Rambus's designated representative to the JC-42.3 Subcommittee, and Lester Vincent, an attorney with the law firm of Blakely, Sokoloff, Taylor & Zafman, who served as Rambus's outside patent counsel.

50. Richard Crisp, an electrical engineer, joined Rambus in 1991. He attended his first JC-42.3 meeting in February 1992 and continued to attend such meetings regularly through December 1995. (In addition to Crisp, David Mooring, at that time Rambus's vice president for business development, and Billy Garrett, another Rambus engineer, sometimes attended JC-42.3 meetings.) In May 1992, Crisp became Rambus's designated

representative to JC-42.3. As such, he personally received any information, such as meeting minutes and ballot forms, that JEDEC furnished to Rambus by mail.

51. Throughout the duration of Crisp's participation in the JC-42.3 Subcommittee, it was his customary practice to send comprehensive reports to his superiors and others within Rambus describing in detail the technologies that were being proposed for inclusion in the JEDEC SDRAM standards. Typically, these reports were communicated via e-mails authored and sent while the JC-42.3 meetings were still in progress.

52. Lester Vincent and his law firm, Blakely, Sokoloff, were retained as patent counsel by Rambus in the summer of 1991, at which time Vincent assumed primary responsibility for prosecuting Rambus's '898 application before the PTO. For several years thereafter, Vincent and his colleagues assisted Rambus with its DRAM-related patent strategy, providing frequent advice to Rambus on patent-related issues and assuming primary responsibility for drafting, filing, and prosecuting the various continuation and divisional patent applications that stemmed from the '898 application.

53. In late March 1992, Vincent met with Crisp and Allen Roberts, the Rambus vice president with responsibility for patents, to discuss, among other things, Rambus's participation in JEDEC. At this meeting, Vincent, Crisp, and Roberts discussed whether Rambus, having joined JEDEC and participated in JEDEC meetings, was at risk of forfeiting – on grounds of equitable estoppel – its rights to enforce future patents covering aspects of the JEDEC standards. Vincent advised that there could be an equitable estoppel problem if Rambus were to convey to other JEDEC participants the false or misleading impression that it would not seek to enforce its patents or its future patents. He further advised that, in order to reduce such risks, Rambus might remain silent and abstain from voting on any proposed JEDEC standards. Rambus in fact did abstain from voting on the scores

of JC-42.3 ballot initiatives that arose during the course of its participation in JEDEC. Richard Crisp did vote on one occasion, however, registering a "No" vote on four separate ballot items.

54. Throughout its four and one-half years of participation in the JC-42.3 Subcommittee, Rambus engaged in a continuous pattern of deceptive, bad-faith conduct. Rambus's bad-faith participation in JEDEC, although evidenced in other ways as well, was perhaps best exemplified in the coordinated activities of Crisp and Vincent. During his four-year tenure as Rambus's representative to JC-42.3, Crisp observed multiple presentations relating to technologies Rambus believed were covered – or, through amendment, could be covered – by pending Rambus patent applications. In fact, in a number of instances, Crisp, while participating in JC-42.3 meetings, sent e-mails back to Rambus headquarters expressing a belief that Rambus had pending applications covering certain technologies being discussed in such meetings, or otherwise suggesting that Rambus's pending patent applications be reviewed, and if necessary amended, to ensure they covered such technologies. On several occasions, Crisp – based in part on information learned through attending JC-42.3 meetings – developed specific proposals for amending Rambus's pending patent claims and communicated such proposals directly (or via a Rambus colleague) to Vincent. Likewise, in some cases, Vincent sent copies of draft amendments to Rambus's patent applications to Crisp, among others, soliciting his input before finalizing such amendments. Plainly, in light of Rambus's failures to disclose pertinent patent-related information to JEDEC, the activities described in this paragraph constituted bad faith.

55. As underscored elsewhere in this complaint, Rambus never disclosed to JEDEC the fact that, throughout the duration of its membership in the organization, Rambus had on file with the PTO, and was actively prosecuting, patent applications that, in its view, either covered or could easily be amended to cover elements of the existing and future SDRAM standards.

Technologies Impacted by Rambus's Scheme

56. Among other specific technologies adopted or proposed for inclusion in the SDRAM standards during the period of Rambus's participation in JEDEC, which Rambus believed were covered by its then-pending patent applications or could be covered through amendments to such applications, were the following: (1) programmable CAS latency; (2) programmable burst length; (3) on-chip PLL/DLL; and (4) dual-edge clock.

57. Column address strobe (or "CAS") latency refers to the amount of time it takes for the memory to release data after receiving a signal, known as the column address strobe, in connection with a read request from the CPU. The technology known as programmable CAS latency allows memory chips to be programmed such that this aspect of the memory's operation can be tailored to facilitate compatibility with a variety of different computer environments.

58. Burst length generally refers to the number of times information (or data) is transmitted between the CPU and memory in conjunction with a single request or instruction. The technology known as programmable burst length allows memory chips to be programmed to adjust this aspect of the memory's operation in order to facilitate compatibility with a variety of different computer environments.

59. From December 1991 through May 1992, Crisp and other Rambus representatives observed multiple JC-42.3 presentations pertaining to programmable CAS latency and programmable burst length, both of which were proposed to be incorporated in the first JEDEC SDRAM standard. Soon thereafter, in the summer of 1992, Crisp received, and voted upon, a ballot calling for inclusion of both technologies in the standard. This was the only time that Crisp voted on a JEDEC ballot, and he voted "No," for technical reasons that he was called upon to, and did, explain, but

without saying anything to suggest that Rambus might possess relevant intellectual property.

60. At the time of these events, Crisp and others within Rambus believed that both programmable CAS latency and programmable burst length were encompassed by the inventions set forth in the specification and drawings of the '898 application and related applications that were then pending at the PTO, and that Rambus – by amending the claims in those pending applications – had the ability to perfect patent rights covering such technologies as used in the SDRAM standard. Indeed, beginning in May 1992, Crisp, Roberts, and other Rambus representatives began a series of consultations with Vincent for the purpose of drafting new claims, linked to the '898 application, that would cover use of certain technologies in the wide-bus architecture adopted by the SDRAM standard. Programmable CAS latency and programmable burst length were both among the technologies discussed for inclusion in these new wide-bus claims.

61. In March 1993, a Rambus representative attended the JC-42.3 meeting at which both programmable CAS latency and programmable burst length were approved for inclusion in the first SDRAM standard and were forwarded to the JEDEC Council, along with a collection of other approved technologies, as part of a comprehensive standard proposal. Despite Rambus's belief that these technologies were subject to pending Rambus patent claims, the Rambus representative remained silent throughout the meeting. In May 1993, the Council formally adopted the proposed SDRAM standard, which was published in November of that year. (Both of these technologies were later carried forward in the second-generation SDRAM standard published in August 1999.) Also in May 1993, Vincent's law firm (Blakely, Sokoloff) first filed patent claims on behalf of Rambus intended to cover use of DRAM technologies in a wide-bus architecture. From that time through the present, Rambus has continued its efforts to perfect patent rights covering use of

programmable CAS latency and programmable burst length as incorporated in the SDRAM standards.

62. The design objectives served by inclusion of programmable CAS latency and programmable burst length technologies in the first- and second-generation JEDEC standards likely could have been accomplished through use of alternative DRAM-related technologies available at the time these standards were developed. At a minimum, there would have been uncertainty at that time regarding the potential to identify or develop feasible alternative technologies. In either event, had Rambus disclosed to the JC-42.3 Subcommittee that it possessed pending patent applications purporting to cover – or that could be amended to cover – programmable CAS latency and burst length technologies in a wide-bus synchronous DRAM architecture, such disclosures likely would have impacted the content of the SDRAM standards, the terms on which Rambus would later be able to license any pertinent patent rights, or both.

63. Phase lock loop ("PLL") and delay lock loop ("DLL") are closely related technologies, both of which are used to synchronize the internal clock that governs operations within a memory chip and the system clock that regulates the timing of other system functions. The former, PLL, synchronizes the two clocks by adjusting the internal clock's frequency to match the system clock's frequency, whereas the latter, DLL, achieves synchronization by delaying the internal clock. "On-chip" PLL/DLL refers to the approach of placing these technologies on the memory chip itself, as opposed to the alternative approach of placing these technologies on, for instance, the memory module or the motherboard – the latter being known as "off-chip" PLL/DLL.

64. Beginning in September 1994, Crisp observed presentations and other work in the JC-42.3 Subcommittee involving proposals to include on-chip PLL in the second generation of the SDRAM standard. At that time, Crisp and others within Rambus believed that on-chip PLL was

encompassed by the inventions set forth in the specification and drawings of the '898 application and related applications then pending at the PTO, and they had already discussed with Vincent their desire to perfect patent rights covering use of this technology in SDRAMs. Indeed, in June of 1993 Vincent's law firm filed, on Rambus's behalf, an amendment to a pending patent application – Application No. 07/847,692 – adding claims that, on their face, covered use of on-chip PLL/DLL technology in either a wide-bus or narrow-bus DRAM architecture. From June 1993 through the present, Rambus has continued its efforts to perfect patent rights covering use of on-chip DLL technology as ultimately incorporated in the second-generation SDRAM standard published in August 1999.

65. The design objectives served by inclusion of on-chip DLL technology in the second-generation JEDEC standard likely could have been accomplished through use of alternative DRAM-related technologies available at the time these standards were developed. At a minimum, there would have been uncertainty at that time regarding the potential to identify or develop feasible alternative technologies. In either event, had Rambus disclosed to the JC-42.3 Subcommittee that it possessed pending patent applications purportedly covering – or that could be amended to cover – on-chip PLL/DLL technologies in a wide-bus synchronous DRAM architecture, such disclosures likely would have impacted the content of the SDRAM standards, the terms on which Rambus would later be able to license any pertinent patent rights, or both.

66. Dual-edge clock is a technology that permits information to be transmitted between the CPU and memory twice with every cycle of the system clock, thereby doubling the rate at which information is transmitted compared to the first generation of SDRAM, which incorporated a "single-edge clock" and hence permitted information to be transmitted only once per clock cycle.

67. Between December 1991 and April 1992, Crisp and other Rambus representatives attended JC-42.3 meetings at which they

observed presentations and other work involving dual-edge clock technology and a closely related technology known as "toggle-mode." Ultimately, the JC-42.3 Subcommittee decided not to incorporate these technologies into the first-generation SDRAM standard. At the time this decision was reached, however, certain JC-42.3 members expressed the view that such technologies would be appropriate for reconsideration in connection with the next generation of SDRAM. Dual-edge clock technology was again discussed by the JC-42.3 Subcommittee in May 1995. Soon thereafter, in October 1995, a survey ballot relating in part to dual-edge clock technology was distributed to JC-42.3 members, and the same ballot was later discussed at a JC-42.3 meeting in December 1995. A formal proposal to include dual-edge clock technology in the second-generation SDRAM standard was made at a JC-42.3 Subcommittee meeting in March 1996. Following Rambus's withdrawal from JEDEC in June 1996, dual-edge clock technology was the subject of further presentations, and the technology ultimately was incorporated into the second-generation SDRAM standard.

68. In September 1994, Vincent's law firm, on behalf of Rambus, filed an amendment to Rambus's Patent Application No. 08/222,646, adding dual-edge clock claims that were not limited to a narrow-bus RDRAM design, but rather purported to cover use of dual-edge clock technology in any synchronous DRAM architecture, including a wide-bus architecture of the sort that was the focus of JEDEC's SDRAM standards. This application, as amended to include dual-edge clock claims, issued as U.S. Patent No. 5,513,327 (hereinafter, "the '327 patent") in April 1996, while Rambus was still a member of JEDEC. From September 1994 through the present, Rambus has continued its efforts to perfect patent rights covering use of dual-edge clock technology as used in a wide-bus synchronous DRAM architecture.

69. The design objectives served by inclusion of dual-edge clock technology in the second-generation SDRAM standard likely could have been accomplished through use of alternative

DRAM-related technologies available at the time these standards were developed. At a minimum, there would have been uncertainty at that time regarding the potential to identify or develop feasible alternative technologies. In either event, had Rambus disclosed to the JC-42.3 Subcommittee that it possessed patents or pending patent applications arguably covering (or that, with respect the applications, could be amended to cover) dual-edge clock technology in a wide-bus synchronous DRAM architecture, such disclosures likely would have impacted the content of the SDRAM standards, the terms on which Rambus would later be able to license any pertinent patent rights, or both.

Rambus's Limited and Misleading Disclosures to JEDEC

70. At no time during its involvement in JEDEC did Rambus ever disclose to the organization the fact that it possessed an issued patent – the '327 patent discussed in Paragraph 68 above – that purported to cover use of a specific technology proposed for inclusion in the JEDEC SDRAM standards. Nor did Rambus ever disclose to JEDEC that it had on file with the PTO various pending patent applications that purported to cover, or could be amended to cover, a number of other technologies included or proposed for inclusion in the JEDEC SDRAM standards. More generally, Rambus never said or did anything to alert JEDEC to (1) Rambus's belief that it could claim rights to certain technological features not only when used in the context of its proprietary, narrow-bus, RDRAM designs, but also when used in the traditional wide-bus architecture that was the focus of JEDEC's SDRAM standard-setting activities; or (2) the fact that Rambus, while a member of JEDEC, was actively working to perfect such patent rights.

71. On the contrary, Rambus's very participation in JEDEC, coupled with its failure to make required patent-related disclosures, conveyed a materially false and misleading impression – namely, that JEDEC, by incorporating into its SDRAM standards technologies openly discussed and considered

during Rambus's tenure in the organization, was not at risk of adopting standards that Rambus could later claim to infringe upon its patents.

72. On at least two occasions during Rambus's involvement in JEDEC, Crisp was asked by JEDEC representatives whether Rambus had any patent-related disclosures to make pertaining to technologies discussed within JC-42.3. In neither instance did Rambus elect to make such disclosures. One of these instances, however, prompted Rambus to present a letter to the JC-42.3 Subcommittee, dated September 11, 1995, which stated in part:

> "At this time, Rambus elects to not make a specific comment on our intellectual property position …. Our presence or silence at committee meetings does not constitute an endorsement of any proposal under the committee's consideration nor does it make any statement regarding potential infringement of Rambus intellectual property."

73. Beyond these statements, the September 1995 letter said nothing concerning Rambus's patent position. In particular, it made no reference to the fact that Rambus possessed pending patent applications that purported to cover, or were being amended to cover, both (1) technologies included in already published JEDEC standards, and (2) additional technologies then being considered for inclusion in future JEDEC standards. Moreover, the episode that gave rise to Rambus's September 1995 letter involved discussion of a narrow-bus, multiplexed, packetized SDRAM design – known as "SyncLink" – that bore a strong resemblance to Rambus's own narrow-bus, multiplexed, packetized RDRAM design. As explained elsewhere in this complaint, the wide-bus, non-packetized synchronous DRAM design adopted by JEDEC differed significantly from Rambus's RDRAM design, and hence from the SyncLink design as well. Thus, to the extent Rambus's September 1995 letter could be interpreted to suggest that Rambus might possess relevant

intellectual property rights, JEDEC's members would naturally have understood that any such rights related to the SyncLink design, not to the use of certain technologies in the JEDEC standards.

74. In connection with the same incident that gave rise to this September 1995 letter, Crisp and others within Rambus internally debated the extent to which, and manner in which, Rambus should consider making patent-related disclosures to JEDEC or to individual JEDEC members. In this regard, on May 24, 1995, Crisp sent an e-mail to Rambus's CEO, Geoff Tate, as well as other Rambus executives, suggesting a possible bifurcated approach to disclosure. As to any "really key" technologies, Crisp suggested that Rambus should consider making disclosures. But "[i]f it is not a really key issue," Crisp stated, "then … it makes no sense to alert them to a potential problem they can easily work around."

75. In the same e-mail, Crisp outlined a second possible approach to dealing with the disclosure issue:

> "We may want to walk into the next JEDEC meeting and simply provide a list of patent numbers which we have issued and say 'we are not lawyers, we will pass no judgment of infringement or non-infringement, but here are our issued patent numbers, you decide for yourselves what does and does not infringe.'"

Although Rambus in this particular instance did not adopt this approach to disclosure, Crisp's suggestion foreshadowed quite closely the manner in which Rambus would later announce its withdrawal from JEDEC roughly a year later, in June 1996 (*see* Paragraphs 81-88 below).

76. Prior to withdrawing from the organization in June 1996, Rambus did make one patent-related disclosure to JEDEC. In

September 1993, Rambus informed JEDEC of the issuance of U.S. Patent No. 5,423,703 (hereinafter, "the '703 patent"). Although the '703 patent claimed priority back to Rambus's '898 application and thus contained the same specification and drawings, the claims of the '703 patent related to a specific clocking technology, unique to RDRAM, that differed significantly from any clocking technology considered by JEDEC. For this reason, the patent rights conferred upon Rambus by the '703 patent – as reflected in the patent's claims – did not relate to or involve JEDEC's work on SDRAM standards. Furthermore, Rambus's disclosure of this patent did nothing to alert JEDEC's members to Rambus's belief that the specification and related drawings common to the '703 patent and all other patent applications in the '898 family provided a basis upon which it could claim additional patent rights covering technologies incorporated in the SDRAM standards.

77. Other than the foregoing, Rambus made no patent-related disclosures to JEDEC or to the JC-42.3 Subcommittee prior to withdrawing from JEDEC in June 1996. While Rambus was a member of JEDEC, however, some JEDEC members obtained (or viewed) copies of one or more foreign patent applications filed by Rambus, which contained the same specification and drawings as the '898 application and its progeny. In light of the various information (identified in, *inter alia*, Paragraphs 54-55, 60, 64, 68, 70, 73, and 76 above) that Rambus failed to disclose to JEDEC, simply viewing these foreign patent applications would have done nothing to alert JEDEC's members to the fact that Rambus believed the specification and related drawings common to the foreign applications and the '898 family of U.S. patent applications permitted it to claim additional patent rights covering the SDRAM standards.

78. Finally, before, during, and after its tenure as a JEDEC member, in connection with its ongoing efforts to market and license RDRAM, Rambus made limited, private disclosures about its technology to some of the companies participating in JC-42.3.

Upon information and belief, these disclosures were made pursuant to agreements prohibiting the company receiving such information from disclosing it to others. In any event, these limited, private disclosures concerning Rambus's proprietary, narrow-bus RDRAM technology were not adequate to satisfy Rambus's disclosure obligations, nor did such disclosures do, or convey, anything to place individual JEDEC members on notice of Rambus's belief that it could claim patent rights over technologies used in the JEDEC SDRAM standards.

Rambus's Violations of the JEDEC Disclosure Duty

79. As discussed above, upon joining JEDEC, Rambus became subject to the same basic disclosure duty applicable to all JEDEC members – the duty to disclose the existence of any patents or pending patent applications it knew or believed "might be involved in" the standard-setting work that JEDEC was undertaking, and to identify the aspect of JEDEC's work to which they related. (*See* Paragraphs 21 and 24 above.)

80. Rambus violated this duty repeatedly, notwithstanding the limited patent-related disclosures discussed above. The fact is that Rambus, while participating as a JEDEC member, possessed a variety of patent applications – and at least one issued patent – that covered, or were designed to cover, technologies involved in the JEDEC standard-setting work, as well as additional applications that Rambus believed could be amended to cover such technologies without the addition of any new matter. Rambus never disclosed these critical facts to JEDEC.

Rambus's Withdrawal from JEDEC

81. In December 1995, Vincent learned of, and discussed with Anthony Diepenbrock, an in-house Rambus attorney, the Commission's proposed consent order in *In re Dell Computer Corporation*, which involved allegations of anticompetitive unilateral conduct occurring within the context of an industry-

wide standard-setting organization. In January 1996, Vincent advised Rambus that it should terminate "further participation in any standards body," including JEDEC.

82. On June 17, 1996, Rambus formally withdrew from JEDEC via a letter addressed to Ken McGhee, an EIA employee who at the time served as Secretary of JEDEC's JC-42 Committee. The letter was originally drafted by Richard Crisp; however, the final version reflected input from Lester Vincent, among others. Other than McGhee, the letter was sent to no one else within JEDEC, including no members of the JC-42.3 Subcommittee.

83. The letter opened by informing Mr. McGhee that Rambus would not be renewing its membership in the various JEDEC committees and subcommittees in which it had participated, including JC-42.3, and that it therefore was returning its membership invoices unpaid. The remainder of the letter stated as follows:

> "Recently at JEDEC meetings the subject of Rambus patents has been raised. Rambus plans to continue to license its proprietary technology on terms that are consistent with the business plan of Rambus, and those terms may not be consistent with the terms set by standards bodies, including JEDEC. A number of major companies are already licensees of Rambus technology. We trust that you will understand that Rambus reserves all rights regarding its intellectual property. Rambus does, however, encourage companies to contact Dave Mooring of Rambus to discuss licensing terms and to sign up as licensees.

To the extent that anyone is interested in the patents of Rambus, I have enclosed a list of Rambus U.S. and foreign patents. Rambus

has also applied for a number of additional patents in order to protect Rambus technology."

84. Although it attached a list of 23 Rambus patents, Rambus's June 1996 withdrawal letter said nothing to inform JEDEC how, if at all, the 23 listed patents – and the vague reference to additional, unspecified patent applications – might relate to the work of the JC-42.3 Subcommittee. The unstated message, as Crisp had suggested roughly a year earlier, was: "[H]ere are our issued patent numbers, you decide for yourselves what does and does not infringe." (*See* Paragraph 75 above.)

85. The list of 23 Rambus patents attached to this letter consisted of 21 U.S. and two foreign (one Taiwanese and one Israeli) patent numbers, with no accompanying explanation.

a. Of the 21 U.S. patents on the list, five fell within the '898 family and the remaining 16 fell outside the '898 family.

b. Of the latter group of 16, several related to discrete designs for generic electronic circuits – that is, they did not relate uniquely to DRAM design or specifically to Rambus's RDRAM architecture. Several other patents included within this group of 16 did relate in some way to DRAM design but did not bear any direct connection to either Rambus's narrow-bus RDRAM architecture or the wide-bus architecture incorporated into the JEDEC SDRAM standards. The remaining few patents from this group of 16 related to specific implementations of Rambus's narrow-bus architecture. There is no indication that any of these 16 patents related to any specific technology or technological feature adopted or considered for adoption in the SDRAM standards.

c. The five U.S. patents that did fall within the '898 family included the '703 patent discussed in Paragraph 76 above, which Rambus had previously disclosed to JEDEC. Of the remaining four, three of the listed patents – like the '703 patent – contained only claims that either (1) were expressly

limited to the narrow-bus RDRAM architecture, or (2) dealt with a specific aspect of the Rambus RDRAM architecture unrelated to JEDEC's work. The final patent within this group – U.S. Patent No. 5,473,575 – contained claims that, although potentially broader in scope than the other four, were limited to the low-voltage design used in Rambus's RDRAM architecture, which materially differed from the higher-voltage designs that had been the focus of JEDEC's work.

d. The remaining two Rambus patents on the list of 23 were the two foreign patents. Beyond the fact that one of these was written in Chinese, these foreign patents, had they been reviewed by JEDEC's members, would not have sufficed to place them on notice of Rambus's patent rights, or potential patent rights, for reasons discussed above.

86. More important than what the June 1996 withdrawal letter said is what it failed to say. Among other things, the letter made no mention of the fact that Rambus possessed pending patent applications covering, or that could be amended to cover, specific technologies included, or proposed for inclusion, in the JEDEC SDRAM standards. Nor did the letter say anything to alert JEDEC to Rambus's belief that it could claim rights to certain technological features not only when used in the context of its proprietary, narrow-bus, RDRAM designs, but also when used in the traditional wide-bus architecture that was the focus of JEDEC's SDRAM standard-setting activities.

87. But this was not all the June 1996 letter failed to disclose. As of June 1996, when Rambus submitted its formal withdrawal letter to JEDEC, the company actually possessed 24 issued patents, not 23. That is, one – <u>but only one</u> – of Rambus's issued patents was omitted from the list attached to the June 1996 withdrawal letter. The omitted patent was Rambus's '327 patent, which issued in April 1996, two months before Rambus's withdrawal from JEDEC. As discussed in Paragraph 68 above, the '327 patent contained claims purporting to cover use of dual-

edge clock technology in any synchronous DRAM architecture. As such, it was the only patent actually obtained by Rambus while a member of JEDEC that arguably covered use of a specific technology included, or considered for inclusion, in JEDEC's wide-bus SDRAM standards.

88. Even after withdrawing from JEDEC, Crisp and others within Rambus continued to closely monitor JEDEC's ongoing work on SDRAM standards, including work involving specific technologies on which Rambus sought to perfect patent rights.

Industry Adoption of the JEDEC Standards

89. In the years following the issuance of JEDEC's first SDRAM standard in November 1993, DRAM manufacturers and their customers began designing, testing, and ultimately manufacturing memory and memory-related products incorporating, or complying with, JEDEC's standardized SDRAM designs. By 1995, JEDEC-compliant SDRAM had begun to replace older-generation, asynchronous DRAM architectures. Thereafter, the shift to the more modern SDRAM technology progressed rapidly. By 1998, total worldwide sales of JEDEC-compliant SDRAM, on a revenue basis, exceeded sales of asynchronous memory. And by 1999, JEDEC-compliant SDRAM had largely replaced asynchronous DRAM in virtually all relevant uses. Toward the end of this period – roughly 1999 to 2000 – some DRAM manufacturers and their customers also began using RDRAM, but only in very limited end uses, accounting for a relatively small portion (*i.e.*, in the range of 5%) of overall DRAM production.

90. Leading up to and following the issuance of JEDEC's second-generation SDRAM standard – or DDR SDRAM – in August 1999, DRAM manufacturers and their customers began designing, testing, and (to a limited extent) producing memory and memory-related products incorporating, or complying with, the DDR SDRAM standard. By 2000, DDR SDRAM was

beginning to be manufactured in increasing volumes. This trend continued during 2001, and a number of DRAM manufacturers and their customers began to replace first-generation SDRAM and RDRAM with DDR SDRAM for certain high-end uses. Current projections indicate that total sales of DDR SDRAM, on a revenue basis, may account for as large as 40% of all DRAM produced worldwide in 2002, and by 2004 this figure is expected to exceed 50%.

Success of Rambus's Scheme

91. Throughout the late 1990s, as the DRAM industry became increasingly locked in to use of JEDEC-compliant SDRAM, and subsequently DDR SDRAM, Rambus continued the process of perfecting patent rights on certain technologies incorporated within the JEDEC SDRAM standards. By the late 1990s, Rambus had succeeded in obtaining numerous patents, not expressly limited to a narrow-bus RDRAM architecture, that purported to cover, among other technologies encompassed by the JEDEC standards, programmable CAS latency, programmable burst length, on-chip DLL, and dual-edge clock.

92. In late 1999, Rambus began contacting all major DRAM and chipset manufacturers worldwide asserting that, by virtue of their manufacture, sale, or use of JEDEC-compliant SDRAM, they were infringing upon Rambus's patent rights, and inviting them to contact Rambus for the purpose of promptly resolving the issue.

93. Thereafter, Rambus entered into license agreements with seven major DRAM manufacturers: Matsushita Electric Industrial Co., Ltd.; Elpida Memory, Inc.; Samsung Electronics Co.; NEC Corporation; Toshiba America Inc.; Oki Electric Industry Co.; and Mitsubishi Electronics America Inc. Pursuant to these licenses, Rambus allowed each company to use those aspects of its technology necessary for the design and manufacture of JEDEC-compliant SDRAM. In exchange, each

company agreed to pay Rambus ongoing royalties reflecting 0.75% of revenues associated with the manufacture and sale of SDRAMs and 3.5% of revenues associated with the manufacture and sale of DDR SDRAMs. By comparison, Rambus typically licenses all the information needed to develop Rambus-compatible RDRAM memory at royalty rates ranging up to a maximum of approximately 2.5% of revenues.

94. After disclosing its patents, Rambus stated publicly that it would demand even higher royalties from any DRAM manufacturer that refused to license the Rambus patents and instead chose to litigate. Rambus also publicly threatened that it might simply refuse to license its patents to any DRAM manufacturer that was unsuccessful in litigation.

95. In January 2000, Rambus filed the first in a series of patent infringement suits. That suit, which was filed in federal district court in Delaware and named only one defendant – Hitachi – was subsequently settled, conditioned upon Hitachi's agreement to submit to Rambus's license terms.

96. With the signing of the Hitachi license, combined with the seven additional licenses discussed above, Rambus had succeeded in obtaining licenses covering roughly 50% of total worldwide production of synchronous DRAM technology. At current market prices for SDRAM, such licenses entitle Rambus to royalties in the range of $50-100 million per year, a number that could increase significantly in the event Rambus were to prevail in the ongoing litigation and secure licenses from the remaining manufacturers of SDRAMs. Indeed, under such circumstances, Rambus's SDRAM-related patent rights could allow Rambus to extract royalty payments well in excess of a billion dollars from the DRAM industry over the life of the patents.

97. In August 2000, Rambus filed suit against another DRAM manufacturer – Infineon – in federal district court in Virginia, accusing Infineon of patent infringement. Infineon later asserted

various affirmative defenses and counterclaims. In April 2001, the case proceeded to trial, resulting in a jury finding of fraud against Rambus relating to its involvement in the standard-setting activities of JC-42.3 and a legal ruling that Rambus's patents were not infringed by Infineon's use of the SDRAM standards. These and other legal issues are currently pending on appeal before the U.S. Court of Appeals for the Federal Circuit, which heard oral argument June 3, 2002. (Infineon's antitrust claim against Rambus was dismissed due to a technical failure of proof concerning the relevant geographic market. This ruling has not been appealed.)

98. Also in August 2000, Rambus itself was sued, in federal district court in California, by another DRAM manufacturer – Hynix – seeking a declaratory judgment that its manufacture and sale of JEDEC-compliant SDRAM did not infringe Rambus's patents. In addition to seeking declaratory relief, Hynix accuses Rambus of, among other things, antitrust violations, unfair competition, and breach of contract. Meanwhile, Rambus counterclaimed, alleging patent infringement, and the suit was subsequently stayed pending a ruling by the Federal Circuit in the *Infineon* litigation.

99. In a second suit filed against Rambus in August 2000, in federal district court in Delaware, another major DRAM manufacturer – Micron – seeks a declaratory judgment that its manufacture and sale of JEDEC-compliant SDRAM does not infringe Rambus's patents. In addition to seeking declaratory relief, Micron accuses Rambus of monopolization, attempted monopolization, fraud, and inequitable conduct. As in the *Hynix* suit, Rambus has asserted counterclaims against Micron, accusing it of patent infringement, and the suit has been stayed, at least for purposes other than discovery, pending resolution of the *Infineon* appeal.

100. In the *Infineon*, *Hynix*, and *Micron* lawsuits combined, Rambus has asserted that a dozen or more of its patents have been

infringed through the production and sale of JEDEC-compliant SDRAM by these three companies. Each of the patents upon which Rambus has sued stems from, and claims priority back to, Rambus's '898 application.

101. Upon information and belief, Rambus also possesses additional patents and patent applications, some claiming priority back to the '898 application, that it has not yet sought, but could in the future seek, to enforce against memory manufacturers producing JEDEC-compliant SDRAM, absent issuance of the relief requested below.

102. In addition to the foregoing, Rambus is involved in other litigation in various foreign countries relating to foreign patents that cover, or purport to cover, many of the same DRAM-related technologies that are at issue in the U.S. litigation.

103. Notably, while Rambus has licenses covering roughly 50% of the synchronous DRAM industry, Rambus asserts in litigation that all or virtually all synchronous DRAM produced worldwide incorporates Rambus technology and that those synchronous DRAM manufacturers that are not paying royalties to Rambus are liable in damages. In addition to facing the threat of potential damages, those companies that have chosen to litigate against Rambus have been forced to incur substantial litigation costs, reaching into the millions, if not tens of millions, of dollars. Unless they prevail against Rambus in litigation, such companies also face the prospect of being denied licenses to Rambus's patents, or otherwise being required to pay royalties significantly in excess of the amounts paid by the memory manufacturers that acquiesced to Rambus's licensing demands without resort to litigation.

104. Rambus also has licensed companies, such as Intel, that do not produce memory chips but do produce related computer components – in Intel's case, chipsets – that are designed to be compatible with synchronous DRAMs.

Inability of DRAM Industry to Work Around Rambus's Patents

105. Given the extensive degree to which the DRAM industry has become locked in to the JEDEC SDRAM standards, it is not economically feasible for the industry to attempt to alter or work around the JEDEC standards in order to avoid payment of royalties to Rambus. Any such effort would face innumerable practical and economic impediments, including but not limited to the out-of-pocket costs associated with redesigning, validating, and qualifying SDRAM products to conform with a revised set of standards. On top of this, such manufacturers could be forced to absorb potentially massive revenue losses if, as a result of modifying the JEDEC standards, their introduction of new products were delayed.

106. Agreeing upon revised SDRAM standards could in itself be a very costly and time-consuming process. Indeed, it is unclear whether the industry would be able to reach any such consensus, given complications inherent in the current market environment, including the fact that some DRAM manufacturers have acquiesced to Rambus's licensing demands while others have not.

107. Added to these complications is the fact that purchasers and other users of JEDEC-compliant SDRAM technology – including manufacturers of computers, chipsets, graphics cards, and motherboards – have themselves become locked in to the JEDEC standards. For this and other reasons, even if the DRAM industry were otherwise able to undertake the complicated and costly task of revising the JEDEC standards to work around Rambus's patent claims, it is unclear whether downstream purchasers of synchronous DRAM would welcome or accept such an action, given the costs that they would be forced to incur in order to conform their own product designs and manufacturing processes to a revised set of standards. Nor is it

clear whether downstream purchasers and other users of SDRAM technology would tolerate the delay in the introduction of new products that likely would result from the process of changing the standard.

108. Any effort to revise the JEDEC standards on a going-forward basis could also interfere with the ability of DRAM designers, manufacturers, and users to maintain the backwards compatibility among successive generations of synchronous DRAM that JEDEC has sought to preserve.

109. For these and other reasons, the DRAM industry has had little or no practical ability to work around Rambus's patent claims, and it is not at all clear the industry could do so in the future.

Relevant Product Markets

110. Synchronous DRAM is produced throughout the world by various memory manufacturers located or doing business in the U.S. and various foreign countries. Synchronous DRAMs, and products incorporating synchronous DRAMs, are imported and exported throughout the world in large volumes.

111. Commercial DRAM chip manufacturers wishing to design and produce synchronous DRAM chips, wherever they may be located throughout the world, are practically limited to using one of two alternative architectures: the JEDEC-compliant SDRAM architecture or Rambus's own proprietary RDRAM architecture, itself a synchronous DRAM technology. No other synchronous DRAM architectures have been developed and made available for wide-spread commercial use.

112. The RDRAM and JEDEC-compliant SDRAM architectures, in turn, each consist of a variety of subsidiary technologies – or technological features – that are necessary in order successfully to design and manufacture a synchronous

DRAM chip. These subsidiary technologies may be regarded as essential technology inputs into the design and manufacture of synchronous DRAMs.

113. As in other aspects of engineering, electrical engineers involved in the design of synchronous DRAM chips select from among alternative technological features, concepts, or approaches in order to address or solve issues, or problems, that arise in the course of developing such chips. The alternative technologies available to address a given technical issue arising in the course of synchronous DRAM design together may comprise a separate, well-defined product market. At least four such markets are relevant for purposes of the instant complaint, including the following:

a. The market for technologies used to specify the length of time – or "latency" period – between the memory's receipt of a read request and its release of data corresponding with the request (hereinafter, the "latency technology market"). This market includes programmable CAS latency and any alternative technologies that may be economically viable substitutes for the use of programmable CAS latency in synchronous DRAM design.

b. The market for technologies used to specify the number of times information (data) is transmitted between the CPU and memory – *i.e.*, the "burst length" – associated with a single request or instruction (hereinafter, the "burst length technology market"). This market includes programmable burst length and any alternative technologies that may be economically viable substitutes for the use of programmable burst length in synchronous DRAM design.

c. The market for technologies used to synchronize the internal clock that governs operations within a memory chip and the system clock that regulates the timing of other system functions (hereinafter, the "clock synchronization technology

market"). This market includes on-chip DLL technology and any alternative technologies that may be economically viable substitutes for the use of an on-chip DLL in synchronous DRAM design.

d. The market for technologies used to accelerate the rate at which data are transmitted between the CPU and memory (hereinafter, the "data acceleration technology market"). This market includes dual-edge clock technology and any alternative technologies that may be economically viable substitutes for the use of a dual-edge clock in synchronous DRAM design.

114. Technologies used in the design of synchronous DRAM chips, to solve separate but related design issues, may be viewed as economic complements. The complementary nature of such design technologies is evidenced by, among other things, the fact that they sometimes are licensed together in a package, as is the case with respect to the patented Rambus technologies encompassed by each of the aforementioned product markets. Where such close relationships exist among a group of technologies, all of which are necessary inputs into the design or manufacture of a common downstream product, one may appropriately define a product market encompassing the group of complementary technologies and their close substitutes. Thus, in addition, or in the alternative, to the four product markets identified above, there is a fifth well-defined product market that is relevant for purposes of this complaint – namely, a market comprising, collectively, all technologies falling within any one of these narrower markets (hereinafter, the "synchronous DRAM technology market").

Geographic Scope of Relevant Product Markets

115. Technologies encompassed within each of the foregoing product markets are used on a worldwide basis. Technologies originating outside the United States frequently are

considered for and used in JEDEC standards, and indeed have been used in both the first- and second-generation SDRAM standards promulgated by JEDEC. The technologies selected for inclusion in these JEDEC standards, in turn, have been incorporated and used by synchronous DRAM manufacturers throughout the world.

116. Both proprietary and non-proprietary technologies have been used in synchronous DRAM design. To the extent such technologies are non-proprietary, they are free to be used, on a non-royalty-incurring basis, by any synchronous DRAM manufacturer or downstream user worldwide. On the other hand, to the extent such technologies are proprietary, inasmuch as they are subject to patents or potential patent claims in one or more jurisdictions, the use of such technologies by synchronous DRAM manufacturers or downstream users may depend upon the user's agreement to specific license terms negotiated with the patent holder. In the event that patent rights are similar in most relevant jurisdictions, however, there is no apparent legal or economic impediment that would preclude licenses from being made available on a multi-national or worldwide basis. Indeed, Rambus, which holds synchronous DRAM-related patents issued in the United States and numerous foreign countries, commonly grants licenses to companies in the U.S. and abroad encompassing rights to use Rambus's patented technologies worldwide.

117. For these and other reasons, each of the technology-related product markets identified above is worldwide in scope.

118. Alternatively, or in addition, the geographic scope of such product markets might appropriately be defined as the United States if, for example, Rambus's U.S. patent rights differed significantly from rights recognized in various foreign jurisdictions, or if Rambus otherwise had the ability to vary royalty rates from one jurisdiction to another.

Anticompetitive Effects of Rambus's Conduct

119. The foregoing conduct by Rambus, during and after its involvement in JEDEC's JC-42.3 Subcommittee, has materially caused or threatened to cause substantial harm to competition and will, in the future, materially cause or threaten to cause further substantial injury to competition and consumers, absent the issuance of appropriate relief in the manner set forth below.

120. The threatened or actual anticompetitive effects of Rambus's conduct include but are not limited to the following:

a. increased royalties (or other payments) associated with the manufacture, sale, or use of synchronous DRAM technology;

b. increases in the price, and/or reductions in the use or output, of synchronous DRAM chips, as well as products incorporating or using synchronous DRAMs or related technology;

c. decreased incentives, on the part of memory manufacturers, to produce memory using synchronous DRAM technology;

d. decreased incentives, on the part of DRAM manufacturers and others, to participate in JEDEC or other industry standard-setting organizations or activities; and

e. both within and outside the DRAM industry, decreased reliance, or willingness to rely, on standards established by industry standard-setting collaborations.

Rambus's Knowing Destruction of Documents

121. Rambus has engaged in a systematic effort – blessed if not orchestrated by its most senior executives – to destroy

documents and other information. Upon information and belief, among other pertinent files destroyed as a result of this campaign were notes and other documentation relating to, among other things, Rambus's involvement in the JC-42.3 Subcommittee. Upon information and belief, this document-destruction campaign was undertaken, wholly or in substantial part, with the purpose of avoiding or minimizing the adverse legal repercussions of the anticompetitive conduct described in the instant complaint. Partly as a consequence of these document-destruction activities, in combination with other bad-faith litigation conduct, Rambus was required by the federal district court presiding over the *Infineon* litigation to pay a sanction exceeding $7 million.

First Violation Alleged

122. As described in Paragraphs 1-121 above, which are incorporated herein by reference, Rambus has willfully engaged in a pattern of anticompetitive and exclusionary acts and practices, undertaken over the course of the past decade, and continuing even today, whereby it has obtained monopoly power in the synchronous DRAM technology market and narrower markets encompassed therein – namely, the latency, burst length, clock synchronization, and data acceleration markets discussed above – which acts and practices constitute unfair methods of competition in violation of Section 5 of the FTC Act.

Second Violation Alleged

123. As described in Paragraphs 1-121 above, which are incorporated herein by reference, Rambus has willfully engaged in a pattern of anticompetitive and exclusionary acts and practices, undertaken over the course of the past decade, and continuing even today, with a specific intent to monopolize the synchronous DRAM technology market and narrower markets encompassed therein, resulting, at a minimum, in a dangerous probability of monopolization in each of the aforementioned

markets, which acts and practices constitute unfair methods of competition in violation of Section 5 of the FTC Act.

Third Violation Alleged

124. As described in Paragraphs 1-121 above, which are incorporated herein by reference, Rambus has willfully engaged in a pattern of anticompetitive and exclusionary acts and practices, undertaken over the course of the past decade, and continuing even today, whereby it has unreasonably restrained trade in the synchronous DRAM technology market and narrower markets encompassed therein, which acts and practices constitute unfair methods of competition in violation of Section 5 of the FTC Act.

Notice

Notice is hereby given to the Respondent that the eighteenth day of September, 2002, at 10:00 a.m., or such later date as determined by an Administrative Law Judge of the Federal Trade Commission, is hereby fixed as the time and Federal Trade Commission offices, 600 Pennsylvania Avenue, N.W., Room 532, Washington, D.C. 20580, as the place when and where a hearing will be had before an Administrative Law Judge of the Federal Trade Commission, on the charges set forth in this complaint, at which time and place you will have the right under the FTC Act to appear and show cause why an order should not be entered requiring you to cease and desist from the violations of law charged in the complaint.

You are notified that the opportunity is afforded to you to file with the Commission an answer to this complaint on or before the twentieth (20^{th}) day after service of it upon you. An answer in which the allegations of the complaint are contested shall contain a concise statement of the facts constituting each ground of defense; and specific admission, denial, or explanation of each fact alleged in the complaint or, if you are without knowledge

thereof, a statement to that effect. Allegations of the complaint not thus answered shall be deemed to have been admitted.

If you elect not to contest the allegations of fact set forth in the complaint, the answer shall consist of a statement that you admit all of the material facts to be true. Such an answer shall constitute a waiver of hearings as to the facts alleged in the complaint and, together with the complaint, will provide a record basis on which the Administrative Law Judge shall file an initial decision containing appropriate findings and conclusions and an appropriate order disposing of the proceeding. In such answer, you may, however, reserve the right to submit proposed findings and conclusions under § 3.46 of the Commission's Rules of Practice for Adjudicative Proceedings and the right to appeal the initial decision to the Commission under § 3.52 of said Rules.

Failure to answer within the time above provided shall be deemed to constitute a waiver of your right to appear and contest the allegations of the complaint and shall authorize the Administrative Law Judge, without further notice to you, to find the facts to be as alleged in the complaint and to enter an initial decision containing such findings, appropriate conclusions, and order.

The ALJ will schedule an initial prehearing scheduling conference to be held not later than 14 days after the last answer is filed by any party named as a respondent in the complaint. Unless otherwise directed by the ALJ, the scheduling conference and further proceedings will take place at the Federal Trade Commission, 600 Pennsylvania Avenue, N.W., Room 532, Washington, D.C. 20580. Rule 3.21(a) requires a meeting of the parties' counsel as early as practicable before the prehearing scheduling conference, and Rule 3.31(b) obligates counsel for each party, within 5 days of receiving a respondent's answer, to make certain initial disclosures without awaiting a formal discovery request.

Notice of Contemplated Relief

Should the Commission conclude from the record developed in any adjudicative proceedings in this matter that Respondent's conduct violated Section 5 of the Federal Trade Commission Act as alleged in the complaint, the Commission may order such relief as is supported by the record and is necessary and appropriate, including but not limited to:

1. Requiring Respondent to cease and desist all efforts it has undertaken by any means, including without limitation the threat, prosecution, or defense of any suits or other actions, whether legal, equitable, or administrative, as well as any arbitration, mediation, or any other form of private dispute resolution, through or in which Respondent has asserted that any person or entity, by manufacturing, selling, or otherwise using JEDEC-compliant SDRAM and DDR SDRAM technology (including future variations of JEDEC-compliant SDRAM and DDR SDRAM technology), infringes any of Respondent's current or future United States patents that claim priority back to U.S. Patent Application Number 07/510,898 filed on April 18, 1990 or any other U.S. Patent Application filed before June 17, 1996.

2. Requiring Respondent not to undertake any new efforts by any means, including without limitation the threat, prosecution, or defense of any suits or other actions, whether legal, equitable, or administrative, as well as any arbitration, mediation, or any other form of private dispute resolution, through or in which Respondent has asserted that any person or entity, by manufacturing, selling, or otherwise using JEDEC-compliant SDRAM and DDR SDRAM technology (including future variations of JEDEC-compliant SDRAM and DDR SDRAM technology), infringes any of Respondent's current or future United States patents that claim priority back to U.S. Patent Application Number 07/510,898 filed on April 18, 1990 or any other U.S. Patent Application filed before June 17, 1996.

3. Requiring Respondent to cease and desist all efforts it has undertaken by any means, including without limitation the threat, prosecution, or defense of any suits or other actions, whether legal, equitable, or administrative, as well as any arbitration, mediation, or any other form of private dispute resolution, through or in which Respondent has asserted that any person or entity, by manufacturing, selling, or otherwise using JEDEC-compliant SDRAM and DDR SDRAM technology (including future variations of JEDEC-compliant SDRAM and DDR SDRAM technology), for import or export to or from the United States, infringes any of Respondent's foreign patents, current or future, that claim priority back to U.S. Patent Application Number 07/510,898 filed on April 18, 1990 or any other Patent Application filed before June 17, 1996.

4. Requiring Respondent not to undertake any new efforts by any means, including without limitation the threat, prosecution, or defense of any suits or other actions, whether legal, equitable, or administrative, as well as any arbitration, mediation, or any other form of private dispute resolution, through or in which Respondent has asserted that any person or entity, by manufacturing, selling, or using JEDEC-compliant SDRAM and DDR SDRAM technology (including future variations of JEDEC-compliant SDRAM and DDR SDRAM technology), for import or export to or from the United States, infringes any of Respondent's foreign patents, current or future, that claim priority back to U.S. Patent Application Number 07/510,898 filed on April 18, 1990 or any other Patent Application filed before June 17, 1996.

5. Requiring Respondent to employ, at Respondent's cost, a Commission-approved compliance officer who will be the sole representative of Respondent for the purpose of communicating Respondent's patent rights related to any

standard under consideration by any standard-setting organization of which Respondent is a member.

6. Such other or additional relief as is necessary to correct or remedy the violations alleged in the complaint.

WHEREFORE, THE PREMISES CONSIDERED, the Federal Trade Commission on this eighteenth day of June, 2002, issues its complaint against said Respondent.

By the Commission.

INITIAL DECISION

By: Stephen J. McGuire, Chief Administrative Law Judge

PART ONE: INTRODUCTION

This Initial Decision is divided into four parts. Part One is the introduction, which includes a summary of the allegations contained in the Complaint; the defenses asserted in Respondent's Answer; the issues presented; the procedural background; a comment on the evidence; and a summary of the decision. Part Two contains the separately numbered findings of fact. Part Three contains the analysis and conclusions of law, which provides an overview of the legal theories asserted by Complaint Counsel; sets forth the applicable law on each of the elements necessary to find a violation; and then applies the law to the facts established at trial. Part Four contains the summary of the conclusions of law and the Order of the Court.

I. FEDERAL TRADE COMMISSION COMPLAINT

The Federal Trade Commission ("FTC") issued its Complaint in this matter on June 18, 2002. The Complaint charges that Respondent, Rambus Inc., a corporation, violated Section 5 of the Federal Trade Commission Act ("FTC Act"), as amended. 15 U.S.C. § 45.

The Complaint charges Respondent with three violations. The first violation charges that Respondent engaged in a pattern of anticompetitive and exclusionary acts and practices, whereby it obtained monopoly power in the synchronous DRAM technology market and narrower markets encompassed therein, in violation of Section 5 of the FTC Act. (Complaint ¶ 122). The second violation charges that Respondent engaged in a pattern of anticompetitive and exclusionary acts and practices with a specific intent to monopolize the synchronous DRAM technology market and narrower markets encompassed therein, resulting, at a

minimum, in a dangerous probability of monopolization in each of the markets, in violation of Section 5 of the FTC Act. (Complaint ¶ 123). The third violation charges that Respondent engaged in a pattern of anticompetitive and exclusionary acts and practices, whereby it unreasonably restrained trade in the synchronous DRAM technology market and narrower markets encompassed therein, which acts and practices constitute unfair methods of competition in violation of Section 5 of the FTC Act. (Complaint ¶ 124).

The Complaint alleges that Respondent participated in the work of the JEDEC Solid State Technology Association ("JEDEC"), an industry standard setting organization in which Respondent was a regular participant, without making it known to JEDEC or to its members that Respondent sought to obtain patents on technologies adopted in the relevant JEDEC standards. (Complaint ¶¶ 2, 43, 44, 45, 46). Respondent's alleged scheme further entailed perfecting its patent rights over these same technologies and then, once the standards had become widely adopted within the DRAM industry, enforcing such patents worldwide against companies manufacturing memory products in compliance with the JEDEC standards. (Complaint ¶¶ 2, 43, 44, 45, 46).

Respondent is alleged to have concealed information in violation of JEDEC's operating rules and procedures which Complaint Counsel argue imposed upon JEDEC members an obligation to "disclose any patents, or pending patent applications, involving the standard-setting work." (Complaint ¶¶ 20, 21, 24, 79). In addition, the Complaint alleges a "basic rule" of JEDEC to avoid anticompetitive activity and a commitment to avoid, where possible, incorporation of patented technologies. (Complaint ¶¶ 17, 18, 19, 20, 22). The Complaint alleges that Respondent violated these duties by conveying to JEDEC the materially false and misleading impression that it possessed no relevant intellectual property rights. (Complaint ¶¶ 2, 80).

The Complaint further alleges that Respondent's conduct caused anticompetitive effects including increased royalties, increase in the price of synchronous DRAM and products incorporating synchronous DRAM, decreased incentives to produce memory using synchronous DRAM technology, and harms to standard setting organizations and activities. (Complaint ¶¶ 119, 120).

II. RESPONDENT'S ANSWER

In its Answer filed on July 29, 2002, Respondent alleged as an affirmative defense that the Complaint failed to state a claim under Section 5 of the FTC Act. The Answer denied the material allegations of the Complaint and asserted that the evidence would show that JEDEC's rules and policies did not impose, and were not commonly understood to impose, the disclosure obligations set out in the Complaint. (Answer, pp. 1-2).

Respondent asserted in its Answer that the evidence would show that it did not have, until after it left JEDEC, any undisclosed patents or patent applications that contained claims reading on devices manufactured in accordance with any JEDEC standard. (Answer, p. 2). Respondent also asserted in its Answer that the evidence would show that JEDEC did not rely on any purported silence on Respondent's part at JEDEC meetings and instead chose to adopt certain technologies because of the cost/performance advantages of those technologies and the absence of reasonable alternatives. (Answer, p. 2).

Respondent's Answer asserted that in light of the absence of a duty to disclose, in light of the absence of pending claims reading on JEDEC standards, and in light of the other evidence to be considered at trial, it would be clear that Respondent's alleged failure to disclose its potential intellectual property claims had no anticompetitive effect in any market and that Respondent had not violated Section 5. (Answer, pp. 1-3).

III. ISSUES PRESENTED

The issues presented in this case are:

(1) whether Respondent engaged in a pattern of deceptive, exclusionary conduct by subverting an open standards process;

(2) whether Respondent utilized such conduct to capture a monopoly in technology-related markets;

(3) whether Respondent's challenged conduct violated principles of antitrust law; and

(4) whether Respondent's conduct resulted in anticompetitive injury.

IV. PROCEDURAL BACKGROUND

On June 18, 2002, the Commission issued its Complaint. This case was initially assigned to Administrative Law Judge ("ALJ") James P. Timony. Rambus filed a motion to stay the proceeding until the Federal Circuit issued its decision in *Rambus Inc. v. Infineon Technologies*, an appeal of a jury verdict against Rambus. The Federal Circuit reversed the jury verdict of fraud and remanded the case, as discussed more fully in Part III, Section I.C. An Order Denying Motion for Stay was issued in this case on July 18, 2002. On July 29, 2002, Rambus filed its Answer in this matter.

On February 26, 2003, ALJ Timony issued an Order On Complaint Counsel's Motions For Default Judgment and For Oral Argument which imposed seven rebuttable presumptions against Rambus based on a finding of intentional destruction of evidence. This Order is discussed in Part III, Section I.B.

On February 28, 2003, ALJ Timony retired from federal service. Stephen J. McGuire was subsequently appointed FTC Chief Administrative Law Judge and assigned the Rambus matter.

Trial in this proceeding commenced on April 30, 2003. The 54 day administrative hearing produced a voluminous evidentiary record including 44 live witnesses, 1,770 admitted exhibits, nearly 12,000 pages of trial transcript, and hundreds of pages of deposition transcripts. The last day on which testimony was received was August 1, 2003. The parties then filed Post-Trial Briefs, Proposed Findings of Fact, and Conclusions of Law, and replies thereto. Closing arguments and oral examination by the Court was conducted on October 8, 2003. Following the closing arguments, the hearing record was closed pursuant to Commission Rule 3.44(c), by Order dated October 9, 2003. Due to the exceptional circumstances of the complexity of the issues presented, the volumes of evidence introduced at trial, and review of the comprehensive proposed findings of fact and post-hearing briefs, it was necessary to extend the deadline for filing the Initial Decision within one year of the issuance of the Complaint. By Order dated December 23, 2003, the Commission also extended the time for filing the Initial Decision within 90 days of the close of the hearing record until February 17, 2004.

V. EVIDENCE

The Initial Decision is based on the transcript of the testimony, the exhibits properly admitted in evidence, and the proposed findings of fact, briefs, conclusions of law, and replies thereto filed by the parties. Once a finding of fact is established, it is cited to in subsequent sections or in the analysis by the designation "F."[1]

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[1] This opinion uses the following abbreviations for citations:

Comp. - Complaint
F. - Finding of fact

The parties submitted extensive post-trial briefs and reply briefs. The Initial Decision addresses only material issues of fact and law. Proposed findings of fact not included in the Initial Decision were rejected, either because they were not supported by the evidence or because they were not dispositive to the determination of the allegations contained in the Complaint. The Commission has held that Administrative Law Judges are not required to discuss the testimony of each witness or all exhibits that are presented during the administrative adjudication. *In re Amrep Corp.*, 102 F.T.C. 1362, 1670 (1983). Further, administrative adjudicators are "not required to make subordinate findings on every collateral contention advanced, but only upon those issues of fact, law, or discretion which are 'material.'" *Minneapolis & St. Louis Ry. Co. v. United States*, 361 U.S. 173, 193-94 (1959).

Many of the documents and parts of the oral testimony were received into the record *in camera*. Where an entire document or where certain trial testimony was given *in camera* treatment for trial, but the portion of the document or the trial testimony utilized in this Initial Decision does not rise to the level necessary for *in camera* treatment, such information is disclosed in the public version of this Initial Decision, pursuant to Commission Rule 3.45(a) (the ALJ "may disclose such *in camera* material to the extent necessary for the proper disposition of the proceeding"). In

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CX - Complaint Counsel Exhibit
RX - Respondent Exhibit
JX - Joint Exhibit
Tr. - Transcript of Testimony before the Administrative Law Judge
Dep. - Transcript of Deposition
Stip. - Stipulation
CCPFF - Complaint Counsel's Proposed Findings of Fact
CCPHB - Complaint Counsel's Post-Hearing Brief
CCPHRB - Complaint Counsel's Post-Hearing Reply Brief
RPHB - Respondent's Post-Hearing Brief
RPHRB - Respondent's Post-Hearing Reply Brief

accordance with 16 C.F.R. § 3.45(f), material that has been given *in camera* treatment is indicated in bold font and braces in the *in camera* version. Where *in camera* material had been redacted from the public version of the Initial Decision, braces precede the redacted material.

VI. SUMMARY OF THE DECISION

Complaint Counsel have failed to sustain their burden of proof with respect all three of the violations alleged in the Complaint. First, the evidence at trial establishes that Complaint Counsel failed to prove the facts they alleged in the Complaint. Second, an analysis of the legal theories advanced by Complaint Counsel demonstrates that there is no legal basis for finding a violation of Section 5 of the Federal Trade Commission Act, either as based on other antitrust laws or solely as an unfair method of competition. Third, an application of the facts established at trial to the legal theories asserted leads to the conclusion that Complaint Counsel have failed to prove their case.

The evidentiary record demonstrates that: (1) the EIA/JEDEC patent policy encouraged the early, voluntary disclosure of essential patents and Respondent did not violate this policy; (2) the case law upon which Complaint Counsel rely to impose antitrust liability is clearly distinguishable on the facts of this case; (3) Respondent's conduct did not amount to deception and did not violate any "extrinsic duties," such as a duty of good faith to disclose relevant patent information; (4) Respondent did not have any undisclosed patents or patent applications during the time that it was a JEDEC member that it was obligated to disclose; (5) amendments to broaden Respondent's patent applications while a member of JEDEC were not improper, either as a matter of law or fact; (6) by having a legitimate business justification for its actions, Respondent did not engage in exclusionary conduct; (7) Respondent did not intentionally mislead JEDEC by knowingly violating a JEDEC disclosure rule; (8) there is no causal link between JEDEC standardization and

Respondent's acquisition of monopoly power; (9) members of JEDEC did not rely on any alleged omission or misrepresentation by Respondent and, if they had, such reliance would not have been reasonable; (10) the challenged conduct did not result in anticompetitive effects, as Complaint Counsel did not demonstrate that there were viable alternatives to Respondent's superior technologies; (11) the challenged conduct did not result in anticompetitive effects as the challenged conduct did not result in higher prices to consumers; and (12) JEDEC is not locked in to using Respondent's technologies in its current standardization efforts.

For these reasons, Complaint Counsel have failed to sustain their burden to establish liability for the violations alleged. Accordingly, the Complaint is **DISMISSED.**

PART TWO: FINDINGS OF FACT

I. DRAM AND THE INVENTIONS OF DRS. FARMWALD AND HOROWITZ

A. DRAM Applications in Computer Systems

1. DRAM Defined

1. DRAM stands for "dynamic random access memory." (Rhoden, Tr. 266). DRAM is a type of electronic memory. (Rhoden, Tr. 266). DRAM is "dynamic" because it needs to be refreshed every fraction of a second. (Rhoden, Tr. 266-67).

2. The primary use for DRAM is in computer systems. (Rhoden, Tr. 267-68; Gross Tr. 2272-73).

3. DRAMs are also used in a wide range of other products involving computer systems. (Sussman, Tr. 1362). These products include printers, PDAs (personal digital assistants), and cameras.

(Kellogg, Tr. 4986-87; Tabrizi, Tr. 9126-27; Krashinsky, Tr. 2770-71; Farmwald, Tr. 8206-07; Gross, Tr. 2272-73).

4. Typically, multiple DRAM chips are placed on a memory module, which is a small printed circuit board. (Rhoden, Tr. 272-73). The module containing the DRAM chips connects to a motherboard. (Rhoden, Tr. 270, 273). In some applications, such as graphics cards, the DRAM chips are not put in memory modules. (Wagner, Tr. 3871-72).

5. A DRAM is made up of a number of cells. (Rhoden, Tr. 359). Information is stored in the cell capacitor as either a high or low voltage. (Rhoden, Tr. 359). The cells of the DRAM are divided into an array via a series of rows and columns with the cells located at the intersections of those rows and columns. (Rhoden, Tr. 359-60). Access to the cell capacitor is made by activating a transistor, which transfers the voltage in the capacitor to a column, also known as a bit line. (Rhoden, Tr. 359-60).

6. In order for a DRAM to have any value, it must be compatible and interoperable with the other components in the same specific system that include the DRAM. (Peisl, Tr. 4410; CX 1075 at 1; Heye, Tr. 3655-65; Jacob, Tr. 5562-66).

2. The Production of DRAMs

a. The DRAM Manufacturing Process

7. The starting point in the manufacturing process is a bare silicon wafer. (Becker, Tr. 1116-17).

8. During the course of the manufacturing process, successive layers are built up on the silicon wafer. (*See generally* Becker, Tr. 1116-32). DRAMs require as many as twenty-two distinct layers. (Becker, Tr. 1131). Each layer requires a series of manufacturing steps. (Becker, Tr. 1131-32). Processing the wafer takes about four hundred manufacturing steps. (Becker, Tr. 1118, 1131).

9. The manufacturing process is nonlinear, meaning that a wafer will reenter different processing areas of the fab a number of times. (Becker, Tr. 1118). A processed wafer contains hundreds of individual DRAM chips. (Becker, Tr. 1117).

10. The processed wafer is electrically tested in order to find the good chips. (Becker, Tr. 1132-34). Such testing, however, does not identify all of the die with disqualifying defects. More stringent testing is only possible after the die have been packaged. (Geilhufe, Tr. 9570).

11. After testing, the wafer is cut into individual DRAMs. (Becker, Tr. 1132-34). The individual chips are then bonded to a metal lattice like structure called a lead frame and are covered with a black hard plastic mold compound. (Becker, Tr. 1132-34).

12. After packaging, the good chips are built into components and tested again. (Becker, Tr. 1135-36).

13. The tested components may also be assembled onto circuit boards to create modules and are further tested. (Becker, Tr. 1135; *see generally* Becker, Tr. 1132-36 (describing the process of how the chips are built into components and connected to modules)).

14. The largest part of a DRAM, approximately ninety percent of the active area, consists of the memory array, that is the memory cells and related circuitry. (Geilhufe, Tr. 9560). The remaining ten percent consists of peripheral circuitry. (Geilhufe, Tr. 9560). Circuitry for implementing the four features at issue here – programmable column address strobe ("CAS") latency, programmable burst length, dual edge clocking, and on-chip delay lock loop ("DLL") – are found in the peripheral circuitry. (Geilhufe, Tr. 9559).

15. The vast majority of DRAM development costs is spent on the memory array portion of the DRAM, including the manufacturing process and equipment development. (Geilhufe,

Tr. 9560-61). Development costs for the peripheral circuitry are much lower. (Geilhufe, Tr. 9560-61).

b. The Various Phases of DRAM Development

16. The development of the DRAM proceeds along a number of "phases" and milestones. Those are the design phase, the layout phase, the simulation phase, the verification phase, tape out, initial silicon, the validation phase, internal qualification phase, and the production phase. (Shirley, Tr. 4141-42; Reczek, Tr. 4306-41).

17. In the design phase, the DRAM designers implement the DRAM specification as a set of circuit designs or schematics. (Shirley, Tr. 4142-43).

18. In the layout phase, the layout designers take the circuit designs created in the first step and create a representation of the circuit designs. (Shirley, Tr. 4143).

19. In the simulation phase, the design engineers simulate the designs in order to verify that the chips will perform as intended before they are first manufactured. (Shirley, Tr. 4144).

20. The verification phase involves ensuring that the schematics created in the design phase are in fact represented by the work done in the layout phase. (Shirley, Tr. 4144-45; Reczek, Tr. 4309).

21. Tape out involves the process of transferring the DRAM layout onto masks that will be used in the fabrication of the DRAM. (Shirley, Tr. 4145). The collection of individual masks necessary to fabricate a DRAM design comprises a mask set. (Shirley, Tr. 4147).

22. A mask contains an image that is transferred to the wafer through a process of using light to expose the wafer to the image

pattern in the mask and using gasses to etch the resulting pattern into the wafer. (Becker, Tr. 1122-24).

23. At some DRAM manufacturers, including Micron Technologies, Inc. ("Micron"), the physical creation of masks is done by specialized firms that provide the service to the DRAM manufacturers. (Shirley, Tr. 4145-46). Other DRAM manufacturers, including Infineon Technologies ("Infineon"), produce their own masks. (Reczek, Tr. 4312).

24. The mask set, once it is received, is used to create the first physical manifestation of the DRAM chips on wafers. Those wafers represent a milestone and are referred to as "initial silicon." (Shirley, Tr. 4147).

25. Initial silicon is then tested in the validation and internal qualification phases to ensure that the DRAM on the wafers operate the way they were intended (the validation phase) and that the DRAM on the wafers operate appropriately in the expected environments (the qualification phase). (Shirley, Tr. 4148-49).

c. Design Modification During DRAM Production

26. The DRAM industry transitions between different versions of DRAM quite frequently. As a witness from Micron explained:

> Switching from one product to another, while still using the same core technology, involves only changing priorities in design and product engineering and may mean some differences in our assembly and test equipment purchases. SDRAM, SLDRAM, nDRAM all use the same fab equipment and core DRAM technology. *In short, while the flavors might change, it's still a DRAM*.

(RX 836 at 3) (emphasis added).

B. The Memory Bottleneck Problem

27. Dr. Michael Farmwald, one of the two founders of Rambus, received his bachelor's degree in mathematics from Purdue University in 1974. (Farmwald, Tr. 8058). He then earned a Ph.D. in computer science from Stanford University in 1981. (Farmwald, Tr. 8059). While a graduate student at Stanford, Dr. Farmwald was in charge of a supercomputer project at Lawrence Livermore National Labs. (Farmwald, Tr. 8059). After obtaining his Ph.D, he continued to work at Livermore for four years and then founded a company called FTL (which stood for "Faster Than Light"), whose goal was to build very fast computers. (Farmwald, Tr. 8060-61). In 1988, Dr. Farmwald went to the University of Illinois to teach in the computer science department. (Farmwald, Tr. 8063-64).

28. While working as a professor at the University of Illinois, Dr. Farmwald realized, and it was a general perception in the DRAM industry, that developments in microprocessor technology would lead to significant speed increases in microprocessors while memory chip performance would not keep up. (Farmwald, Tr. 8063, 8067). He recognized that the result of these trends would be a "bottleneck" – memory technology would limit computer system performance. (Farmwald, Tr. 8068-69).

29. Moore's law, named after Gordon Moore, founder of Intel Corp. ("Intel"), predicts that processor speeds will increase by a factor of four every three years. (Farmwald, Tr. 8068). This "law" has held true for over the last two decades. (Farmwald, Tr. 8068). The performance of DRAMs, however, was increasing at a lesser rate; while DRAMs were fast in comparison to microprocessors in the early 1980s, as an historical matter, DRAM performance had increased very slowly over time. (Farmwald, Tr. 8072).

30. Graphing predicted microprocessor speeds against memory performance, Dr. Farmwald predicted an ever increasing

gap between microprocessor performance and DRAM performance. (Farmwald, Tr. 8071-73).

31. Assuming that the predicted DRAM speeds were not improved, Dr. Farmwald projected that the number of DRAMs needed to support future microprocessors would become extremely large over time. (Farmwald, Tr. 8073).

32. The increasing number of DRAMs needed to support faster computers was also consistent with Dr. Farmwald's experience that microprocessors were demanding higher and higher bandwidth memory systems ("bandwidth" being the amount of information that can be transferred over a specific period of time). (Farmwald, Tr. 8076-79).

33. Dr. Farmwald also plotted the projected price for computers, which showed that the cost for computer systems was dropping over time. (Farmwald, Tr. 8074-75). Comparing these projected costs with the number of DRAMs that would be required to support the bandwidth needs of faster microprocessors, Dr. Farmwald knew that "there was something broken" – the costs of the thousands of DRAMs needed at higher microprocessor speeds would prevent the decline of computer system prices. (Farmwald, Tr. 8075-76).

34. Later, a 1992 Rambus "Corporate Backgrounder" described the issue: "[o]ne of the most serious problems is the chronic speed mismatch between processors and main memory. Designers refer to this as the memory bottleneck. The data transfer rates of memory ICs [integrated circuits] lag far behind a processor's ability to handle the data." (RX 81 at 4).

35. To meet the higher bandwidth needs of microprocessors without the overwhelming cost of thousands of DRAMs, DRAM performance had to increase at a higher rate. (Farmwald, Tr. 8076).

36. Years later, Dr. Farmwald's 1988 observations were recognized by others in the industry. For example, an April 1992 internal memorandum of Siemens AG ("Seimens") states that "[a]s a result of the trend toward increasingly faster RISC and CISC processors, the DRAM interface has become more and more of a problem for system developers. In order to eliminate this data transmission rate bottleneck, various competing concepts regarding the design of newer DRAMs have emerged . . . ." (RX 285A at 1).

37. Similarly, an October 1992 article published in the Institute of Electrical and Electronic Engineers, Inc. ("IEEE") Spectrum warned, "[i]f the price-to-performance ratio of computer systems is to keep improving, the gap in speed between processors and memory must be closed." (RX 329 at 1). IEEE Spectrum is the overall general magazine for the IEEE, a professional organization of electronic and electrical engineers. (Prince, Tr. 8972-73). The article went on to explain that "the accepted dynamic RAM (DRAM) architectures and solutions have been pushed to their limits. A basic change in architecture seems the only way to obtain an urgently needed increase in memory speed." (RX 329 at 1). This article reflected a general discussion within the industry in 1992 that computer companies needed faster DRAMs. (Prince, Tr. 8977-78).

38. Another article in the October 1992 IEEE Spectrum stated, "[i]f dynamic RAMs and processors are to trade data at close to top speed, the interface between them must be re-engineered. . . . None of the types of interfaces now popular can do this while conserving power and cost to the desired degree." (RX 333 at 1).

39. In February 1994, Dr. Betty Prince, a long-time consultant in the DRAM industry and the author of five books on DRAM technologies (Prince, Tr. 8970-72), wrote in an article published in IEEE Spectrum that "the mismatched bandwidths of fast processors and the slower memory chips they must employ are a problem of long standing. Processors now as always require more

data per unit time than many standard memory chips have been designed to provide." (RX 465 at 1). She also provided a graph showing that this performance gap was increasing over time. (RX 465 at 1). Dr. Prince agreed that the performance gap she wrote about created a bottleneck. (Prince, Tr. 8990-91).

40. Intel saw the memory bottleneck coming in 1995, and the recognition of this bottleneck prompted Intel to investigate various memory technologies in an effort to remedy the situation. (MacWilliams, Tr. 4929-30).

C. Farmwald's and Horowitz's Inventions Solve the Memory Bottleneck Problem by Addressing Numerous Issues

41. In 1988, Dr. Farmwald conceived the general idea of a new memory interface and protocol (an organization of the bits and timing of bits transferred by a memory chip) that would allow a single DRAM chip to have higher performance than a board Dr. Farmwald had designed containing 320 existing DRAM chips. (Farmwald, Tr. 8086-88).

42. In order to progress beyond his initial ideas Dr. Farmwald realized that he needed the assistance of an expert in circuit design. (Farmwald, Tr. 8089). Dr. Farmwald sought the help of a former colleague – Dr. Mark Horowitz, a professor at Stanford. (Farmwald, Tr. 8089-90).

43. Dr. Horowitz had completed both his bachelors and masters degrees in electrical engineering from MIT in four years, receiving the degrees in 1978. (Horowitz, Tr. 8477). After working for a year at Signetics, he then earned a Ph.D. in integrated circuit design from Stanford University in 1983. (Horowitz, Tr. 8477-80). Dr. Horowitz has been a professor in the electrical engineering and computer science departments at Stanford University since the mid-1980's. (Horowitz, Tr. 8476).

Dr. Horowitz currently holds two endowed chairs at Stanford. (Horowitz, Tr. 8482).

44. Dr. Farmwald convinced Dr. Horowitz to take a year's leave from Stanford to further explore their ideas. (Farmwald, Tr. 8092-93). Starting in the spring of 1989, the two worked from Dr. Horowitz's Palo Alto home. (Farmwald, Tr. 8093-94).

45. Dr. Horowitz's goal was to build the fastest possible DRAM interface. (Horowitz, Tr. 8486). Drs. Horowitz and Farmwald determined that 500 megahertz ("MHz") DRAM operation might be possible, and they worked toward that goal. (Horowitz, Tr. 8505-06).

46. In creating their inventions, Drs. Farmwald and Horowitz had to solve numerous problems. (Horowitz, Tr. 8487). They realized that current memory interfaces could not run at high speeds as a result of electrical issues, clocking issues, and issues relating to the protocol, and that they would need innovations in each of these areas in order to meet their goal. (Horowitz, Tr. 8487-88).

1. Electrical Issues

47. With respect to electrical issues, Drs. Farmwald and Horowitz needed to develop driver and receiver circuitry that could generate very high-speed signals, and they also needed to develop a bus that would allow the signals to propagate. (Farmwald, Tr. 8118-20; Horowitz, Tr. 8488).

48. Drs. Farmwald and Horowitz developed a number of solutions to the electrical issues that arose. First, they realized that reflected signals from the end of the bus lines would be a serious problem at high speeds and conceived the idea of introducing resistors to "terminate" the bus lines and reduce reflections. (Horowitz, Tr. 8492-93).

49. Second, Drs. Farmwald and Horowitz realized that the high voltage signaling then in use would generate too much power at high speeds, and they developed low voltage signaling using a particular kind of driver called a "current mode" or "current source" driver. (Farmwald, Tr. 8119, 8144-45; Horowitz, Tr. 8494-95; RX 82 at 9).

50. Third, Drs. Farmwald and Horowitz realized that they could not build a 500 MHz DRAM with current technology and so, to transmit data at the highest possible speed, they conceived the idea of transmitting and receiving data on both edges of a 250 MHz clock. (Farmwald, Tr. 8118; Horowitz, Tr. 8495-97).

2. Clocking Issues

51. With respect to clocking issues, Drs. Farmwald and Horowitz realized from personal experience that, although current memory chips were asynchronous, they would have to develop a synchronous device with mechanisms for exercising very tight control over timing with respect to the clock to make sure that each bit of data – traveling at a very high speed – was sampled at the right time. (Horowitz, Tr. 8488-89; *see infra* F. 52-53, 284 for discussion of asynchronous versus synchronous devices).

52. Drs. Farmwald and Horowitz decided to design a synchronous system since the timing reference provided by a clock could be used to limit timing uncertainties in the system and allow for high speed performance. (Horowitz, Tr. 8499-502).

53. Even in a synchronous system there remain some timing uncertainties; for example, expected delays of the buffers may vary from DRAM to DRAM due to differences in their fabrication. (Horowitz, Tr. 8503-04). In order to have the highest speed possible, Drs. Farmwald and Horowitz wanted to minimize this remaining uncertainty to the extent possible; they therefore came up with the idea of using a delay locked loop (DLL) or a

phase locked loop (PLL) on-chip. (Farmwald, Tr. 8118; Horowitz, Tr. 8504).

3. The Memory Interface Protocol

54. With respect to the design of the protocol, additional optimizations developed for high speed operation included returning a variable amount of data in response to a request rather than a single bit of data and by putting registers and associated control circuitry directly on the DRAM. (Farmwald, Tr. 8115; Horowitz, Tr. 8489-90).

55. With respect to the protocol, Drs. Farmwald and Horowitz again came up with various innovations. As one example, they decided to put registers on the DRAM to make the interface more efficient. (Farmwald, Tr. 8115-16; Horowitz, Tr. 8506). These registers would be programmed with parameters, such as the address range that a particular DRAM would respond to or the access time of the DRAM. (Horowitz, Tr. 8507, 8509-10).

56. Drs. Farmwald and Horowitz wanted to make the access time variable for two reasons. First, if the bus were improved so that it could operate at a faster clock frequency, the access time of the DRAM could be adjusted so that it would operate with that faster clock. Second, a variable access time would allow the access times of all the DRAMs in a system to be adjusted to have the same access time. (Horowitz, Tr. 8510-11).

57. As another example of an innovation related to the protocol, Drs. Farmwald and Horowitz allowed the response to a request to include a variable amount of data, a feature known as “variable block size” or “variable burst length.” (Farmwald, Tr. 8116-17, 8146; Horowitz, Tr. 8512; RX 82 at 9).

II. RAMBUS: COMPANY DEVELOPMENT AND PUBLIC PROMOTION OF TECHNOLOGY

A. The Founding of Rambus

58. Drs. Farmwald and Horowitz founded "Rambus Inc." in March of 1990. (CX 545 at 5; RX 81 at 19). By 1992, its headquarters were located in Mountain View, California, in Silicon Valley. (RX 81 at 1, 3).

59. Rambus is, and at all relevant times has been, a corporation as "corporation" is defined by Section 4 of the Federal Trade Commission Act, 15 U.S.C. § 44; and at all relevant times has been and is now engaged in commerce as "commerce" is defined in that same provision. (Answer, ¶¶ 5, 6).

60. Rambus designs, develops, licenses, and markets both nationally and internationally, high-speed chip connection technology to enhance the performance of computers, consumer electronics, and communications systems. (Answer, ¶ 5). Rambus is a pure-play licensing company; it does not manufacture DRAM, but rather uses research and development to invent new DRAM technologies and makes its money by licensing its technology to others. (Teece, Tr. 10350-51).

61. For the fiscal year that ended on September 30, 2001, Rambus reported revenues of approximately $117 million. (Comp., ¶ 5; Answer, ¶ 5).

62. Rambus's founders intended to improve memory performance through multiple inventions based on modifications of standard DRAMs (*see* CX 533 at 2), which could be used separately or in combination(s). The greatest performance gains would be realized by using these inventions in combination. Rambus DRAM or "RDRAM" is the name for the "revolutionary DRAM architecture and high speed chip-to-chip data transfer technology" that incorporates several of Rambus's inventions,

including its proprietary bus technology. (RX 81 at 3). Each of the various generations of RDRAM are manufactured in accordance with specifications established through a collaboration among Rambus and its DRAM partners. (Farmwald, Tr. 8149, 8241).

63. Early on, Rambus realized that it was important to its business strategy to protect the intellectual property rights to its technology. (CX 535 at 1). Part of its early strategy to do this was to pursue an application for "a basic, broad patent filed in all major industrial nations" and thereafter "follow up with additional patents on inventions created during the development of the technology." (CX 535 at 1). It was also important to Rambus to enter into nondisclosure agreements with companies exposed to its technology. (CX 535 at 1).

64. The only business model that "made any sense" to Rambus co-founder Michael Farmwald "was to patent [the technology], convince others to build it, and charge them royalties" because "[w]hen we were first formed, it was my view that we could not possibly raise enough money to build DRAMs. DRAM fabs cost, even back then they cost, [sic] order of a billion dollars. You couldn't really build DRAMs without owning your own fab, and so a business plan which involved actually building and selling DRAMs was hopeless, and so from the very beginning we were a royalty-based company." (Farmwald, Tr. 8095; CX 2106 at 27 (Farmwald, Dep.)).

65. Rambus's primary objective was to commercialize the revolutionary inventions Drs. Farmwald and Horowitz had created in the form of an open industry *de facto* standard, and to ensure that the standard "didn't go off in incompatible directions." (Farmwald, Tr. 8110, 8125-26, 8148).

66. Rambus contemplated that it would earn its income by working with DRAM companies to implement the Rambus interface in their products, and, for that work, get paid consulting fees (for the time its engineers spent working with partners) and

royalties for the use of Rambus's intellectual property that would be incorporated into DRAM companies' products. (Farmwald, Tr. 8150).

67. To become and remain a viable company, it intended to charge low single digit royalties, which it believed to be fair in light of the importance of Rambus's intellectual property contribution to the product and the large size of the DRAM market. (Farmwald, Tr. 8128; CX 1282 at 5).

68. Rambus founder Farmwald knew that companies never like to pay royalties unless they have to and they can not "get out of it." (CX 2106 at 27 (Farmwald, Dep.)).

1. Securing Venture Capital Funding

69. In an effort to receive funding for the start-up of Rambus Inc., the founders approached various venture capital firms: Kleiner Perkins, one of the largest venture capital firms in the world; Merrill Pickard Anderson and Eyre; and Mohr Davidow. (Farmwald, Tr. 8099). As part of the meetings with the venture capital firms, the founders prepared presentations and showed them documents, such as early business plans. (Farmwald, Tr. 8100). These meetings occurred around the time of a June 1989 RamBus Business Plan. (Farmwald, Tr. 8100-01; *see* CX 533).

70. The start-up had significant financial considerations and according to the June 1989 business plan, "RamBus" founders (Michael Farmwald, Mark Horowitz), were able to invest $75,000 in "seed money" and were seeking an additional $1.5 million in equity investment. (CX 533 at 4). This amount would only fund the company through "the completion of a prototype and to the development of [its] initial DRAM vendor partnerships." (CX 533 at 4). Until it signed with its revenue producing partners, estimated expenses were $100,000 per month. (CX 533 at 5).

71. In March 1990, Rambus Inc. was born after receiving venture capital funding of $1.86 million from three firms. (CX 545 at 5; RX 81 at 19).

2. Early Business Plan for the Farmwald/Horowitz Inventions

72. As a 1989 draft business plan explained, Farmwald and Horowitz hoped to establish a *de facto* standard "by offering all interested DRAM and central processing unit ("CPU") vendors a sufficiently low licensing fee (2%) that it will not be worth their time and effort to attempt to circumvent or violate the patents." (RX 15 at 9).

73. Dr. Farmwald explained, "[w]e were going to try and find customers for our parts, big customers, and we were going to try and license all the DRAM makers to build our part to supply those customers," which would lead to *de facto* standardization. (Farmwald, Tr. 8124-25).

74. The founders intended to use a program of phased licensing and promotion of its proprietary RDRAM technology in order to convince the industry to adopt its proprietary technology as the industry standard. (Farmwald, Tr. 8297).

75. The plan was for their technology to be an "open standard"; they refused to license its technology on exclusive terms. (Farmwald, Tr. 8185; RX 25 at 16).

76. An "open standard" in the DRAM industry is a standard for which any patents that apply to it are available on reasonable and nondiscriminatory terms. (Bechtelsheim, Tr. 5897; CX 2112 at 190-91 (Mooring Dep.)).

77. Farmwald and Horowitz wanted to avoid what happened to the Sony Betamax, which was hampered in the market by restrictive licensing. (Farmwald, Tr. 8165-66). Instead, their goal

was to license the technology "openly and fairly to everybody so everyone is on equal footing with a relatively low royalty." (Farmwald, Tr. 8165-66).

78. Their early business plans indicate that they were aware that it would be necessary early on to charge lower royalties in order to foster acceptance of their proprietary technology. They recognized that there was a "trade-off of royalty size vs. incentive to develop alternatives" to their technology. (CX 533 at 14).

79. To ensure that the Farmwald/Horowitz technology was standardized, i.e., that parts from one manufacturer were interchangeable with parts from another manufacturer, the inventors planned to cooperate with their partners (i.e., the licensees who would manufacture the devices) to ensure that feedback was propagated to all partners so that everyone would use the same good ideas instead of creating customized parts. (Farmwald, Tr. 8148; *see* RX 82 at 17).

80. Farmwald and Horowitz believed that they had compelling, revolutionary ideas, that their patents would be significant, and that a small royalty would be palatable given the performance leap of the technology. (Farmwald, Tr. 8112-13).

81. The key to success for Farmwald and Horowitz was that they "had to find a number of high-volume customers and high-volume producers to produce the part so that it became the part that everybody was using" in order for their technology to become a *de facto* standard. (Farmwald, Tr. 8140; CX 1750 at 1).

82. To this end, the inventions were designed to be produced using existing DRAM manufacturing technology. (Farmwald, Tr. 8142-43; RX 82 at 6).

B. The RDRAM Technology

83. Because from the start the founders believed that "[r]oyalties are the lifeblood of Rambus" (CX 2106 at 221 (Farmwald, Dep.)), Rambus placed great importance on promoting and protecting its proprietary technology. The Rambus founders "felt we had a very significant invention. We felt that the only way to protect and to extract value from that invention was to patent it." (CX 2106 at 28 (Farmwald, Dep.)).

84. Rambus saw its proprietary Rambus DRAM ("RDRAM") technology as offering dramatic improvements over existing memory technology of the time. In 1992 it claimed that RDRAM technology "achieves a ten-fold increase in component throughput" and would result in "dramatically increasing system price/performance." (RX 81 at 3). In addition, Rambus claimed that use of the RDRAM technology "assures a smaller system with fewer components, and provides the user with a modular, scalable solution." (RX 81 at 3).

85. The high-speed chip-to-chip data transfer RDRAM technology was intended to be used not only in memory chips themselves, but also to be implemented in other chips including memory controllers, processors, graphics/video chips and other high performance components used in virtually every computer system. (RX 81 at 3). The proprietary Rambus technology was targeted at mainstream applications from consumer digital video products to desktop computers and graphics up to massively parallel computers. (RX 81 at 3).

86. The RDRAM technology in the early 1990's included numerous inventions relating to the bus, the interface between the bus and computer chips, and the DRAM. The 1992 Corporate Backgrounder makes clear that the Rambus "solution is comprised of three main elements: the Rambus Channel, the Rambus Interface, and the RDRAM." (RX 81 at 6). The Rambus Channel refers to the bus, while the Rambus Interface and

RDRAM refer to other Rambus innovations separate from the bus. (RX 81 at 7). Each of these elements contain a number of independent inventions. (RX 81 at 8-11).

87. RDRAM narrow bus technology contemplates the use of circuitry on the chips at either end of the bus connection to optimize the signals flowing across the connection. (Horowitz, Tr. 8488-90). This circuitry contains high-level logic which implements a protocol for the chip-to-chip information transfer. (Horowitz, Tr. 8489-90).

88. One of the ways that RDRAM technology achieves a high-speed data transfer over the narrow bus is through "multiplexing," which means that the bus can carry different pieces of information at different points in time. (Horowitz, Tr. 8620-21). This aspect of the RDRAM interface protocol means that over several clock cycles the bus can carry a combination of address and control and data signals on one or more of the same bus lines. (Horowitz, Tr. 8620-21; *see* Rhoden, Tr. 402-03).

89. Another aspect of the RDRAM technology is the use of a "packetized" data transfer protocol. (Horowitz, Tr. 8621; Rhoden, Tr. 403-05). This term means that information is bundled and the bundle may be sent over multiple clock cycles rather than transmitted all at once. (Jacob, Tr. 5465; Rhoden, Tr. 403-04).

90. The RDRAM technology also contains various other distinctive aspects, including a clocking system, sometimes referred to as a loop clock, to assist in controlling the synchronization of the data transfer between chips (Rhoden, Tr. 404; Horowitz, Tr. 8647), and a method of physically packaging the RDRAM memory chips so that multiple chips could be vertically mounted on one another to occupy a small space. (Horowitz, Tr. 8623).

91. The RDRAM technology was sufficiently distinctive that it was widely considered "revolutionary" in the industry and was

promoted as such by Rambus. (Horowitz, Tr. 8571; Gross, Tr. 2291; Heye, Tr. 3686-87).

C. The 1990 Business Plan

92. Early Rambus investors were informed that "[t]he primary business of the RamBus Company" would be to license proprietary technology "to manufacturers of DRAM chips and microprocessors"; that "[t]he DRAM market is . . . highly sensitized to the concept of standardization"; and that market conditions were such that there is "the ability to set world wide standards for the next generation of DRAM chips and memory systems." (CX 533 at 9).

93. The purpose of this early draft of its business plan was to encourage investment by explaining to investors why Rambus's technology would enable Rambus to be successful in the existing and future DRAM market. (*See generally* CX 533 at 9-10).

94. Investors were told that "the patented RamBus technology . . . has the opportunity to establish a single high performance DRAM standard," that in part due to "[t]he DRAM industry's penchent [sic] for standardization," once the Rambus technology was licensed to "all major vendors," it would be "extremely unlikely that any potential competitor would be able to gain critical mass enough to challenge" Rambus; and that such considerations, including the existence of "strong barriers to entry" restraining "potential competitors," made Rambus an "exceptionally attractive investment opportunity." (CX 533 at 9).

95. The strength of Rambus's business model depended also on the strength of its technological innovations. Indeed, Rambus's early filed broad patent application and the advantage its technology was seen to enjoy by virtue of being "faster, denser, lower power and cheaper than any other approach" were touted to investors as the most significant barriers to entry for potential, follow-on competitors. (CX 533 at 9). It was the "stiff

competition" presented by Rambus innovative technology as well as its marketing strategy of licensing all of the major vendors that it claimed made it less pervious to competitors than other potential investment opportunities. (CX 533 at 9).

96. Rambus hired its first (and to date only) Chief Executive Officer – Geoffrey Tate – who joined Rambus in May 1990. (CX 545 at 5).

D. RDRAM Promotion and Licensing Strategy

97. By November 1990, Rambus had begun its efforts to promote and protect its technology. (CX 535 at 4-5). At that date Rambus had filed for, but not yet obtained, a base patent on its technology (CX 535 at 3) and had entered into license contracts that compelled partners to use Rambus technology patents and trade secrets only for use in RDRAM-compatible chips. (CX 535 at 4-5).

98. By June 1992, Rambus had signed technology license agreements with NEC Corp. ("NEC"), Toshiba Corp. ("Toshiba"), and Fujitsu Laboratories, Ltd. ("Fujitsu"). (CX 543A at 11). By January 1994, Rambus had signed license agreements with Hitachi, Ltd. ("Hitachi"), Oki Electric Industry Co. ("Oki"), Lucky Goldstar, and Intel. (CX 547 at 12). These agreements involved substantial interaction between Rambus and the licensees. (Farmwald, Tr. 8241).

99. In the course of negotiating with DRAM manufacturers and others, Rambus encountered resistence to its business model, and specifically to royalties. (CX 711 at 13, 61). "A few systems companies and IC [integrated circuit] companies have had a very negative reaction to our business model. Some believe that it is not 'fair' that we are wanting to charge a royalty on ICs that incorporate our technology. Others believe our royalty will make ICS incorporating our technology 'too expensive.' Two specific examples are Sun and Tseng." (CX 543A at 14).

100. Rambus limited the use of its license agreements to so-called RDRAM compatible uses only. Most companies accepted this term. Samsung Electronics Co., Ltd. ("Samsung"), however, insisted on an agreement without field of use restrictions. (CX 767).

101. In 1994, Samsung recognized that Rambus's inventions could be used in non-compatible Rambus parts, i.e. in parts without Rambus's proprietary bus technology. (CX 767). Moreover, Rambus made it clear to Samsung that Rambus's intellectual property rights were not limited to the RDRAM product. (CX 2078 at 116 (Karp, Dep.)).

E. Presentation of the Rambus Inventions to the DRAM Industry

1. Rambus Visits to DRAM Manufacturers and Systems Companies

102. In 1989-90, Drs. Farmwald and Horowitz made visits to many DRAM manufacturers and systems companies to try to convince them about the benefits of their approach and to get feedback from them. (Horowitz, Tr. 8515).

103. Among the DRAM manufacturers that Drs. Farmwald and Horowitz visited in 1989-90 were Texas Instruments, IBM, Toshiba, Fujitsu, Mitsubishi Electric Corp. ("Mitsubishi"), NEC, Matsushita Elect. Indus. Co., Ltd. ("Matsushita"), Micron, and Siemens (whose former semiconductor division is now Infineon Technologies). (Horowitz, Tr. 8515; Farmwald, Tr. 8166).

104. Among the systems companies that Drs. Farmwald and Horowitz visited in 1989-90 were IBM (both a DRAM manufacturer and a systems company), Sun Microsystems ("Sun"), Motorola, Apple Computer ("Apple"), SGI, and Tandem. (Horowitz, Tr. 8515; Farmwald, Tr. 8166-67).

105. The response to the early presentations in 1989-90 was "just disbelief" that Drs. Farmwald and Horowitz would be able to achieve a 500 megabit per second DRAM data rate. (Horowitz, Tr. 8516). People who listened to these presentations were also skeptical about many of the specific features of the technology. For example, it was felt that putting registers on a DRAM was too expensive for a commodity part and that one could not put a phase locked loop or a delay locked loop on the DRAM itself. (Horowitz, Tr. 8517).

106. The four inventions at issue in this case were described in these early presentations. For example, one of the early presentations that Dr. Horowitz gave, with slides dated January 31, 1990, states that the Rambus interface "allows 'block mode' transfer from an individual DRAM" with "1-1024 byte long blocks supported." (RX 29 at 9; Horowitz, Tr. 8518-20). This describes variable block size or variable burst length. (Horowitz, Tr. 8520).

107. The January 31, 1990 presentation also describes the use of a delay locked loop on the DRAM to reduce clock skew. (RX 29 at 33-34; Horowitz, Tr. 8521-22).

108. The January 31, 1990 presentation also refers to the dual-edge clock or double data rate technique. (RX 29 at 34; Horowitz, Tr. 8522-23).

2. Preparation and Description of the Rambus Inventions Through Various Technical Publications

109. In the 1990-91 period, Dr. Horowitz prepared detailed technical descriptions of the Rambus technology. (Horowitz, Tr. 8523). These documents were for Rambus's internal use and were also used with customers and potential customers to convince them of the merits of Rambus technology and to help them build it. (Horowitz, Tr. 8523-24). These documents disclose all four of the relevant product markets in this case: dual-edge clocking, on-

chip DLL, programmable CAS latency, and programmable burst length.

a. The May 1990 Technical Description

110. One of these technical descriptions is dated May 7, 1990 and was generated at about that time. (RX 63; Farmwald, Tr. 8168-69; Horowitz, Tr. 8524-25).

111. The May 7, 1990 technical description described all four of the technological features at issue in this case. (Horowitz, Tr. 8525-29).

112. For example, the technical description described dual-edge clocking in a figure with two input receivers, one clocked by a signal designated "CLK" (clock) and the other clocked by the complement of CLK (clock bar), a signal that is zero when clock is one and vice versa. (RX 63 at 10; Horowitz, Tr. 8525-26). This means that one receiver samples an input when the clock goes high (the rising edge of the clock) and the other when the clock goes low (the falling edge). (Horowitz, Tr. 8526).

113. The May 7, 1990 technical description also described a delay-locked loop on the DRAM (on-chip DLL feature). (Horowitz, Tr. 8527-28). A figure in the technical description shows two delay locked loops generating the internal clocks for Rambus's design. (RX 63 at 14; Horowitz, Tr. 8527).

114. The May 7, 1990 technical description also described programmable latency. (Horowitz, Tr. 8528). In the "device registers" section of the document, an "access time" or latency register is listed. (RX 63 at 18; Horowitz, Tr. 8528). "Latency" refers to the time between request and response. (Horowitz, Tr. 8530). The document explains that a fixed value for latency "does not allow for technology improvements," and, consequently, the Rambus system "set[s] the time between request and response during system reset." (RX 63 at 5-6; Horowitz, Tr. 8530-31). In

other words, the value in the access time or latency register would be fixed when the system was started up and probably would not be changed after that time. (Horowitz, Tr. 8531).

115. The May 7, 1990 technical description also described variable burst length. (Horowitz, Tr. 8528-29). The document contains a table showing a variable number of bytes in the block size or burst length depending on the value in the "BlockType" field. (RX 63 at 21; Horowitz, Tr. 8528-29).

b. The November 1990 Technical Description

116. A later Rambus technical description, dated November 5, 1990, was generated around that time. (RX 94; Farmwald, Tr. 8169; Horowitz, Tr. 8535).

117. The November 5, 1990 technical description was sent to Siemens (now Infineon). (RX 99; Farmwald, Tr. 8169-70).

118. The November 5, 1990 technical description described dual-edged clocking. First, the document contains the same figure relating to inputting data on both edges of the clock as in the May 7, 1990 description. (RX 63 at 10; RX 94 at 15; Horowitz, Tr. at 8535-36). Second, the document shows that the output data is also being transmitted on both edges of the clock. (RX 94 at 19; Horowitz, Tr. 8536).

119. The November 5, 1990 technical description described two alternatives for the DRAM clock circuitry. One alternative was to use a phase locked loop. (RX 94 at 45; Horowitz, Tr. 8536-37). The other alternative was to use delay locked loops. (RX 94 at 46; Horowitz, Tr. 8537).

120. The November 5, 1990 technical description described variable latency using a data delay field in the request packet. (RX 94 at 59; Horowitz, Tr. 8537-38).

121. The November 5, 1990 technical description described variable block size or burst length with a table similar to that in the May 7, 1990 technical description. (RX 63 at 21; RX 94 at 60; Horowitz, Tr. at 8538).

c. Siemens Responds With a List of Questions About Rambus Technology

122. Both Dr. Farmwald and Dr. Horowitz received feedback from Siemens regarding the November 5, 1990 technical description. (RX 102; RX 117; Farmwald, Tr. 8171-72; Horowitz, Tr. 8541-42).

123. A fax from K. Horninger of Siemens to Dr. Farmwald, dated December 7, 1990, contained a detailed list of questions relating to the November 5, 1990 technical description. (RX 102; Farmwald, Tr. 8171-73).

124. A fax from H.J. Neubauer of Siemens to Dr. Horowitz, dated January 29, 1991, stated "Dear Dr. Horowitz, concerning the RAMBUS Technical Description some basic items remained open. In the following we present a list of detailed questions to you which we would like to get answered." (RX 117 at 2; Horowitz, Tr. 8542).

125. A number of the questions in the fax that Siemens sent to Dr. Horowitz related to the four features of Rambus technology at issue in this case. (*See* RX 117).

126. Question number one in the Siemens fax asked about the details of how eight bits of data would be transmitted by the DRAM and relates to Rambus's variable block size feature. (RX 117 at 2; Horowitz, Tr. 8543-44).

127. Question number two in the Siemens fax asked about the implementation of variable latency in the Rambus technology. (RX 117 at 2; Horowitz, Tr. 8544).

128. Another question in the Siemens fax referenced Figure 13 on internal page 14 of the November 5, 1990 technical description. (RX 117 at 4). That figure showed dual-edge clocking or double data rate on the output. Dr. Horowitz's understanding was that Siemens's question related to the implementation of the double data rate drivers as shown in the November 5, 1990 technical description. (RX 94 at 19; RX 117 at 4; Horowitz, Tr. 8546).

129. Another question in the Siemens fax referenced Figure 28 on internal page 41 of the November 5, 1990 technical description. (RX 117 at 4). That figure shows a delay locked loop and Siemens's question was about the delay locked loop. (RX 94 at 46; RX 117 at 4; Horowitz, Tr. 8546).

d. The April 1991 Technical Description

130. A still later Rambus technical description was released on April 1, 1991 and was a more complete version with many more technical details. (RX 130; Farmwald, Tr. 8171; Horowitz, Tr. 8538).

131. The April 1, 1991 technical description described dual-edged clocking. (RX 130 at 36; Horowitz, Tr. at 8539).

132. The April 1, 1991 technical description described using a phase locked loop on the DRAM. (RX 130 at 56; Horowitz, Tr. 8539).

133. The April 1, 1991 technical description described programmable latency through the use of a "read delay" or latency register. (RX 130 at 94; Horowitz, Tr. 8539-40).

134. The April 1, 1991 technical description described variable block size or burst length, with the value in a "count" field representing the number of bytes to be transferred. (RX 130 at 64; Horowitz, Tr. at 8539).

F. The March 1992 Press Events

135. On March 9, 1992, Rambus held simultaneous events in the Silicon Valley and in Tokyo to publicly announce its technology and its business plan. (Farmwald, Tr. 8182-84; RX 67 at 1). Prior to this date, Rambus had presented its technology to companies on an individual basis and had secured licenses from three of the top five DRAM manufacturers: Fujitsu, NEC, and Toshiba. (RX 67 at 2).

136. The press release announcing these events stated that Rambus's revolutionary technology would offer a tenfold improvement over traditional DRAMs and would solve the memory bottleneck. (RX 67 at 1). The press release also described Rambus's business plan as licensing its technology in return for license fees and royalties. (RX 67 at 2). By controlling the Rambus interface standard, Rambus would ensure compatibility. (RX 67 at 2). The press release also made it clear that Rambus's "open standard" would be "available for license by any IC [Integrated Circuit] company." (RX 67 at 2; *see also* Farmwald, Tr. 8185).

137. At the events, Rambus made available a "Corporate Backgrounder" that provided an overview of Rambus's business strategy and its technology. (RX 81; Farmwald, Tr. 8186). The Backgrounder explicitly detailed Rambus's intellectual property strategy: "Rambus Inc. is fully protecting the intellectual property rights of its technology by filing basic, broad patents in all major industrial nations around the world." (RX 81 at 3).

138. Later in this same public document, there are descriptions of Rambus's technology. (RX 81 at 8-11). The Backgrounder states that Rambus's "dramatic performance improvements were achieved through numerous technical breakthroughs" and then proceeds to describe "some of the major technical highlights of the Rambus solution." (RX 81 at 8). The technology descriptions

included the use of dual-edge clocking: "[a]n innovative electrical interface permits the Rambus Channel to operate at 500 Megabytes/second by using both edges of a 250 MHz clock." (RX 81 at 8). Moreover, the technology descriptions explicitly state that Rambus used the on-chip PLL/DLL technology: "[c]lock skew and capacitive loading are minimized by a phase lock loop circuit on board both the master and the RDRAM." (RX 81 at 8).

139. The Backgrounder also made it clear that Rambus's technology was divided into three distinct elements of the memory system: the Rambus Channel (the high-speed bus); the Rambus Interface (the circuitry that connects a device, such as a controller or DRAM, to the bus); and the Rambus DRAM (the memory itself). (RX 81 at 7; Farmwald, Tr. 8188-90).

140. The Backgrounder also stated that Rambus's business strategy was to license its technology, work with the licensee to help implement the technology, and to receive fees and royalties in return. (RX 81 at 3; *see also* Farmwald, Tr. 8186-87).

141. Later that year, at the invitation of Betty Prince, a long-time consultant in the DRAM industry (Prince, Tr. 8970-72, 8986-87), Dr. Farmwald and David Mooring of Rambus published an article in the October 1992 issue of IEEE Spectrum, which gave a brief description of the Rambus technology and stated that the "technology behind the architecture can be licensed for a royalty fee comparable to that for other patented technologies." (RX 332 at 1).

142. During the early 1990's Rambus's business model was well known in the industry. Brett Williams, a JEDEC Solid State Technology Association ("JEDEC") representative for Micron testified that in 1992, "I knew it was [Rambus's] business model to patent their technology, and that's how they would gain their revenues." (Williams, Tr. 857). Similarly, Martin Peisl of Infineon stated that he was aware of Rambus's business model in the early

1990's and expected Rambus to get patents to cover its technology. (Peisl, Tr. 4505).

143. According to Andreas Bechtelsheim, formerly of Sun Microsystems, Rambus made very clear to Sun that it intended to seek patent coverage for all of its inventions and developments, and Rambus explained to various companies, including Sun, that it was seeking patent coverage for its inventions because it intended to obtain revenue or earn revenue through licensing its technology to both memory manufacturers and system manufacturers. (Bechtelsheim, Tr. 5819).

G. Press Coverage: The March 1992 Microprocessor Report Article

144. In connection with the public announcement of Rambus's technology and its business plan in March 1992, Rambus provided information to the press regarding Rambus's inventions, and numerous articles about Rambus appeared. (RX 1446).

145. Many of these articles provided a significant amount of technical detail. For example, an article entitled "Rambus Unveils Revolutionary Memory Interface" in the March 4, 1992 Microprocessor Report describes Rambus's technology in some depth and described three of the four features of Rambus technology at issue here, as well as aspects of the fourth. (RX 1446 at 22-26).

146. The article states that the "Rambus Channel is a 500-Mbyte/s interface, operating with a 250-MHz clock and transferring a byte of data on each clock edge" and that a "phase-locked loop on each Rambus device limits clock skew within the chip." (RX 1446 at 22, 23).

147. The article also states that the "six-byte request packet encodes a 36-bit address, a 4-bit operation code, and 8-bit transfer

length count (in bytes). Byte addressing and block sizes of up to 256 bytes are supported." (RX 1446 at 24).

148. The article also notes that "control registers" on the DRAM can be used to specify certain parameters. (RX 1446 at 23).

H. Rambus's Disclosure of Inventions Through Public Documents

1. The 1992 Marketing Brochure

149. In early 1992, Rambus produced and distributed its first marketing brochure about Rambus technology. (RX 2183; Horowitz, Tr. 8547). The 1992 marketing brochure describes the four features of Rambus technology at issue here. (Horowitz, Tr. 8547-48).

150. The 1992 marketing brochure states that the "heart of [the Rambus] Interface is high performance PLL (phase-locked-loop) circuitry which provides the clocks for transmitting and receiving Rambus Channel data." (RX 2183 at 6).

151. The 1992 marketing brochure describes variable burst length, because data transfers could involve a variable amount of data, indicating: "[t]ransfers of 1 to 256 Bytes per Request." (RX 2183 at 7).

152. The 1992 marketing brochure describes dual-edge clocking, stating that "[d]ata effectively transferred on both edges of the clock." (RX 2183 at 9).

153. The 1992 marketing brochure describes programmable latency, stating that "the Read Data Packet is returned a time ReadDelay after the Request Packet" and that this delay value is "programmed into the configuration registers of all devices during system initialization." (RX 2183 at 11).

2. Publications Describing the First Rambus DRAM

154. The first Rambus DRAM was a 4.5 megabit Rambus DRAM produced by Toshiba in the 1991-92 time frame. (Horowitz, Tr. 8548-49).

155. A paper about the Toshiba 4.5 megabit Rambus DRAM was presented at the 1992 International Symposium on VLSI Circuits (VLSI Circuits Symposium) and published in the proceedings of that symposium. (RX 301 at 76-77; Horowitz, Tr. 8552-54).

156. The VLSI Circuits Symposium is held annually and is one of the top two conferences in the world for circuit designers. (Horowitz, Tr. 8552). The "technical program committees" of the Symposium read all the papers submitted and choose the better ones for publication at the conference. (Horowitz, Tr. 8552-53). The technical program committees for the 1992 VLSI Circuits Symposium that selected the paper about the Toshiba 4.5 megabit Rambus DRAM included representatives from IBM; Texas Instruments; Siemens AG; Sun Microsystems; Intel; Hitachi; Samsung; Matsushita; Mitsubishi; Fujitsu Laboratories, Ltd.; Sanyo Electric Co., Ltd.; Oki; and NEC. (RX 301 at 5).

157. The paper published in the proceedings of the 1992 VLSI Circuits Symposium about the Toshiba 4.5 megabit Rambus DRAM discusses the four features of Rambus technology at issue in this case. (Horowitz, Tr. 8554). Figure 2 of the paper shows a block size transfer and read latency. (RX 301 at 77; Horowitz, Tr. 8555). Figure 3 of the paper shows double data rate input receivers. (RX 301 at 77; Horowitz, Tr. 8555). The paper also states that "[t]o eliminate skew caused by the internal circuitry, the DRAM contains two PLLs." (RX 301 at 76; Horowitz, Tr. 8555).

158. At the end of the 1992 VLSI Circuits Symposium, the authors of the top papers were invited to provide a longer version to be published in the Journal of Solid State Circuits. (Horowitz, Tr. 8555-56). The Journal of Solid State Circuits is the most widely read journal for circuit designers. (Horowitz, Tr. 8555-56). The paper about the Toshiba 4.5 megabit Rambus DRAM was selected, and a longer version of that paper was published in the Journal of Solid State Circuits in April 1993. (RX 385; Horowitz, Tr. 8556).

I. Presentations of the Proprietary RDRAM Technology and Nondisclosure Agreements

159. Continuing for many years, Rambus pursued a strategy of actively promoting its proprietary RDRAM technology to companies that were in a position to manufacture memory chips or related chipsets. Rambus also promoted RDRAM to others, including systems companies. (*See* Crisp, Tr. 2931; CX 543A at 1, 3, 7-8).

160. Rambus's efforts to promote adoption of its proprietary RDRAM technology included making presentations concerning the proprietary RDRAM technology to memory chip manufacturers and other firms. (*E.g.* CX 2107 at 63 (Oh, Dep.); Bechtelsheim, Tr. 5818-19; Kellogg, Tr. 5052-53).

161. In connection with such efforts, Rambus commonly entered into nondisclosure agreements that prohibited the firms from disclosing information concerning the proprietary Rambus technology to others without the consent of Rambus. (Bechtelsheim, Tr. 5818-19; Rhoden, Tr. 521; Kellogg, Tr. 5052-53). Rambus's presentations often included a discussion of the patent protection Rambus was seeking for its inventions. (CX 2079 at 83 (Mooring, Dep.); CX 2111 at 314-15, 316-18, 319-20, 320-21, 322-24 (Tate, Dep.)).

162. In April 1992, Gordon Kelley of IBM attended a presentation by Rambus at IBM comparing the proprietary Rambus RDRAM technology with Synchronous Dynamic Random Access Memory ("SDRAM"). (G. Kelley, Tr. 2535).

163. Desi Rhoden was employed at Hewlett-Packard ("HP") when he began to learn about the Rambus technology in the early 90's. (Rhoden, Tr. 396). Rambus came to HP to give a presentation about its new memory that it was developing. (Rhoden, Tr. 396). The presentation was made pursuant to a nondisclosure agreement between Rambus and HP. (Rhoden, Tr. 521). Although Rambus did not say anything at that presentation about pending Rambus patent applications, Rhoden assumed that Rambus probably did have patent applications. (Rhoden, Tr. 521).

164. Andreas Bechtelsheim, a Vice-President for technology at Sun (Bechtelsheim, Tr. 5752), was involved in presentations and discussions with Rambus and understood that Rambus had patent rights that covered its proprietary RDRAM technology. (Bechtelsheim, Tr. 5828-29; 5841-42). Rambus "made clear [to Bechtelsheim] that they were going to protect any patent on their memory technology because that was their business model." (Bechtelsheim, Tr. 5829).

165. Mark Kellogg, an employee of IBM, learned about Rambus technology through a presentation by Rambus to IBM in the early 1990's. (Kellogg, Tr. 5017, 5052-53).

166. Terry Lee, an employee at Micron, learned about Rambus technology in part from a meeting with Rambus held in 1995. (Lee, Tr. 6601-02). Following the meeting, he and a colleague, Kevin Ryan, reviewed selected patent abstracts. (Lee, Tr. at 6607-08). Lee concluded that the patents appeared to apply specifically to the RDRAM bus structure. (Lee, Tr. at 6610-11). In March of 1997, Lee expressed concerns to the JEDEC JC 42.3 committee that a double data rate SDRAM ("DDR SDRAM")

presentation "looked like" one of the Rambus patents he had reviewed in 1995. (Lee, Tr. 6956-59).

J. The June 1992 Business Plan

167. By June 1992, Rambus CEO Geoffrey Tate transmitted to the Rambus Board of Directors a comprehensive five-year business plan, which, he explained, was based on "inputs from all of the executives." (CX 543A at 1). As reflected in the "Executive Summary" of this June 1992 Business Plan, Rambus's strategy was to:

> develop a breakthrough technology with high value added in a large percentage of computer, communications, and consumer digital systems products;
>
> establish strong intellectual property barriers; . . .
>
> to license the technology for integration onto high volume ICs of all major IC companies and to have license fees cover the costs of technology and market development;
>
> to establish Rambus as the new interface standard for systems requiring high performance at low cost; . . .
>
> to establish a very high profit stream of technology royalties; [and]
>
> to continually improve on Rambus Technology through minor and major enhancements . . . .

(CX 543A at 3).

K. Rambus Patent Applications

1. The '898 Patent Application

168. Rambus filed patent application serial no. 07/510,898 (the '898 application) in the United States Patent and Trademark Office ("PTO") on April 18, 1990. (CX 1451 at 1-2; Nusbaum, Tr. 1507). The '898 patent application included a descriptive portion, called the "specification," that was sixty-two pages long, and included fifteen original drawings. (CX 1451 at 3-63, 140-50). The '898 patent application contained one-hundred fifty claims. (CX 1451 at 64-125).

169. In connection with the prosecution of its '898 patent application, Rambus was issued a communication by the patent examiner at the PTO containing a restriction requirement. (Nusbaum, Tr. 1511).

170. A restriction requirement reflects that the examiner has reviewed the application and determined that the application contains claims describing multiple "independent and distinct inventions." The applicant is required to elect which of the claimed inventions it wishes to pursue in the application. (Nusbaum, Tr. 1510).

171. The restriction requirement received by Rambus was an eleven-way restriction requirement; Rambus responded by restricting its original application and filing ten divisional patent applications on March 5, 1992, all of which claimed priority based on the filing date of the original '898 application, April 18, 1990. (Nusbaum, Tr. 1511-12; First Set of Stipulations, Stip. 22).

172. Over time, Rambus filed numerous additional continuation and divisional patent applications claiming priority based on the filing date of the original '898 application. (*See* First Set of Stipulations, Stip. 22).

173. Prior to June 1996, Rambus filed a total of seventeen continuation and divisional patent applications claiming priority based on the filing date of the original ‘898 application, and had been issued six United States patents on such applications. (First Set of Stipulations, Stip. 22).

174. As of April 2003, Rambus had filed sixty-three continuation and divisional patent applications claiming priority based on the filing date of the original ‘898 application, of which ten were still pending. (First Set of Stipulations, Stip. 22).

175. As of April 2003, at least 43 United States patents had been issued to Rambus from continuation and divisional applications claiming priority to the original ‘898 application. (First Set of Stipulations, Stip. 13).

176. Over time, various of the Rambus continuation and divisional patent applications claiming priority to the ‘898 application embodied changes and amendments to the claims made in the original ‘898 application and came to describe aspects of the original invention. (*See, e.g.*, Crisp, Tr. 2927-28).

177. The patents that Rambus has asserted against DRAM manufacturers have all issued from applications that are continuations or divisionals stemming from the original ‘898 application and all share a specification with that original application. (First Set of Stipulations, Stip. 22; Nusbaum, Tr. 1513-14).

178. Pursuant to the “written description” requirement for a patent’s validity, the PTO determined that the claims of these patents were supported by the specification of the original ‘898 application. (Nusbaum, Tr. 1611-14).

2. The '703 Patent

179. Rambus's first United States patent, U.S. Patent No. 5,243,703 ("the '703 patent"), issued on September 7, 1993. (RX 425). Rambus disclosed the '703 patent to JEDEC during a committee meeting in September 1993. (First Set of Stipulations, Stip. 11). The '703 patent was subsequently added to the "patent tracking list" maintained by JEDEC, where it was described as involving a "Sync Clock." (JX 18 at 18).

180. The '703 patent can be traced back to a divisional application of the original '898 application. (RX 425 at 1; Fliesler, Tr. 8812).

181. The written description and drawings of the '703 patent, like all the issued patents that claim priority to the '898 application, are substantially the same as the written description and drawings in the '898 application. (RX 425 at 1; CX 1451 at 1; Fliesler, Tr. 8812, 8817). Thus, the '703 patent contains the same descriptions of technologies as in the '898 application and PCT application. (RX 425 at 7, 8, 9, 14-17, 21; Fliesler, Tr. 8819-20).

182. In addition to listing the original '898 application, the '703 patent's written description also contains a list of the nine other divisional applications stemming from the '898 application that were pending at the time. (RX 425 at 11; Fliesler, Tr. 8813-14).

3. The PCT Application

183. On April 16, 1991, Rambus filed an international patent application pursuant to the Patent Cooperation Treaty (the "PCT application"). (CX 1454 at 1).

184. The PCT application is identical in all material respects to the '898 application. In particular, the PCT application contains

the same written description, drawings, and claims as the ‘898 application. (CX 1451; CX 1454; Fliesler, Tr. 8811).

185. The PCT application was published and made publicly available as of October 31, 1991. (CX 1454 at 1; First Set of Stipulations, Stip. 8). Several JEDEC members obtained the PCT application in the early 1990’s, including Mitsubishi and IBM. (RX 379A at 1; RX 201 at 1).

4. The ‘898 and PCT Applications Describe Numerous Inventions

186. The ‘898 and PCT applications each contain a lengthy disclosure consisting of a sixty-two page written description, fifteen drawings, and one hundred and fifty claims. (CX 1451, CX 1454).

187. The written description of the ‘898 and PCT applications contain numerous headings and subheadings, such as “Device Address Mapping,” “Bus,” “Protocol and Bus Operation,” “Retry Format,” “Bus Arbitration,” “System Configuration/Reset,” “ECC,” “Low Power 3-D Packaging,” “Bus Electrical Description,” “Clocking,” “Device Interface,” “Electrical Interface - Input/Output Circuitry,” and “DRAM Column Access Modification.” (CX 1451 at 18, 20, 21, 30, 32, 37, 40, 43, 45, 47, 54; CX 1454 at 18, 20, 21, 30, 32, 37, 41, 44, 46, 48, 55).

188. Although the applications describe how an entire system is to be put together, they also describe numerous technical features that can be used independently of one another and of the system. (Fliesler, Tr. 8788-89).

189. The ‘898 and PCT applications note that, although a preferred implementation of the invention contains 8 bus data lines, “[p]ersons skilled in the art will recognize that 16 bus data lines or other numbers of bus data lines can be used to implement the teaching of this invention.” (CX 1451 at 10; CX 1454 at 10).

190. A person of ordinary skill in the art to which the '898 and PCT applications pertain would have an electrical engineering degree and at least two to three years of experience in designing computer memory circuits. (Fliesler, Tr. 8779-80; Nusbaum, Tr. 1613).

191. It was Dr. Horowitz's understanding when the patent application was filed that the various solutions to problems described in the application could be used independently of one another. Thus, if one did not want quite the level of performance that Drs. Farmwald and Horowitz envisioned, one could use only a subset of the techniques described in the patent application. (Horowitz, Tr. 8514-15).

192. Dr. Farmwald never thought of his ideas as implementing a "narrow" bus. (Farmwald, Tr. 8143). Rambus originally used a 9-bit wide bus because that corresponded to the number of pins that could fit on the edges of the chips that existed at the time; later Rambus used wider buses because more pins could be placed on the chip. (Farmwald, Tr. 8143-44). While some of the inventions of Drs. Farmwald and Horowitz might enable narrower busses to work better, the inventions are not specific to a particular bus width. (Farmwald, Tr. 8144).

193. A March 12, 1993 Mitsubishi memorandum begins by stating that a "need has arisen to evaluate in detail all of the claims in a patent being applied for by Rambus (1 patent, a total number of claims is 150)." (RX 2214A at 1). The memorandum goes on to list guidelines for this evaluation, including "1) Do not discuss Rambus interface. 2) Determine whether or not any other areas contain technologies that will be important in increasing memory speed in the future." (RX 2214A at 1).

194. A June 10, 1993 Mitsubishi document with the heading "RAMBUS Patent (summary of responses)" states: "[i]n addition to the technologies of narrower bus width and communication by

protocol that are described above, the RAMBUS patent includes a variety of requirements such as memory system configuration, packaging method, and device configuration, and it can be achieved through a combination of these factors." (RX 406 at 4). The document continues: "[t]he individual technologies that appear in the RAMBUS patent will be used independently in the future." (RX 406 at 4).

a. Description of Access Time Registers

195. The '898 application and the PCT application describe access time registers that store latency, that is the amount of time between receiving a request and driving data onto the bus in response to that request. (CX 1451 at 16, 23; CX 1454 at 16, 23; Jacob, Tr. 5481). The applications state that "each slave may have one or several access-time registers," where "slave" can refer to a DRAM. (CX 1451 at 16; CX 1454 at 16; Jacob, Tr. 5649).

196. In common use, programmable CAS latency in the mode register of an SDRAM is set at initialization. (Jacob, Tr. 5648-49). The '898 application and PCT application state with respect to the access time registers (and other registers): "[m]ost of these registers can be modified and preferably are set as part of an initialization sequence." (CX 1451 at 16; CX 1454 at 16).

197. A Mitsubishi document headed "Assessment of Rambus Patents (Second Half)" states next to the numbers 95, 97 and 103: "Modifiable Access Time Register (Similar to SDRAM latency control)." (RX 2213A at 25, 27). Claim 103 of the PCT application (and '898 application) refers to a "modifiable access-time register." (CX 1451 at 104; CX 1454 at 105).

198. In a claim-by-claim analysis of the PCT application produced by Mitsubishi, a marginal note identifies claim 103 of the application as relating to latency and SDRAM. (RX 2213A at 7, 9). The analysis further indicates that Mitsubishi determined that this claim relating to latency in SDRAMs was particularly

important, for Claim 103 was marked "A." (RX 2213A at 7, 9). A later page of the document explains that an "A" grade means that a technology is "important for increasing DRAM speed." (RX 2213A at 27).

b. Description of Block Size

199. The '898 application and the PCT application describe varying the "block size," that is the amount of data transmitted in response or received in response to a request. (CX 1451 at 29-30; CX 1454 at 29-30; Jacob, Tr. 5477-78). The applications each state that "BlockSize [0:3] specifies the size of the data block transfer." (CX 1451 at 29; CX 1454 at 29). The applications each contain a table showing the "Number of Bytes in Block" corresponding to the value in the "BlockSize" field. (CX 1451 at 30; CX 1454 at 30).

200. "Burst length," as the term is used in SDRAMs, refers to the amount of data to be transferred per read or write transaction. (Rhoden, Tr. 379-80; Jacob, Tr. 5396-97.) Likewise, "block size," encodes the amount of data to be transferred per read or write transaction. (Jacob, Tr. 5477). The two terms describe the same function and are used interchangably. (Horowitz, Tr. 8661-62; Geilhufe, Tr. 9643).

c. Description of Bus Clock

201. The '898 and PCT applications state: "[c]lock distribution problems can be further reduced by using a bus clock and device clock rate equal to the bus cycle data rate divided by two, that is, the bus clock period is twice the bus cycle period. Thus, a 500 MHz bus preferably uses a 250 MHz clock rate." (CX 1451 at 49; CX 1454 at 50). If clock rate is half the data rate on the bus, both edges of the clock must be used to transmit data. (Fliesler, Tr. 8801-02).

202. Figure 10 in the ‘898 and PCT applications shows two input receivers clocked by “clock” and “clock bar” as in the Rambus technical descriptions. (CX 1451 at 147; CX 1454 at 148; Fliesler, Tr. 8799). If “clock bar” is high when “clock” is low, and vice versa, data is input on both the rising and falling edges of clock. (Fliesler, Tr. 8799-800).

203. Figure 13 in the ‘898 and PCT applications shows a timing diagram with data being input, as indicated by the arrows along the bottom of the figure, on both the rising and falling edges of the clock. (CX 1451 at 149; CX 1454 at 150). Howard Sussman, the JEDEC representative for Sanyo and formerly the JEDEC representative of NEC, testified that Figure 13 of the PCT application shows to him that “input being sampled on the high and low edge of the clock” and that is “double data rate input.” (Sussman, Tr. 1322, 1467-68).

d. Description of Variable Delay Circuitry With a Feedback Loop

204. Figure 12 of the ‘898 and PCT applications describes variable delay circuitry and a feedback loop. (CX 1451 at 148; CX 1454 at 149; Jacob, Tr. 5649-50).

205. When Joel Karp, then of Samsung, reviewed Rambus’s PCT application in 1991, Figure 12 “jumped out” at him as evidencing a DLL. (CX 2078 at 119 (Karp Micron Dep.); CX 2114 at 276-77 (Karp Dep.)).

206. In its license negotiations with Rambus in 1994, Joel Karp felt that Samsung was motivated to seek a non-assertion provision for non-Rambus-compatible uses of Rambus’s inventions because of the on-chip DLL shown in Rambus’s PCT application. (CX 2078 at 107-08, 119-20 (Karp, Micron Dep.)).

5. Review of the '898 or PCT Application Should Have Raised Concerns That Rambus Might Be Able to Obtain Claims Over the Four Technologies at Issue

207. A person of ordinary skill in the art or a patent lawyer reviewing the '898 application or PCT application would have realized that Rambus might have claims broad enough to cover programmable CAS latency, programmable burst length, dual-edge clocking, and on-chip DLL. (Fliesler, Tr. 8784-85, 8810-11).

208. An experienced DRAM designer reviewing the PCT application would reach the conclusion that there is considerable similarity in form and function between programmable latency, variable burst length, dual-edge clocking, and on-chip DLL as described in the PCT application and the corresponding features in SDRAMs or DDR SDRAMs. (Geilhufe, Tr. 9556-57).

209. If an experienced DRAM designer working on designing an SDRAM incorporating programmable latency and burst length in the early 1990's had reviewed the PCT application, he likely would have become concerned that Rambus might have claims to those features and would have raised the issue with management. (Geilhufe, Tr. 9558).

210. A manager faced with this issue, in light of the potential for substantial economic consequences if a DRAM design infringes a patent, would likely have gathered additional technical analysis from specialists and, if there remained a concern, would have taken the issue to corporate counsel for a careful review. (Geilhufe, Tr. 9558-59).

211. When Mitsubishi reviewed the PCT application, it undertook an in-depth study. A March 3, 1993 Mitsubishi memorandum requests cooperation on evaluating Rambus's PCT patent application because they "realized that the technology is

related not only to stand-alone semiconductor devices but also to systems." (RX 379A at 1).

212. A June 10, 1993 Mitsubishi document stressed the need for expert analysis of Rambus's patent application to determine the scope of the claims, particularly as to individual technologies disclosed in the patent application: "[t]here is a need to examine the specifications of the patent claims to determine whether individual technologies used independently will infringe on the RAMBUS patent, and for that we will have to obtain the views and interpretations of experts." (RX 406 at 4; *see also* RX 416A at 1).

213. An August 16, 1993 Mitsubishi document again raised the issue of whether Rambus could have claims on features separate from any particular bus architecture. (RX 419A at 1).

214. A January 11, 1996 memorandum indicates that Mitsubishi subsequently conducted an "investigation of the US patents owned by Rambus" that were granted by the end of October 1995 and that eighteen patents met that criteria. (RX 528A at 1).

215. Mitsubishi also maintained a chart tracking all of Rambus's issued U.S. patents. For example, one version of this chart begins with Rambus's first issued U.S. Patent No. 5,243,703, at number one and concludes with U.S. Patent No. 5,578,940 which issued on November 26, 1996 at number twenty-seven. (RX 2216 at 2, 4). Rambus's '327 patent is listed at number twenty-three on the chart. (RX 2216 at 3).

216. A later version of the Mitsubishi chart contains thirty-seven Rambus patents and includes patents that issued in early 1998. (RX 2218 at 3-6).

217. A Mitsubishi analysis of the claims of the PCT application specifically calls out the modifiable access time

register and notes its similarity to SDRAM latency control. (RX 2213A at 27).

218. An August 24, 1996 report on a Rambus meeting states: "Rambus' patents. Issued: 16, filed: 80. For example, data is transferred at both edges." (RX 756A at 1).

219. As Complaint Counsel concede, Rambus has obtained patent claims that cover programmable CAS latency, variable burst length, dual-edge clocking, and on-chip DLL as those features are used in SDRAMs and/or DDR SDRAMs. (Complaint, ¶ 91). Rambus has asserted claims covering these four features against SDRAMs and DDR SDRAMs. (Complaint, ¶ 92).

III. JEDEC IS A COLLABORATIVE STANDARD SETTING BODY FOR THE SEMICONDUCTOR INDUSTRY

A. Early History of JEDEC

220. JEDEC was founded in 1958 and originally named the "Joint Electron Device Engineering Council." (CX 302 at 10; J. Kelly, Tr. 1773-74 ("JEDEC has been active within an EIA organization under the name JEDEC since approximately 1958, and under other names with slightly different functions for a number of years prior to that, probably dating back to the 1940s.")).

221. The current name of JEDEC is the "JEDEC Solid State Technology Association." (J. Kelly, Tr. 1750-51).

222. Between 1991 and 1996, JEDEC was an activity within the Electronic Industries Association ("EIA") Solid State Products Division, which was itself a division of the EIA's Components Group. (CX 3092 at 14, 27; J. Kelly, Tr. 2075).

223. EIA is a "broad-based association that represents the electronics industry in the United States, and it engages in a

variety of different activities in support of that industry." (J. Kelly, Tr. 1750; CX 302 at 28).

224. In 1998, EIA changed its name to the Electronic Industries Alliance and JEDEC became a separate division of EIA. (CX 302 at 11). In 1999, JEDEC became independently incorporated. (CX 302 at 11).

225. Both EIA and JEDEC are headquartered in Arlington, Virginia. (J. Kelly, Tr. 1751).

B. The Purpose and Function of JEDEC

226. JEDEC seeks to create consensus based standards which reflect the interests of DRAM manufacturers and exists because of an industry need for standardization. (CX 2767 at 1; J. Kelly, Tr. 1784; Landgraf, Tr. 1685).

C. The Organization of JEDEC

1. Member Companies

227. A company becomes a member of both JEDEC and EIA by completing and submitting an application and paying dues. (CX 601; J. Kelly, Tr. 1801-02; Rhoden, Tr. 294-95). "Eligible organizations can become members of JEDEC by joining the EIA Solid State Products Division or by joining JEDEC directly," and paying annual dues. (CX 208 at 7).

228. During the time Rambus was a JEDEC member, dues were paid to EIA. (CX 602 at 6, 7).

229. There was no contractual relationship between JEDEC and Rambus. (J. Kelly, Tr. 2075).

230. During the 1990's, JEDEC had approximately two hundred fifty member companies who sent approximately 1800

individuals to participate in approximately fifty committees. (J. Kelly, Tr. 1774-75).

231. In 1992, when Rambus joined JEDEC, the membership application stated that: "JEDEC Committee membership is limited to companies and independent entities of companies that (1) manufacture solid state products, or provide related services or equipment, and (2) participate in the United States market." (CX 602 at 2).

232. JEDEC's membership includes companies from around the world. (Rhoden, Tr. 294 (noting companies from Korea, Germany, Taiwan and Japan); *see* CX 302 at 8).

233. Membership entitles companies to attend meetings, receive minutes, vote, and receive copies of standards and other publications. (J. Kelly, Tr. 1805-06).

234. Companies not interested in the outcome of a particular issue were encouraged to abstain from voting. (Rhoden, Tr. 303-04).

235. During the early and mid-1990's, JEDEC minutes were regularly circulated to all members. (Crisp, Tr. 3139). The minutes were also available in the early 1990's to non-members, with the possible exception of a Russian company. (G. Kelley, Tr. 2622-23).

236. JEDEC manual 21-H gives committee chairs discretion to allow guests to attend meetings: "[a]ll JEDEC Committee meetings are open to members, their designated alternatives, and guests invited by the Committee. Others may attend meetings only with prior approval of the Chairman." (RX 1211 at 10).

2. The JEDEC Council, Board of Directors and Officers

237. Today, the JEDEC Board of Directors is the governing body of JEDEC. (J. Kelly, Tr. 1768; CX 214 at 1, 14). Prior to 1999, the JEDEC Council was the governing body of JEDEC. (J. Kelly, Tr. 1768).

238. Prior to 1998, the JEDEC Council could not unilaterally set or change policies without approval of the EIA Engineering Department Executive Council ("EDEC"). (*See* J. Kelly, Tr. 2078, 2105).

239. The chairman of the board of directors is elected by JEDEC members. (Rhoden, Tr. 286).

240. The JEDEC chairman is responsible for "the business aspect of JEDEC, trying to make sure that we [JEDEC] have office space, staff, relationships with other organizations, and to make sure that we take care of the business aspects of the corporation itself." (Rhoden, Tr. 286-87).

241. Desi Rhoden is the current Chairman of the JEDEC Board of Directors. (Rhoden, Tr. 283).

242. John Kelly is the current President of JEDEC. (J. Kelly, Tr. 1750-51).

243. John Kelly has also been the General Counsel of EIA since 1990. (J. Kelly, Tr. 1754).

244. The EIA General Counsel is "the legal counsel for all of the operating units within EIA, including JEDEC." (J. Kelly, Tr. 1754). The EIA General Counsel is the person responsible for interpreting EIA rules and the JEDEC rules, including the JEDEC patent policy. (J. Kelly, Tr. 1939; Sussman, Tr. 1348-49).

245. While the General Counsel may interpret the policies and rules, EDEC establishes what the policies and rules are. (J. Kelly, Tr. 2078).

246. Today, JEDEC employs a staff of ten persons to facilitate the meetings of JEDEC committees. (J. Kelly, Tr. 1792-93). During the early to mid-1990's, the size of JEDEC's staff was considerably smaller than the current size. (J. Kelly, Tr. 1795).

3. The JC 42 Committee

247. JEDEC is organized into committees and subcommittees. (Landgraf, Tr. 1687).

248. The members of each committee or subcommittee elect a chairman. (J. Kelly, Tr. 1794).

249. The JC 42 committee is concerned with developing standards for memory products. The JC 42 membership consists of "[a]lmost all of the DRAM memory companies, SRAM memory companies, logic companies, customers of memory, as well as interconnect companies, such as socket manufacturers," and testing companies. (Williams, Tr. 765-66; Rhoden, Tr. 288).

250. The JC 42 Chairman is responsible for coordinating all the activities in the JC 42 committee and subcommittees, including the scheduling of meetings. (Rhoden, Tr. 288).

251. The JC 42 committee had several subcommittees focusing on particular specialized subject matters. (J. Kelly, Tr. 1769; Rhoden, Tr. 285 (JC 42 included subcommittees devoted to DRAM (42.3), SRAM (42.2), memory modules (42.5), flash memory and other types of programmable devices)).

252. JEDEC's JC 42.3 subcommittee develops standards relating to DRAM products. (Peisl, Tr. 4381; Rhoden, Tr. 283-84).

253. In late 1991, approximately forty to fifty companies were represented on the JC 42.3 subcommittee. (Rhoden, Tr. 340-41; JX 10 at 1-2).

254. The JC 42 committee and its related subcommittees typically meet between four and eight times per year. (Rhoden, Tr. 340).

255. Minutes of JC 42 committee and its subcommittees are prepared by Ken McGhee, a staff person. (Rhoden, Tr. 327). There is a review process that goes on before the minutes are made official and distributed to members. (Rhoden, Tr. 591).

256. The minutes of JC 42 and its subcommittees record the key decisions that are made during the standard development process, including motions and votes. (Rhoden, Tr. 327-28). The minutes were intended to be a chronological statement of the events and occurrences in the meeting, although they were not a transcript. (Rhoden, Tr. 590-91).

D. The Standard Development Process

257. The standard development process begins with discussions among the participants at a JEDEC meeting concerning subjects that members may feel should be considered as possible standards. (Rhoden, Tr. 406-07).

258. JEDEC entertains a number of proposals by members when working toward a standard for a new device. (Rhoden, Tr. 415).

259. JEDEC members decide which of these ideas to pursue. (Rhoden, Tr. 415-416).

260. There is a first showing or first presentation when proposals typically receive an item number. (Calvin, Tr. 1025).

261. In some cases, discussions of possible features generate a survey ballot that requests the members to give their views concerning different solutions. (Rhoden, Tr. 481, 516).

262. Following the conclusion of the second or subsequent presentations, the committee decides if it wants to create a ballot to vote on the substance of a proposed standard. (Rhoden, Tr. 406-07).

263. JEDEC participants often had significant differences of opinion concerning the development of a standard. These differences of opinion drove heated debates concerning the merits of the various solutions to the technical challenges facing the JEDEC participants. (*E.g.*, CX 711 at 14; CX 711 at 33; CX 711 at 47; CX 680 at 1; CX 680 at 2; Rhoden, Tr. 434-35 ("if you give ten engineers a problem, you'll probably get 12 or 14 solutions, and the same is true inside the discussions inside the committee")).

264. From time to time, ballots failed or were put on hold in the JEDEC committees because the committees did not reach a consensus. (JX 12 at 6, 12; JX 19 at 10; JX 26 at 5).

265. If it preferred, a committee could pass items individually but place the individual items on hold until an entire list of related items that were needed to define a single standard was complete, and once that group of ballots was complete and passed, then together the committee could motion them to go to Council for publication. (G. Kelley, Tr. 2554).

266. After a JEDEC committee approves a standard, the proposed standard is sent by a ballot to the JEDEC board of directors, which then has to again by a consensus approve the ballot in order for the proposal to become a JEDEC standard. (J. Kelly, Tr. 1785; Rhoden, Tr. 406-07).

267. JEDEC's consensus based process means that the board of directors will consider any committee votes that were cast in opposition to the proposed standard. (J. Kelly, Tr. 1786).

268. JEDEC's consensus based process often requires years in order to adopt a new standard or change an existing standard. (Polzin, Tr. 3977; Peisl, Tr. 4453 ("JEDEC is traditionally a very slowly moving consortium, and there's a reason for that, because there's so many companies involved, it's basically the whole industry that produces parts for the PC and the laptop and the server business, so to try to reach consensus at JEDEC, based on my experience, have been incredibly hard and tough. In the last decade, essentially there were only two standards that emerged for SDR and DDR.")).

269. In order to create common parts that are plug compatible during the 1990's, JEDEC standards became more detailed. (CX 35 at 14-15; G. Kelley, Tr. 2390).

270. Formal standardization in the DRAM industry benefits the entire industry. (Prince, Tr. 9016-17).

271. JEDEC standards are very valuable to manufacturers. (CX 707 at 1 ("JEDEC is a big deal to them [Samsung] because it [JEDEC] represents the big users."); Peisl, Tr. 4383-84; Bechtelsheim, Tr. 5790).

E. Rambus's Involvement in JEDEC

1. Rambus's Participation in JEDEC

272. The first Rambus employee to attend a JEDEC meeting on behalf of the company was William Garrett, who first attended a meeting in early December 1991 at the invitation of Toshiba. (CX 670 at 1). Garrett was later replaced as the Rambus primary representative at the JC 42.3 Committee by Richard Crisp, who then became Rambus's representative at JEDEC. (Crisp, Tr. 2929).

273. In February 1994 Rambus renewed its JEDEC membership for the 1994 calendar year and in April 1995 Rambus paid its dues to renew its JEDEC membership for the 1995 calendar year. (CX 602 at 6-7).

274. The final JEDEC meeting attended by Rambus was the meeting in December 1995. (CX 2104 at 853-54 (Crisp, Micron Dep.)). Rambus did not renew its membership for 1996. (CX 887).

2. Rambus Representatives Learn [*103] About the EIA/JEDEC Patent Policy

275. Jim Townsend, JC 42 Chairman and IBM representative, made a presentation concerning the patent policy and showed the patent tracking list at most JEDEC meetings attended by Crisp. (JX 12 at 5, 28-29; JX 13 at 4; CX 42A at 2; JX 15 at 4; JX 16 at 5; JX 17 at 3; JX 18 at 3, 15-18; JX 19 at 4; JX 20 at 4, 15-18; JX 21 at 4, 14-18; JX 22 at 3, 12-16; JX 25 at 3, 18-26; CX 88A at 2; JX 27 at 4, 20-25).

276. At the May 1992 JEDEC meeting, Chairman Townsend showed a copy of the new American National Standards Institute ("ANSI") patent policy implementation guide and secretary Ken McGhee spoke concerning the EIA patent policies. (CX 34 at 3, 10-11; CX 34A at 2, 7).

277. At the September 1993 JEDEC meeting, Townsend showed a draft of portions of the revised JEP 21-I Manual. (JX 17 at 12; *see also* CX 2092 at 63-64 (Crisp, Infineon Trial Tr.)). The draft stated only that "the committee Chairperson must have received written notice from the patent holder" that the license would be made available on a reasonable and nondiscriminatory basis. (JX 17 at 12). The draft did not impose an obligation to disclose intellectual property and did not advise the Chairperson to call attention to such an obligation. (JX 17 at 12).

3. Rambus Continued to Stay Abreast of JEDEC and SyncLink Activities

278. The minutes of JC 42.3 meetings are publicly available. (G. Kelley, Tr. 2623).

279. Several sources provided information to Rambus about JEDEC meetings after Rambus withdrew from JEDEC. (Crisp, Tr. 3413).

280. In 1997, Richard Crisp, Rambus's principal JEDEC representative, received information about JEDEC's activities from a source called "deep throat." (Crisp, Tr. 3414; CX 929 at 1; CX 932 at 1 (Crisp June 1997 email: "My 'deep throat' (DT) source told me that the DDR bandwagon is moving fast within JEDEC with all companies participating.")).

281. Crisp also received unsolicited information relating to proceedings at JEDEC from an anonymous source called "Mixmaster," a reporter Crisp called the "Carroll contact," and a source known as "Secret Squirrel." (Crisp, Tr. 3414-17; CX 935 at 1).

282. Crisp shared JEDEC-related information he received from Deep Throat, the Carroll Contact, Mixmaster, and other sources with Rambus executives and engineers. (Crisp, Tr. 3413-17; CX 935 at 1; CX 929 at 1; CX 973 at 1; CX 979 at 1; CX 1014 at 1).

283. After June 1996, Rambus continued to follow SyncLink's activities. (Crisp, Tr. 3388-89; Crisp, Tr. 3395-96; CX 711 at 183).

IV. EARLY DEVELOPMENT AND ADOPTION OF JEDEC DRAM STANDARDS

A. The Initial SDRAM Standard

1. Demand for a New Generation of Memory

284. "Asynchronous DRAM" is a term that is used to describe DRAMs that are driven off the row address strobe ("RAS") and column address strobe ("CAS") signals where the RAS and CAS actually control the operation of the DRAM rather than a clock. (Jacob, Tr. 5394).

285. Page mode and extended data out ("EDO" DRAMs) are types of asynchronous DRAM. (Sussman, Tr. 1469; Polzin, Tr. 4031). In the late 1980's page mode and EDO DRAMs were commonly used in the industry. (Sussman, Tr. 1361). Page mode and EDO DRAMs were standardized at JEDEC. (Sussman, Tr. 1362; Prince, Tr. 9020-21).

286. In order to respond to the rising demand for performance and to ensure that the new JEDEC standard would result in common parts that were plug compatible, the JC 42.3 subcommittee began to standardize certain aspects of DRAM performance and design relationships. (CX 35 at 14; G. Kelley, Tr. 2388-91). Prior to that time, JC 42.3 work had generally focused on standardizing the location of pins, also known as pin-out diagrams. (G. Kelley, Tr. 2388).

287. The JC 42.3 subcommittee subsequently exceeded those boundaries and began standardizing certain technologies that are unrelated to interoperability. An on-chip DLL, for example, as included in the DDR SDRAM standard is not required for interoperability. Rather, as Complaint Counsel's technical expert, Professor Jacob, explained, the DLL used in DDR SDRAMs is transparent to the DRAM interface. (Jacob, Tr. 5617-18).

288. A new generation of memory was needed because the industry anticipated that microprocessor and computer speeds would increase and the industry demanded memory that could operate at the same speeds. (CX 2088 at 291-92 (Meyer, Infineon Trial Tr.)).

289. One option considered by the JC 42.3 subcommittee was to continue to develop a new generation of EDO DRAMs. (CX 711 at 1).

290. Subsequently, "Burst EDO" was also developed and standardized at JEDEC in mid-1995. (Williams, Tr. 873, 879-80; RX 585 at 1).

291. Burst EDO failed in the marketplace in competition with SDRAM. (Williams, Tr. 829). As Dr. Oh of Hyundai Electronics Industries Co., Ltd. ("Hyundai") testified regarding [*107] Burst EDO: "this is enhanced version of EDO, and we wanted to convince our customers the advantages of this part, but was not accepted by our customers." (CX 2108 at 236 (Oh Dep.)).

292. JEDEC also began to consider a DRAM that had been developed by IBM called "High Speed Toggle." (G. Kelley, Tr. 2584-85). High speed toggle is also known as "HST." (G. Kelley, Tr. 2441).

293. According to the definition provided by Complaint Counsel's expert, HST was an asynchronous part. Professor Jacob testified that an asynchronous DRAM is one where asynchronous RAS and CAS signals control the operation of the DRAM rather than a clock. (Jacob, Tr. 5394). Since RAS and CAS were *asynchronous* in HST, it follows from Professor Jacob's definition that HST was asynchronous. (Rhoden, Tr. 568; Kellogg, Tr. 5173). Indeed, a January 1992 document written by Willi Meyer of Siemens states: "IBM presented generic high speed toggle mode in Sep '90 which was asynchronous." (CX 2431 at 1; Kellogg, Tr. 5173).

294. In HST, IBM proposed to transfer data on both edges of the toggle signal. (Kellogg, Tr. 5173; Sussman, Tr. 1381; Rhoden, Tr. 436-37; CX 2080 at 242 (Karp, Micron Dep.)). While some witnesses loosely referred to this toggle signal as a "clock," it was not a free running clock like the system clock in a synchronous memory such as SDRAM or DDR SDRAM. (Rhoden, Tr. 437; Sussman, Tr. 1471).

295. IBM and Siemens made HST presentations at JEDEC during 1990 and 1991 which were included in survey ballots. (JX 2 at 92; JX 3 at 56-57; JX 3 at 7; CX 316 at 1; CX 314).

296. At the May 9, 1991 JC 42.3 meeting, the subcommittee passed a motion to ballot the IBM HST presentation. (JX 5 at 12). At the same meeting Siemens also made a HST presentation that was like the IBM HST except it used a G/pin instead of a new toggle pin. (JX 5 at 12).

2. Proposal of a Fully Synchronous DRAM

297. At the JEDEC JC 42.3 meeting in May 1991, Howard Sussman of NEC proposed a fully synchronous DRAM to JEDEC for the first time. (Sussman, Tr. 1364; CX 2088 at 272-75 (Meyer, Infineon Trial Tr.)).

298. It is unclear whether Sussman proposed during his initial proposal to use a single edge clock to input and output data and a programmable mode register to set CAS latency and burst length. (Sussman, Tr. 1365-67 and 1373-75). There was no documentation about the NEC proposal attached to the May 1991 minutes. (*See* JX 5).

299. In 1991, Sussman held an unofficial meeting of JEDEC members in Boxborough, Massachusetts to discuss his synchronous DRAM proposal. (Sussman, Tr. 1369-70; CX 20). A report about that meeting prepared by Sussman was intended to provide "a consensus of where we were." (Sussman, Tr. 1370).

The description of the features of Sussman's synchronous DRAM proposal does not include any mention of a mode register, programmable CAS latency, or programmable burst length. (CX 20 at 1). A report about the Boxborough meeting prepared by Gordon Kelley of IBM makes clear that Sussman was proposing a *fixed* CAS latency at this time. (RX 173 at 3). Kelley's list of the main features of the NEC proposal makes no mention of a mode register or programmable burst length. (*See* RX 173 at 3).

300. At the JC 42.3 meeting on September 18, 1991, the subcommittee voted in favor of the IBM HST technology. There were four no votes and a number of comments. (JX 7 at 8). NEC and Samsung commented that the use of a separate toggle signal can limit speed. (JX 7 at 8). The subcommittee decided to put the ballot on hold until more resolution to the comments could be made. (JX 7 at 9).

301. Also at the JC 42.3 meeting on September 18, 1991, Sussman made a second presentation of NEC's SDRAM proposal. (JX 7 at 13 and 160-62; CX 2088 at 276 (Meyer, Infineon Trial Tr.)).

302. A number of other companies also presented synchronous DRAM proposals at this meeting, including Texas Instruments, Toshiba, and Hewlett-Packard. (JX 7 at 13, 163-77).

303. At the September 1991 JEDEC meeting, NEC's second showing of the synchronous DRAM proposal does not mention a mode register, programmable CAS latency, or programmable burst length. (JX 7 at 160-62).

304. It was not until October 1991, at a second unofficial meeting of JEDEC members in Portland, Oregon, that Sussman's presentation materials indicated that latency and burst length should be programmable. Both programmable CAS latency and programmable burst length are included in a list of key features of the proposed device. (JX 10 at 50; Sussman, Tr. 1373-75). A

timing diagram, a version of which had been used by Sussman at the August 1991 non-JEDEC meeting as well as the September 1991 JEDEC meeting, had the following language *added* to the right-hand column when it was used at the non-JEDEC meeting in October 1991: "Latency is programmable." (*Compare* JX 10 at 51 *with* CX 20 at 3 and *with* JX 7 at 160).

305. Toshiba also made a presentation for a synchronous DRAM including programmable CAS latency (JX 10 at 67), causing Howard Kalter of IBM to remark that "programmable latency was the cleverest item Toshiba ever created." (RX 199 at 2). By this time, Toshiba was a Rambus licensee and was working on the design of the first RDRAM chip. (Horowitz, Tr. 8548-49).

306. At the JEDEC JC 42.3 meeting on December 4-5, 1991 (the first JEDEC meeting attended by Rambus), Mark Kellogg of IBM made a presentation comparing HST to synchronous DRAMs. (JX 10 at 5 and 84; Kellogg, Tr. 5172-73).

307. Also at the JC 42.3 meeting of December 4-5, 1991, Howard Sussman presented the results of a non-JEDEC meeting that had been held in Portland, Oregon on October 24, 1991 to discuss high bandwidth DRAM. (JX 10 at 4; Sussman, Tr. 1373). The conclusion from that meeting was that a fully synchronous DRAM with all signals referenced to a single positive clock edge would best meet system requirements. (JX 10 at 50).

308. At the JC 42.3 meeting held on February 27-28, 1992, NEC, Hitachi, Fujitsu, Toshiba, Mitsubishi and Sun all made presentations regarding synchronous DRAM devices. (JX 12 at 39, 42, 60, 69, 76, 94, 110).

309. These companies continued to also make presentations regarding asynchronous DRAMs that they proposed to develop as well. For example, at the February 1992 JC 42.3 meeting, Toshiba made two presentations regarding "address compression" for asynchronous DRAMs, Fujitsu made a presentation regarding an asynchronous DRAM in a new kind of packaging, and NEC made

a presentation regarding an asynchronous DRAM with a "revolutionary pinout." (JX 12 at 11).

310. No further action on HST was taken at the February 1992 JC 42.3 meeting. High Speed Toggle items continued to be listed, however, on an active items list presented at the February 1992 meeting by the Subcommittee Chairman. (JX 12 at 19; JX 12 at 20).

311. At a DRAM Task Group meeting on April 9-10, 1992, NEC, Fujitsu, Toshiba, Samsung, Hitachi and Mitsubishi presented proposals for a fully synchronous DRAM. (CX 34 at 30, 33-36).

312. At the April 1992 DRAM Task Group meeting, IBM proposed a slightly modified version of its HST technology. (CX 34 at 32; Kellogg, Tr. 5175).

313. Following the April 1992 DRAM Task Group meeting, the JC 42.3 subcommittee decided to pursue a fully synchronous DRAM rather than IBM's toggle mode. (G. Kelley, Tr. 2515). The JC 42.3 subcommittee also continued to develop various asynchronous DRAMs while it was standardizing synchronous DRAMs.

314. By the time Rambus attended its first JEDEC meeting in December 1991, Howard Sussman was reporting the consensus that a "fully synchronous DRAM with all signals referenced to a single (positive) clock edge would best meet system requirements." (JX 10 at 50).

315. The only evidence of consideration of dual-edge clocking that Complaint Counsel presented after this time is HST which actually proposed an asynchronous DRAM with output data on both edges of a "toggle signal." (*See* CX 2431 at 1; Kellogg, Tr. 5173).

3. Inclusion of Programmable CAS Latency and Burst Length

316. At the JC 42.3 meeting of December 4-5, 1991, NEC presented the results of a separate meeting in Portland, concluding that the latency of data to the clock and the burst length should be programmable. (JX 10 at 50).

317. At the same meeting, Texas Instruments made a revised presentation of its SDRAM proposal that also included programmable CAS latency and programmable burst length. (JX 10 at 4, 56; Rhoden, Tr. 419-20).

318. Toshiba made a second showing that included programmable CAS latency and burst length. (JX 10 at 67; Rhoden, Tr. 424). Wrap length and burst length are the same thing. (Rhoden, Tr. 419-20; Williams, Tr. 812-13; Sussman, Tr. 1374-75). Neither of the "first showings" at the September 1991 meeting included programmable CAS latency and programmable burst length. (*See* JX 7 at 163-77).

319. The JC 42.3 Subcommittee considered a number of alternative methods of determining the CAS latency and burst length, including using a fixed burst length, using pins to set the CAS latency and burst length, and using fuses to set CAS latency and burst length. (Rhoden, Tr. 425-34; Kellogg, Tr. 5099-102 and 5130-31). The alternative methods considered at JEDEC were rejected. Complaint Counsel did not present sufficient evidence to find that they ever made it past the "first showing" stage. (*See* JX 10 at 5, 64, 71; Rhoden, Tr. 425-34; Kellogg, Tr. 5099-102).

320. At the December 1991 JC 42.3 meeting, Samsung presented a proposal for SDRAMs that included fixed CAS latency and burst length. Samsung proposed using a single CAS latency of 2 and a single burst length of 8. (JX 10 at 71; Rhoden, Tr. 425-28; Kellogg, Tr. 5099-101). The Samsung proposal also

included a fuse option to select between two different burst options. (JX 10 at 71; Rhoden, Tr. 427-28).

321. At the December 1991 JC 42.3 meeting, Mitsubishi presented a proposal for an SDRAM that would use two pins, BT and WP, to set the burst length and burst type. (JX 10 at 74; Kellogg, Tr. 5102). In its proposal, Mitsubishi provided for two burst length options, a burst length of 4 and 8. (JX 1 at 74; Rhoden, Tr. 430-34). The Mitsubishi presentation was designated as a "first time presentation." (JX 10 at 5).

322. At the December 1991 JC 42.3 meeting, Texas Instruments presented a proposal using the WCBR cycle to program the mode register to determine burst length and CAS latency. (JX 10 at 50, 56).

323. WCBR indicates a situation where the write signal is low and a CAS signal is sent before the RAS signal. While common in a test or refresh operation, CAS before RAS differs from a normal read or write operation where the RAS would be sent before the CAS. (Kellogg, Tr. 5107-09).

324. At the JC 42.3 meeting of February 27-28, 1992, NEC, Hitachi, Fujitsu, Toshiba and Mitsubishi all made SDRAM proposals that included programmable CAS latency and burst length. (JX 12 at 39, 42, 60, 69, 76, 91, 94; Sussman, Tr. 1382-83). At the same meeting, Sun presented comments on what features it would like to see included in SDRAMs, including programmable CAS latency and burst length. (JX 12 at 110).

325. At a DRAM Task Group meeting of April 9-10, 1992, NEC, Fujitsu, Toshiba, Samsung, Hitachi, Mitsubishi and IBM presented proposals that included programmable burst length. (CX 34 at 30, 32-35).

326. At the next meeting of JC 42.3 on May 7, 1992, the minutes of the April DRAM Task Group's meeting were presented to the full JC 42.3 subcommittee. (CX 34 at 4 and 30-37).

327. At the May 1992 meeting of the JC 42.3 Subcommittee, Samsung, NEC, Toshiba, Hitachi and Mitsubishi all made SDRAM presentations that included programmable CAS latency and burst length. (CX 34 at 44, 63, 83, 85, 99, 108, 140).

328. At the May 1992 JC 42.3 meeting, Cray Corporation ("Cray") gave a presentation that proposed the use of fuses to select between a set of features for a single bank configuration and a set of featurers for a dual bank configuration, where the feature set included, *inter alia*, the CAS latency value and burst length value. The Cray presentation was not identified as a first showing in the minutes (*see* CX 34 at 3-12), and there is no evidence that it ever progressed to a first showing. (*See* Sussman, Tr. 1388; Kellogg, Tr. 5103-05).

329. On June 11, 1992, four SDRAM ballots were sent out to all members. (CX 252A at 1). One ballot sought approval for use of a particular implementation of a mode register which was used to program CAS latency and burst length, as well as other features. (CX 252A at 1, 3; Crisp, Tr. 3075-76; Rhoden, Tr. 448; Williams, Tr. 811-12).

330. Richard Crisp was present at the July 1992 JC 42.3 meeting and participated for Rambus in the discussion and the vote on the proposals, including the mode register proposal. (JX 13 at 1, 9-10). David Mooring of Rambus also was present. (JX 13 at 2). Rambus voted "no" to the proposals. (JX 13 at 9-10; CX 2112 at 78-79 (Mooring, Dep.)). Rambus's comments cited technical reasons for voting against it. (JX 13 at 9-11). These were the only votes cast by Rambus for or against any JEDEC proposals.

331. The results of the vote on the mode register ballot were presented at the next JC 42.3 meeting on July 21, 1992. (JX 13 at 9-12; Sussman, Tr. 1393). The initial tally showed fourteen members in support of the proposal, five against and seven abstentions. (JX 13 at 10). Various subcommittee members offered comments, especially with respect to the need for a CAS latency of 4. (JX 13 at 10-11). Finally, it was agreed to re-ballot the mode register proposal with an optional latency mode of 4. (JX 13 at 11).

332. At the September 16-17, 1992 JC 42.3 meeting, Sun made an SDRAM presentation that included programmable CAS latency and burst length. (CX 42 at 39-40).

333. On January 21, 1993, the DRAM Task Group made minor technical edits to the NEC mode register that included programmable CAS latency and burst length and had previously been balloted as "Proposed Standard for 16M Bit x 4 Sync DRAM Mode Register" JC 42.3-92-85 (item 376.3). The DRAM Task Group decided that a re-ballot was not necessary and added the ballot to the pass-hold category. (CX 47 at 3).

4. Presentations of Additional Technologies

a. Low Voltage Swing Signaling

334. During 1992, JEDEC work included a number of presentations that included low voltage swing signaling. At the February 27, 1992 JC 42.3 meeting, NEC, Fujitsu, Mosaid Technologies Inc. ("Mosaid"), Sun and Intel all made proposals that included low-voltage swing signaling. (JX 12 at 39, 76, 104, 111, 113; Crisp, Tr. 3045-46). At this same meeting, the JC 42.3 Committee discussed GTL technology for use with SDRAM. (JX 12 at 36, 56-58, 60, 101-02, 104, 111).

335. At the April 8, 1992 Special SDRAM Task Group meeting, the JC 42.3 Subcommittee considered SDRAM proposals that included low voltage swing signaling. (CX 34 at 32

(IBM), 33 (NEC, Fujitsu), 35 (Samsung, Hitachi), 36 (Mitsubishi)).

336. At the May 7, 1992 JC 42.3 meeting, the Subcommittee considered SDRAM proposals that included low voltage swing signaling. (CX 34 at 59 (NEC), 122-123 (Fujitsu)).

337. At the September 16-17 1992, JC 42.3 meeting, the Subcommittee considered Sun's 15 meg SDRAM specification which included low voltage swing signaling. (CX 42 at 31).

338. Complaint Counsel did not present evidence sufficient to find that these low voltage swing signaling presentations were ever balloted or that they were incorporated into the SDRAM standard.

b. Dual Bank Design

339. During 1992 and 1993, JEDEC work included a number of presentations that included dual bank design. At the February 1992 JC 42.3 meeting, the Subcommittee addressed the topic of multiple active subarrays in two presentations (JX 12 at 34, 37) and multibank or dual bank design in other presentations. (*See, e.g.*, JX 12 at 60). The Subcommittee considered proposals for multibank, or dual bank, design from NEC, Mitsubishi, Fujitsu, and Sun. (JX 12 at 39, 60, 76, 110).

340. At the May 7, 1992 JC 42.3 meeting, the Subcommittee considered SDRAM proposals that included dual bank design. (CX 34 at 59 (NEC), 122-123 (Fujitsu)).

341. During that meeting, Kelley of IBM, prompted by Meyer of Siemens, asked Crisp whether Rambus might have patent claims that related to dual bank design. (CX 2089 at 130, 133-37 (Meyer, Infineon Trial Tr.). "The way how Mr. Kelley formulated the question was: Do you want to give a comment on this?" (CX

2089 at 136 (Meyer, Infineon Trial Tr.)). Rambus declined to comment. (CX 2089 at 136 (Meyer, Infineon Trial Tr.)).

342. At the September 16-17 1992, JC 42.3 meeting, the Subcommittee considered Sun's 15 meg SDRAM specification which included a dual bank design. (CX 42 at 30 ("The 4M x 4 device is organized internally as two banks.")).

343. Complaint Counsel did not present evidence sufficient to find that these dual bank design presentations were ever balloted or that they were incorporated into the SDRAM standard.

c. Auto-Precharge

344. At a number of meetings during the course of 1992, the JC 42.3 Subcommittee discussed using the auto-precharge technology in the SDRAM standard. (February 1992: JX 12 at 37, 39 (NEC), 76 (Fujitsu), 94 (Toshiba), 108 (Sun); April 1992: CX 34 at 32 (IBM), 33 (NEC), 35 (Hitachi); May 1992: CX 34 at 6, 150).

345. At the September 16-17, 1992 JC 42.3 meeting, the Subcommittee considered Sun's 15 meg SDRAM specification which included an "autoprecharge" option. (CX 42 at 45). Auto-precharge was incorporated as a feature in the JEDEC SDRAM 21-C standard, issued in November 1993. (JX 56 at 115).

346. Complaint Counsel did not present evidence sufficient to find that these auto precharge presentations were ever balloted or that they were incorporated into the SDRAM standard.

d. Source Synchronous Clocking

347. At the April 1992 JC 42.3 Special Task Group meeting, the DRAM Task Group discussed the issue of source synchronous clocking. (CX 1708 at 2 ("Hitachi brought up the issue of source synchronous clocking."); Crisp, Tr. 3053-54 (recalling that a

discussion on source synchronous clocking had taken place at this meeting)).

348. Complaint Counsel did not present evidence sufficient to find that this discussion of source synchronous clocking was ever balloted or incorporated into the SDRAM standard.

e. Externally Supplied Reference Voltage

349. At the February 27, 1992 JC 42.3 meeting, Samsung proposed an externally supplied reference voltage. (JX 12 at 58; Crisp, Tr. 3043).

350. Complaint Counsel did not present evidence sufficient to find that this presentation was ever balloted or incorporated into the SDRAM standard.

5. Adoption of the SDRAM Standard

351. At the JC 42.3 meeting on March 3-4, 1993, the subcommittee voted unanimously to send 14 SDRAM ballots to Council to become approved as a standard for SDRAMs intended for publication as Release 4 of the 21-C standard. (JX 15 at 14; JX 16 at 5). The ballots were in fact sent to Council after the vote. (G. Kelley, Tr. 2554-55; JX 16 at 5).

352. The subcommittee agreed to issue a press release stating that the Sync DRAM standard has been approved by subcommittee. (JX 15 at 14; G. Kelley, Tr. 2555). A copy of the release was attached to the minutes of the March meeting. (JX 15 at 99). Among the features included in this standard was programmable CAS latency and burst length. (JX 56 at 114).

353. At the JC 42.3 meeting on May 19-20, 1993, Gordon Kelley of IBM reported to the full JC 42.3 subcommittee that the SDRAM ballots had gone to Council and that all council members, apart from AT&T, had supported the ballots. He

attached to the minutes a letter responding to AT&T's concern by proposing additions to the Mode Register. (JX 16 at 5 and 36-37). G. Kelley also distributed copies of the ballots to the subcommittee. (JX 16 at 5; G. Kelley, Tr. 2557-58).

354. On May 24, 1993 the JEDEC Council formally approved adoption of the standard in Release 4 of the 21-C standard. (CX 54 at 8-10; G. Kelley, Tr. 2559-60).

355. In November 1993 JEDEC published the SDRAM standard as JEDEC Standard No. 21-C Release 4. (JX 56; Williams, Tr. 801). The standard included a programmable mode register that includes programmable CAS latency and burst length. (JX 56 at 114; Rhoden, Tr. 456-58; Williams, Tr. 801-03; Sussman, Tr. 1399-400).

356. JEDEC published its standard for SDRAM as part of Release 4 of JEDEC Standard 21-C in November 1993. (First Set of Stipulations, Stip. 19). Since 1993, JEDEC has published several revisions of the JEDEC standard governing SDRAMs, JEDEC Standard 21-C. (First Set of Stipulations, Stip. 20).

357. For a manufacturer to produce JEDEC-compliant SDRAMs, the standard requires the manufacturer to design and produce SDRAMs with programmable CAS latency and burst length on a mode register. (Sussman, Tr. 1399-401).

358. The first published SDRAM standard showed a pinout for three different configurations of SDRAM. (JX 56 at 106). The x4 configuration shown had 11 address lines (A0-A11), 4 data lines (DQ0-DQ3), and 5 control lines (W, CE, RE, S, DQM, and CKE, where CE is equivalent to CAS and RE to RAS). (JX 56 at 106; *see* JX 56 at 18-22). The remaining pins consist of a clock pin, power pins and "no connect" pins. (JX 56 at 106). The x8 configuration added four data lines. (JX 56 at 106). The x9 configuration added an additional data line, bringing the total number of bus lines to 26. (JX 56 at 106). No configuration of

SDRAM with more than 26 bus lines is shown in the standard as initially published in November 1993. (*See* JX 56).

6. Subsequent Proposals: Costs, CAS Latency and SDRAM Lite

359. As late as 1995, asynchronous DRAMs continued to make up approximately 97% of the market, with Fast Page Mode approximating 87.2% and EDOs 9.9% of the market. (Rapp, Tr. 10248).

360. JEDEC members noted that SDRAMs were not being produced due to their overhead and yield issues. (JX 27 at 12-13).

361. JC 42.3 members showed a continued interest in asynchronous DRAMs and at the January 5, 1995 JC 42.3 meeting, Micron made a presentation of an asynchronous DRAM called Burst EDO that was based upon a page mode DRAM. (JX 23 at 69-79; Williams, Tr. 821, 825-26).

362. Although Burst EDO was standardized by JEDEC (Williams, Tr. 873, 879-80; RX 585 at 1), it failed in the marketplace in competition with SDRAM. (Williams, Tr. 829; CX 2108 at 236 (Oh, Dep.) ("this is enhanced version of EDO, and we wanted to convince our customers the advantages of this part, but was not accepted by our customers.")).

363. Other JEDEC members made proposals aimed at reducing the costs of SDRAMs. At the March 15, 1995 JC 42.3 meeting, TI proposed reducing test cost by making CAS latency of 1 optional. The proposal retained the then-current features of SDRAM, including a mode register with programmable CAS latency and burst length. (JX 25 at 14, 107).

364. At the May 24, 1995 JC 42.3 meeting, TI made a second showing of its proposal to make CAS latency of 1 optional. (JX 26 at 9). The proposal continued to retain a mode register with

programmable CAS latency and burst length from the SDRAM standard. (JX 26 at 62). A motion to ballot the TI proposal was unanimously accepted. (JX 26 at 9). Crisp sent an email from the meeting stating that "TI would prefer to eliminate the requirement for supporting CAS latency = 1 to reduce cost of speed testing by removing some testing permutations." (CS 711 at 70).

365. At the September 11, 1995 JC 42.3 meeting, NEC made an SDRAM Lite presentation that proposed an SDRAM with a reduced feature set aimed at saving costs. (Rhoden, Tr. 475-76; Lee, Tr. 6625-27). That proposal suggested using a fixed CAS latency of 3 and two burst lengths of 1 and 4. (JX 27 at 13, 66; Lee, Tr. 6626, 6629-30, 6632, 11,017; Sussman, Tr. 1416-17; CX 91A at 33). The minutes of the meeting at which the presentation was made confirm that NEC wanted to retain burst length of both 1 and 4 in SDRAM Lite. (JX 27 at 13).

366. There was initial support for SDRAM Lite at the meeting, with twenty-three members voting that an SDRAM Lite standard was needed and four voting against. (JX 27 at 12). It was agreed at the meeting that Desi Rhoden would prepare a survey ballot that JEDEC would issue. (JX 27 at 14).

367. At the JC 42.3 meeting on December 6, 1995, SDRAM Lite was further discussed. (JX 28 at 6; CX 711 at 191-92). The discussion indicated that "PC users" would not be satisfied with a single CAS latency of 3. (CX 711 at 191).

368. On January 31, 1996, there was an interim meeting of JC 42.3 where results of the SDRAM Lite survey ballot were discussed. Included in the discussion was having fixed CAS latency and burst length. (JX 29 at 13, 14; Lee, Tr. 6630, 6632, 11018-19). The survey ballot also asked members if they wanted to include auto-precharge in the reduced specification. (JX 29 at 15). The results of the survey ballot indicate that more respondents wanted to retain multiple CAS latency and burst length values than not. (JX 29 at 13).

369. According to Terry Lee of Micron, the SDRAM Lite proposal lost support and was abandoned because it was recognized that the cost added in the full SDRAM technology was not as great as initially thought and because members were frustrated at the length of time it was taking to get a standard. (Lee, Tr. 6634-35; see also Sussman, Tr. 1416-17).

370. SDRAMs began selling in volume in 1997, accounting for 33.5% of the DRAMs sold, and became the dominant product in the market in 1998, accounting for 60.8% of DRAMs sold. By that stage, full page mode DRAMs had declined to 8.8% and EDO to 27.6% of DRAMs sold. (Rapp, Tr. 10248-49).

B. DDR SDRAM – The Next Generation SDRAM

1. Work Within and Outside of JEDEC

371. Work formally began on the DDR SDRAM standard with a first presentation given by Fujitsu in December 1996. (CX 375 at 1; JX 35 at 6, 34-42; Rhoden, Tr. 1197-98).

372. Desi Rhoden was chairman of the 42.3 subcommittee is currently chairman of the JC 42 committee and chairman of the JEDEC Board of Directors. (Rhoden, Tr. 1190-91). In 1998, Rhoden was very actively involved in the DDR SDRAM standardization process within the JEDEC JC 42 committee. (Rhoden, Tr. 1191-92).

373. On March 9, 1998, Rhoden sent an email to Ken McGhee, the JEDEC Secretary, for forwarding to all JC 42 members. (Rhoden, Tr. 1192-93; CX 375). The email was an effort by Rhoden to recap what had transpired in the DDR SDRAM standardization process. (Rhoden, Tr. 1195).

374. Rhoden's email dates the first presentation to JEDEC of a DDR SDRAM proposal as December 1996 and states that the

DDR device was being developed "outside of JEDEC" in 1996. (CX 375 at 1).

375. Rhoden's email also states that the decision to "finally get serious" about DDR SDRAM was not made until March 1997. (Rhoden, Tr. 1201). "Real, focused, dedicated work" on the DDR SDRAM standard did not take place until April 1997. (Rhoden, Tr. 1202). The DDR SDRAM standard did not take "its basic shape" until September 1997. (Rhoden, Tr. 1202).

376. There is other contemporaneous evidence that work on the DDR SDRAM device did not begin, even outside of JEDEC, until the summer of 1996. In an April 1997 presentation, Rhoden stated: "DDR & SLDRAM were Introduced In JEDEC in Dec 1996." (RX 911 at 3).

377. An IBM presentation on DDR SDRAM dated March 17, 1997 notes that "Industry has been working on DDR definition for 6-9 months," that is, beginning at some point between approximately mid-June and mid-September 1996. (RX 892 at 1). Initially, this work consisted of "small supplier consortiums and individual supplier/user meetings." (RX 892 at 1). Consistent with Rhoden, the IBM document dates the first "Official DDR presentations" at JEDEC to December 1996, referring (again) to the first showing by Fujitsu. (RX 892 at 1).

378. A March 10, 1997 Mitsubishi memorandum regarding "DDR SDRAM Specification Planning History and Recent Trends" confirms that DDR efforts began outside of JEDEC in the summer of 1996. "To counter Intel's move toward adopting Rambus, eight companies have been meeting once every 2 weeks to quickly plan DDR specifications." (RX 885A at 1). The Mitsubishi memorandum's first mention of JEDEC work relating to DDR SDRAM is the first showing by Fujitsu in December 1996. (RX 885A at 1).

379. A July 1997 official JEDEC ballot form regarding a proposed DDR SDRAM pinout states: "DDR SDRAMs has been under discussion within JEDEC since September 1996." (RX 967 at 1).

380. JC 42.3 committee approval of the DDR SDRAM standard was made in March 1998, but was not published until 2000. (*See* CX 375 at 1; JX 57).

381. The DDR SDRAM standard received JEDEC Board of Director approval in 1999. (Rhoden, Tr. 743).

382. The first time that a balloted item was approved as part of the JEDEC DDR SDRAM standard was June 1997. (CX 375 at 2).

2. Future Synchronous SDRAM Features

383. Despite detailed minutes taken at each JEDEC meeting about what presentations were made and what topics discussed, there is little evidence regarding any discussion of "next generation SDRAM" until late 1995, when a "Future Synchronous DRAM (SDRAM) Features" survey ballot was issued. (*See* CX 260 at 1).

384. Complaint Counsel presented a March 1995 email from Crisp which quotes Wiggers, a JEDEC representative from Hewlett-Packard, as saying that JEDEC had been working for over two years to standardize a high-speed interface. (CX 711 at 54). In the next line Crisp states that "[t]his servers [sic] to further underscore the fact that the JC 16 committee (led by Farhad Tabrizi of Hyundai) is not delivering on its responsibilities." (CX 711 at 54). Thus, Wiggers's statement was in reference to the work of JC 16, *not* in reference to some undefined new kind of SDRAM within the JC 42.3 subcommittee. (Crisp, Tr. 3520-21).

385. The testimony of Peter MacWilliams of Intel, who testified that he "first heard about DDR in '95" (MacWilliams, Tr.

4815), says nothing about JEDEC. MacWilliams may have been referring to what Rhoden had described as "private and independent work outside of JEDEC for most of 1996 . . .." (CX 375 at 1).

386. Moreover, since the JEDEC future SDRAM survey ballot was not issued until late 1995, with the results not presented at JEDEC until December 1995, it is unlikely that MacWilliams was aware in any JEDEC-related context, prior to that time, of what features might be in a next generation standard. (*See* CX 260; JX 28 at 6).

a. Presentation of Programmable CAS Latency and Burst Length

387. In October 1995, JEDEC staff distributed to subcommittee members, including Rambus, a survey ballot requested at the September 1995 JC 42.3 meeting. (CX 260). The subject of the survey was "Future Synchronous DRAM (SDRAM) Features." (CX 260 at 1). The ballot asked whether members thought it important to add any additional latency values to those already available. (CX 260 at 9).

388. The results of the SDRAM Features Survey Ballot that had issued on October 30, 1995 were tallied at the same meeting on December 6, 1995. (JX 28 at 36-48). Mosaid made a presentation on the results of the survey. (JX 28 at 6). The CAS latency portion of the survey results showed that JC 42.3 members strongly supported adding into the mode register CAS latencies in excess of four. (JX 28 at 42).

389. At the March 20, 1996, JC 42.3 meeting, the RAM features and functions subcommittee made a presentation that included use of programmable CAS latency and burst length. (JX 31 at 64).

390. At the June 5, 1996, JC 42.3 meeting, two presentations were made by Oki on behalf of EIAJ that included programmable CAS latency and burst length. (JX 33 at 7, 41-46 and JX 33 at 47-49). The presentations for 100-150 MHz SDRAM included three required burst length values and four required CAS latency values. (JX 33 at 41, 45, 47, 48).

391. At the September 10, 1997 JC 42.3 meeting, the subcommittee voted unanimously to send a DDR mode register to Council. (JX 40 at 7-8; Lee, Tr. 6640-41). That mode register included programmable CAS latency (CX 234 at 150; JX 57 at 12; Lee, Tr. 6641) and burst length (CX 234 at 150; JX 57 at 12).

392. The mode register was approved by Council and included in Release 9 of the 21-C standard published by JEDEC in August 1999 and subsequently in the consolidated DDR SDRAM Specification (JESD79) that was published by JEDEC in June 2000. (JX 57 at 12).

b. Discussion of PLL/DLL

393. There was recognition in the mid-1990's among JEDEC members that, as bus speed increased, an on-chip PLL or DLL would become necessary. (Soderman, Tr. 9408-10; Rhoden, Tr. 546).

394. PLLs are similar to DLLs in that they can be used for similar purposes in some applications. (Jacob, Tr. 5617). They are, however, different types of circuits: a PLL uses a voltage controlled oscillator while a DLL uses variable delay lines. (Jacob, Tr. 5616-17).

395. Rhoden testified that the JEDEC subcommittee members used the terms PLL and DLL interchangeably. (Rhoden, Tr. 492). Once JEDEC chose a DLL, the contemporaneous evidence shows it was always referred to as a "DLL," never as a "PLL." (*See, e.g.*, CX 234 at 176).

396. When Rambus first presented its technology to DRAM manufacturers in the 1989-90 time frame, many felt that it was not possible to put a PLL on a DRAM. (Horowitz, Tr. 8517). As late as 1997, well after Rambus had proven that PLLs and DLL could be placed on DRAMs and very high data transfer rates achieved, many DRAM manufacturers remained daunted by the difficulties involved. In a November 1997 email, for example, Hans Wiggers of Hewlett-Packard explained that DLLs would be "essential" for the data rates that they hoped to achieve, while recognizing that "I know everyone is afraid of DLLs." (RX 1040).

397. At the September 13-14, 1994 JC 42.3 meeting, NEC made a presentation regarding PLLs on SDRAMs. NEC's presentation showed an on-chip PLL circuit and proposed to include a PLL-enable bit in the mode register in order to enable on-chip PLLs. (JX 21 at 87, 91, 92; Rhoden, Tr. 466; G. Kelley, Tr. 2569-70).

398. As both Complaint Counsel's technical expert and Rambus's technical expert made clear, PLLs and DLLs are implemented differently – the former uses a voltage controlled oscillator, while the latter uses variable delay lines. (Jacob, Tr. 5443, 5617; Soderman, Tr. 9401).

399. In October 1995, JEDEC staff distributed to subcommittee members, including Rambus, the survey ballot requested at the September 1995 JC 42.3 meeting. (CX 260). The subject of the survey was "Future Synchronous DRAM (SDRAM) Features." (CX 260 at 1). Question 3.9-1 asked members whether they believed that use of an on-chip PLL or DLL was important to reduce the access time from the clock for future generations of SDRAMs future generations of DRAMs. (CX 260 at 12).

400. At the JC 42.3 meeting of December 6, 1995, the tally of the votes cast in the Future SDRAM Features Survey Ballot was announced. Eleven members voted "yes" and four members "no"

to the question as to whether their company believed that "on chip PLL or DLL is important to reduce the access time from the clock for future generations of SDRAMs." (JX 28 at 45). On-chip PLL/DLL was included among issues with "strong support" in the conclusion of the SDRAM Feature Survey Ballot. (JX 28 at 35).

401. Mosaid presented the results of the survey. In response to a question from Hyundai Electronics Industries ("Hyundai"), Mosaid disclosed a pending patent application with claims relating to on-chip DLL technology, but stated that the patent likely to result from the application may not be necessary to use a standard but rather would be an implementation patent. (JX 28 at 6; CX 711 at 192). Mosaid agreed to comply with the patent policy if the patent ends up as a "concept patent," not if it ends up as an "implementation patent." (CX 711 at 192).

402. At the January 31, 1996 JC 42.3 interim meeting, Micron presented a proposal discussing the potential use of on-chip PLL/DLLs and echo clocks in Future SDRAMs. (JX 29 at 17). Micron proposed using a single PLL on the controller or clock chip and echo clocks rather than on-chip PLLs. (JX 29 at 18; Rhoden, Tr. 487).

403. At the JC 42.3 meeting of March 20, 1996, Desi Rhoden, on behalf of the JC 42.3C RAM Features and Functions Letter Committee, made a presentation that included on-chip PLL/DLL. (JX 31 at 64; Rhoden, Tr. 492). The presentation provided information regarding what features might be required in the future and confirmed the general knowledge that to achieve high data transfer rates, an on-chip PLL or DLL would be required. (JX 31 at 64).

404. Samsung also made a future SDRAM proposal that included discussion of alternatives to on-chip PLL/DLL. (JX 31 at 68-72; Rhoden, Tr. 513-14; Lee, Tr. 6691). The Samsung presentation related to "alternatives to on-chip PLL/DLL" as it proposed a PLL on the memory controller. (JX 31 at 71)).

405. During the course of its work relating to what ultimately became the DDR SDRAM standard, the JC 42.3 subcommittee also considered, as an alternative to on-chip PLL/DLL, the use of vernier circuits. (JX 36 at 58, 64; CX 367 at 3; Kellogg, Tr. 5168).

406. During the course of its work relating to what ultimately became the DDR SDRAM standard, the JC 42.3 subcommittee also considered, as an alternative to on-chip PLL/DLL, the use of an edge-aligned, bi-directional data strobe. (CX 368 at 1, 4; CX 370 at 2, 3; CX 2713 at 2). Although DDR SDRAMs have a "bidirectional data strobe (DQS)," they still use a DLL to align the strobe with the clock. (JX 57 at 5).

407. By the time of the JC 42.3 meeting of December 9-10, 1997, the subcommittee had decided to include an on-chip DLL in the DDR standard that could be turned on or off. (Lee, Tr. 6680-81). At this meeting the subcommittee discussed the timing of a device where the on-chip DLL was disabled or enabled. (JX 41 at 18; Lee, Tr. 6680-81).

c. Consideration of Dual Edge Clocking

408. Dual edge clocking can refer to a number of technologies and implementations and is not limited to capturing data off both edges of the clock. (*See* Lee, Tr. 6688).

409. In a DDR SDRAM, the clock is all but ignored during writes to the DRAM; the DRAM samples incoming data not with respect to the system clock, but with respect to another signal known as the DQS data strobe. (Jacob, Tr. 5642).

410. In a DDR SDRAM read operation, data is driven by a data strobe which is not a "clock." A "clock" is a "free-running" signal, that is running all the time, while the data strobe in DDR SDRAMs is not free-running. (Macri, Tr. 4634).

411. IBM and other JEDEC members made further High Speed Toggle ("HST") proposals in 1990 and 1991. (G. Kelley, Tr. 2584-85). HST did not transfer data on both edges of the clock signal, but instead on both edges of a "toggle" signal. While some witnesses loosely referred to this toggle signal as a "clock," it was not a free running clock like the system clock in a synchronous memory such as SDRAM or DDR SDRAM. (Rhoden, Tr. 437; Sussman, Tr. 1471).

412. At the JC 42.3 Subcommittee meeting held on December 4-5, 1991, Mark Kellogg of IBM made a presentation comparing High Speed Toggle to synchronous DRAMs. (JX 10 at 5, 84; Kellogg, Tr. 5172-73).

413. Although IBM held patents on HST (G. Kelley, Tr. 2715), there is no evidence that they disclosed them in connection with DDR SDRAM.

414. At a special meeting of the JC 42.3 Subcommittee Task Force held on April 14, 1992, IBM proposed a "slightly modified version of its HST technology." This proposal was for an asynchronous DRAM. (CX 34 at 32).

415. At a meeting of the JC 42.3 subcommittee held on May 24, 1995, Hyundai, Texas Instruments and Mitsubishi all made presentations relating to the SyncLink technology. (JX 26 at 10-11, 95-112).

416. In October 1995, JEDEC staff distributed to subcommittee members, including Rambus, a survey ballot requested at the September 1995 JC 42.3 meeting. (CX 260). The subject of the survey was "Future Synchronous DRAM (SDRAM) Features." (CX 260 at 1). Question 3.9-4 asked members whether they believed future generations of DRAMs could benefit from using both edges of the clock for sampling inputs. (CX 260 at 12). This question related to dual edge clocking. (Calvin, Tr. 1033; Lee, Tr. 6689).

417. At a meeting of the JC 42.3 Subcommittee held on December 6, 1995, the results of the survey ballots were tabulated and announced. No clear consensus on the proposed use of dual edge clock in the next generation standard was reached, with seven members responding that the next generation of SDRAMs would benefit from using dual-edge clock technology and nine members responding that it would not. (JX 28 at 45). Two specific comments relating to dual edge clock technology were recorded in the results of the survey ballot, both supportive of using the technology. (JX 28 at 45).

418. At a meeting of the JC 42.3 Subcommittee held on March 20, 1996, Samsung made a presentation proposing to use dual edge clock technology in the future SDRAM standard. (JX 31 at 71; Rhoden, Tr. 512; Calvin, Tr. 1035; Landgraf, Tr. 1719-20; G. Kelley, Tr. 2581-82; CX 2114 at 85 (Karp, Dep.)). There is no evidence that the Samsung presentation ever progressed any further.

419. At the same meeting in March 1996, JEDEC considered running a single-edged clock faster in order to double the data rate. (Rhoden, Tr. 542-43; *see* JX 31 at 64). Rhoden's presentation was not a proposal for a device; it simply provided information regarding what features would be required in the future if certain clock speeds were eventually implemented. (Rhoden, Tr. 542-43; *see* JX 31 at 64).

420. During the course of its work relating to what ultimately became the DDR SDRAM standard, the JC 42.3 Subcommittee also considered, as a possible alternative to dual edge clocking, the use of a single edged clock. (CX 371 at 3; Lee, Tr. 6710-13).

421. At the September 10, 1997, JC 42.3 meeting the subcommittee voted to send a ballot including using both edges of a data strobe to Council. (JX 40 at 8; Lee, Tr. 6714-15).

422. In 1999-2000, JEDEC considered the possibility of interleaving SDRAM chips on the module in order to double the data rate. (CX 150 at 109-17). In December 1999, Kentron Technologies, Inc. ("Kentron") made a proposal to JEDEC to interleave SDRAM chips on the module. (CX 150 at 115).

3. Subsequent Proposed Features

a. Externally Supplied Reference Voltage

423. At the May 1994 JC 42.3 meeting and the March 1995 JC-16 meeting, there were presentations regarding externally supplied reference voltage. (CX 711 at 25, 27; CX 711 at 52, 54).

424. Some SDRAM pinouts included an optional VREF pin, making it clear that an externally supplied reference voltage was not required for the SDRAM standards; DDR SDRAM pinouts contain a VREF pin. (Lee, Tr. 11035).

b. Source Synchronous Clocking

425. During the March 15, 1995 JC 42.3 meeting, Crisp recorded a Fujitsu representative's suggestion that it would be necessary to use two clocks, a clock-in and clock-out, for high speed operation. (CX 711 at 58). In an email Crisp stated, "[i]t appears that they are starting to figure out that we have a very good idea with respect to source synchronous clocking. Of course they may get into patent trouble if they do this." (CX 711 at 58).

426. JEDEC included a bidirectional data strobe, or DQS strobe, as part of the DDR SDRAM standard. (CX 234 at 164). The data strobe might be considered to be a form of source synchronous clocking, but it is not a well-defined technology. (Lee, Tr. 6682).

4. Adoption of the DDR SDRAM Standard

427. In August 1999, JEDEC issued Release 9 of the 21-C standard. (CX 234).

428. Users requested that JEDEC take everything that related to DDR out of Release 9 and put it in a separate specification. (Rhoden, Tr. 1293-94). In response to user requests, JEDEC took all of the DDR specifications that had previously issued in Release 9 of the 21-C standard (CX 234) and put them together in one document. (Rhoden, Tr. 1293-94). That document, entitled "Double Data Rate (DDR) SDRAM Specification" and numbered "JESD79" was published in June 2000. (JX 57; Rhoden, Tr. 1293-94).

429. Apart from the possibility of some slight updating and clean-up, JESD79 contains the same DDR related material as in Release 9 of the 21-C standard. (Rhoden, Tr. 1294).

5. Features Incorporated into the Standard

430. The DDR SDRAM Standard incorporated in Release 9 of 21-C and JESD79 included many features that had been previously adopted in the first generation SDRAM standard as well as new features such as dual edge clocking and on-chip DLLs. (Sussman, Tr. 1428-29; McWilliams, Tr. 4822; Bechtelsheim, Tr. 5871-72; CX 2451 at 20).

a. On-Chip DLL

431. The DDR SDRAM standard utilizes the use of on-chip DLLs. (CX 234 at 176; CX 234 at 197; JX 57 at 8; Lee, Tr. 6643; Rhoden, Tr. 564).

b. Dual Edge Clocking

432. The DDR SDRAM requires a particular implementation of dual edged clocking in which read data is aligned with the rising and falling edges of the clock, but write data is not. The JESD79 DDR SDRAM specification covers SDRAMs that have

dual edge clocking. (JX 57 at 5, 21; Sussman, Tr. 1427; Kellogg, Tr. 5172).

c. Programmable CAS Latency and Burst Length

433. The DDR standard requires a particular implementation of programmable CAS latency and burst length according to which these values are programmed in specific bits of a mode register. (CX 234 at 150; Geilhufe, Tr. 9742-44; Lee, Tr. 6625). In June 2000, JEDEC published a Double Data Rate (DDR) SDRAM Specification (JESD79), which was unique to DDR SDRAM. It continued to include a programmable mode register to define CAS latency. (JX 57 at 12).

C. Interoperability: The Effect of JEDEC's Specifications versus Manufacturers' Specifications

434. The JEDEC SDRAM and DDR SDRAM standards determined what features were required to be present in JEDEC compliant DRAMs. (Peisl, Tr. 4384).

435. The JEDEC SDRAM and DDR SDRAM standards were sometimes insufficient to ensure interoperability, forcing other industry participants, primarily Intel, to issue specifications used by the DRAM manufacturers in place of the JEDEC standards. (MacWilliams, Tr. 4908-09; *see also* Krashinsky, Tr. 2814-15).

V. RAMLINK AND SYNCLINK, THE SYNCLINK CONSORTIUM, INTEL AND DRAM MANUFACTURERS

436. In addition to the Rambus and JEDEC efforts to develop standards for next generation DRAM technology, there were other similar efforts during the 1990's. Among these were the Ramlink, SyncLink and SyncLink Consortium efforts, which did not result in commercially viable DRAM standards. (F. 437-86).

A. The IEEE RamLink and SyncLink Working Groups

1. The IEEE Membership Requirements and Lack of Patent Disclosure Obligations

437. The Institute of Electrical and Electronic Engineers, Inc. ("IEEE") was a professional organization that engaged in various activities, including standard setting activities. (Tabrizi, Tr. 9117; RX 668 at 2; RX 2011 at 1).

438. Membership in the IEEE was not by company; rather, individuals belonged to IEEE in their individual capacity. (Tabrizi, Tr. 9117; RX 579). There was significant overlap between IEEE and JEDEC, including, for example, individuals from five companies attended both the August 21, 1995 IEEE 1596.6 meeting and the September 11, 1995 JEDEC 42.3 meeting. (First Set of Stipulations, Stip. 21).

439. The IEEE procedures did not impose any obligation on companies with respect to patent disclosure. (Tabrizi, Tr. 9122; Crisp, Tr. 3283-84; JX 27 at 26).

2. RamLink Was Developed to Standardize a New Future Memory Bus

440. RamLink was being developed by the 1596.4 working group within the IEEE. (Gustavson, Tr. 9280). According to a trip report regarding the February 22, 1995 Ramlink II Working Group, "[t]he Ramlink concept is to use super high speed serial link to transfer the memory (not necessary DRAM) data to processor." (RX 535 at 1).

441. RamLink developed as an effort to standardize a new generic bus to which one could connect any kind of memory. (Tabrizi, Tr. 9117).

442. IEEE was balloting the RamLink proposal for standardization as of June 1995. (Gustavson, Tr. 9283).

3. The IEEE SyncLink Project Emanated From and Modified the Proposed RamLink Standard

443. SyncLink developed as a subset of RamLink. (Tabrizi, Tr. 9117; Gustavson, Tr. 9280-82). Whereas RamLink was intended to be a generic bus to which one could connect any kind of memory, SyncLink was intended to be specific to synchronous DRAMs. (Tabrizi, Tr. 9117).

444. The SyncLink project thus modified the RamLink protocol. (Gustavson, Tr. 9284; *see also* RX 589 at 1). The resulting SyncLink architecture was partially multiplexed; command and address information were sent on a single bus, but data was sent on a separate bus. (Tabrizi, Tr. 9119).

445. RamLink consisted of a high speed bus protocol that permitted access, based on scheduling of events, to the bandwidth that already existed inside DRAMs. (JX 26 at 95).

446. Richard Crisp attended some of the meetings of the IEEE RamLink and SyncLink working groups. (Crisp, Tr. 3528; RX 579 at 6; RX 590 at 3).

4. Presentation of the RamLink/Synclink Architecture at JEDEC – Rambus Elects Not to Comment On Its Intellectual Property Position

447. In May 1995, Hyundai, Texas Instruments, and Mitsubishi presented the RamLink and SyncLink architectures at JEDEC. (JX 26 at 10-11, 95-113). The Mitsubishi presentation of SyncLink included a description of dual edge clocking. (JX 26 at 112; Rhoden, Tr. 471-72; Kelley, Tr. 2574-75; Sussman, Tr. 1408-09).

448. Gordon Kelley asked whether any companies had patent issues regarding SyncLink. (CX 711 at 72).

449. When Crisp, the Rambus JEDEC representative, did not respond to this inquiry at the May 1995 meeting, Kelley asked Crisp to go back to Rambus and then report back to the Committee whether Rambus knew of any patents, especially Rambus patents, that may read on the SyncLink technology. (CX 711 at 73; Crisp, Tr. 3267-68).

450. At the September 1995 meeting of the JEDEC Committee, Crisp provided the Committee a letter from Rambus stating "Rambus elects not to make a specific comment on our intellectual property position relative to the SyncLink proposal" and that "[o]ur presence or silence at committee meetings does not constitute an endorsement of any proposal under the committee's consideration nor does it make any statement regarding potential infringement of Rambus intellectual property." (CX 829).

5. Richard Crisp Indicates That the SyncLink Proposal May Infringe Rambus Patents But Declines To Comment Regarding Rambus Intellectual Property

451. In June 1995, Reese Brown posted a copy of the ballot for the proposed IEEE RamLink standard on the JEDEC reflector. (CX 711 at 76-77).

452. Thereafter, Crisp wrote an email to Brown stating in part that the proposed IEEE standard had patent issues associated with it. (CX 711 at 79-80; Crisp, Tr. 3282-83). Brown forwarded Crisp's email to Hans Wiggers, the Chairman of the RamLink working group as of mid-1995. (Crisp, Tr. 3283; Gustavson, Tr. 9282).

453. Wiggers wrote to Crisp because, as Chairman of the RamLink working group, he took Crisp's comment about patent issues "very seriously." (CX 711 at 90-91; Wiggers, Tr. 10595). Wiggers stated that he assumed Crisp had attended the IEEE working group meetings in "good faith," and if Crisp knew of any way in which the proposed RamLink standard violated patents held by Rambus or others, he thought Crisp had a "moral obligation" to bring to his attention information about which patents were being violated. (CX 711 at 90-91; Crisp, Tr. 3284-86).

454. Crisp replied to Wiggers by email:

> Regarding patents, I have stated to several persons that my personal opinion is that the Ramlink/Synclink proposals will have a number of problems with Rambus intellectual property. We were the first out there with high bandwidth, low pincount; DRAMs, our founders were busily at work on their original concept before the first Ramlink meeting was held, and their work was documented, dated and filed properly with the US patent office.
>
> . . .
> If you want to search for issued patents held by Rambus, then you may learn something about what we clearly have covered and what we do not. But I must caution you that there is a lot of material that is currently pending and we will not make any comment at all about it until it issues.

(CX 711 at 104-05).

455. Wiggers wrote to Crisp again in July 1995, stating that as part of submitting the RamLink standard to the IEEE Standards Board, he had to certify that there were no patent issues

outstanding. He stated that he had to report his previous communications with Crisp. (CX 711 at 130-31; Crisp, Tr. at 3291-92).

456. Wiggers ultimately related to the working group only a short statement to the effect that Crisp expressed a personal opinion that the SyncLink proposal may infringe Rambus patents that date as far back as 1989. (CX 711 at 146; *see also* Crisp, Tr. 3296-97).

457. The Secretary of the SyncLink Consortium, Dr. Gustavson, and two other engineers subsequently undertook to review the claims in Rambus's pending patent applications and came to the conclusion that the SyncLink device would infringe those patents, if they issued. (Gustavson, Tr. 9286-87).

458. The IEEE thereafter requested that the 1596.4 working group redesign the RamLink standard so that it wouldn't violate any Rambus patent claims. (Gustavson, Tr. 9296-97).

459. After Gustavson reviewed the claims of certain of Rambus's pending patent applications, he concluded that there was no way to work around the claims that he saw, since they related to things that the working group had been doing for ten years or so. (Gustavson, Tr. 9286-87). Nevertheless, Gustavson thought the Rambus patent claims should not block the balloting of the proposed RamLink standard. (Gustavson, Tr. 9294).

460. Gustavson concluded, "[w]e discussed the situation re patents in general, and seem to be in agreement that standards ought to make no assurance to the eventual user that no patent conflicts are involved, . . . because that is impossible. Firstly, the writers may not become aware of conflicting patents until long after the standard is finished, due to the various pipeline delays and imperfect communication. As far as I could tell, Crisp and Rambus's positions were entirely reasonable in this regard, and so I expect they won't try to interfere with the standardization

process (they are going to great lengths to separate themselves from it now. . . .)." (RX 593 at 2).

461. Although the IEEE later issued the proposed RamLink standard, no product implementing the RamLink standard ever came to market. (Prince, Tr. 9012).

6. Hyundai Negotiates "Other DRAM" Provision As Part of Its RDRAM License Agreement

462. After Hyundai became aware that Rambus might have patents covering aspects of SyncLink, it negotiated an "Other DRAM" provision in its license agreement with Rambus as a kind of "insurance program." A draft amendment to the license agreement was sent by Rambus to Hyundai and expressly listed SDRAM and DDR SDRAM as examples of "Other DRAM" under the agreement. (RX 2275 at 1). This "Other DRAM" provision permitted Hyundai to use Rambus technology in DRAMs other than RDRAMs, on the condition that Hyundai complied with its contractual obligations, including an itemization of all products subject to royalties, the marking of all such products with Rambus proprietary markings, providing royalty reports showing shipments of all such products each quarter, and ongoing payments of royalties for such products. (CX 1599 at 12-14, ¶¶ 5.3, 5.5).

463. Hyundai and Rambus signed a license agreement in December 1995. Included in the Hyundai-Rambus license agreement is an "Other DRAM" provision that granted Hyundai the right to use Rambus technology in DRAMs other than RDRAMs, subject to payment of a 2.5% royalty. (CX 1599 at 3, 12; Crisp, Tr. 3320-22; *see also* CX 2107 at 84-85, 91-92 (Oh Dep.)).

B. The SyncLink Consortium

1. Formation and Purpose of the Consortium

464. In August 1995, Hyundai, Mitsubishi, Mosaid, Texas Instruments, Micron, Samsung, and Apple formed the SyncLink Consortium. (RX 591 at 1; RX 610 at 1). Companies joining later or sending attendees included Hitachi, Fujitsu, NEC, Hewlett-Packard, IBM, Panasonic, Molex, VIS, AMP, and Vanguard International. (RX 2090 at 7-8). Members included not only DRAM suppliers, but also customers and other companies. (Tabrizi, Tr. 9177-78). Of the thirty-four companies that attended at least one SyncLink/SLDRAM Inc. meeting in 1996 or 1997, thirty-one also attended a JEDEC 42.3 meeting in that same time period. (Respondent's Submission Regarding Company Attendance at SyncLink and JEDEC 42.3 Meetings (October 28, 2003)).

465. The SyncLink Consortium was intending to develop the next generation main memory architecture that could be used in various applications, including personal computers, servers, workstations and various other segments of the market. (Tabrizi, Tr. 9126-27; *see also* RX 591 at 2).

466. While the SyncLink Consortium represented to the public that it was "developing an open, royalty-free industry standard," the Consortium members had agreed among themselves that the SyncLink-related patents would only be freely available to members of the Consortium and its corporate successors, SLDRAM Inc. and Advanced Memory, Inc. ("AMI2"). (*Compare* RX 765 at 1 (9/9/96 press release referencing a "royalty-free standard"), *with* RX 591 at 2 (8/22/95 SyncLink minutes stating that patents will be "freely available to Consortium members")).

467. The SyncLink Consortium received a patent on the SyncLink pinout itself – the very specification that had been standardized by JEDEC. (Rhoden, Tr. 1211; *see* RX 2086).

468. Moreover, AMI2 Chairman and JEDEC President Desi Rhoden, who is a named inventor on the SyncLink "pinout patent," testified that when SyncLink announced that SLDRAM would be "royalty free," that did not mean free. (Rhoden, Tr. 1214).

469. In fact, the Consortium's corporate successor has offered to license the patents at reasonable royalty rates. (RX 1858 at 1).

470. The SyncLink Consortium was formed as a consortium outside of the IEEE in part because the Consortium members did not consider the IEEE rules regarding disclosure of patents to be satisfactory. Because individual members in the IEEE represented only themselves and not any company, there was no obligation of patent disclosure. (Tabrizi, Tr. 9120, 9122).

471. The SyncLink Consortium members shared know-how and design experience relating to the SyncLink architecture. (Tabrizi, Tr. 9128-29).

472. The SyncLink Consortium members also shared the cost of development of the first chip and the expenses associated with other projects. SLDRAM Inc. levied special assessments of its members as needed for different projects. (Tabrizi, Tr. 9128).

2. Concern About Patents of Non-Members

473. The SyncLink Consortium applied for and held patents in its own name. (Tabrizi, 9124-25; Gustavson, Tr. 9314).

474. Consortium members used the patents to encourage companies to join the Consortium (and its successor, AMI2) and to discourage members from resigning from the Consortium. (*See* RX 1100 at 2; RX 1362 at 1 (*in camera*)).

475. Members of the SyncLink Consortium were particularly concerned about avoiding Rambus's patents. (CX 488 at 2; *see also* Gustavson, Tr. 9302-03).

3. SyncLink's Activities With Respect to Rambus Patent Applications and Intel's Announced Support of RDRAM

476. As previously noted, the SyncLink Consortium Secretary, Dr. David Gustavson, reviewed Rambus's pending European patent applications along with two other Consortium representatives and determined that the SyncLink device *would* infringe, *if* the applications ever issued as patents. (Gustavson, Tr. 9286-87). Gustavson did not, however, believe that the patents would issue, (Gustavson, Tr. 9286-87), and Hans Wiggers, the chair of the Ramlink Committee, believed that Rambus was simply trying to "torpedo" the Ramlink and SyncLink standards. (Wiggers, Tr. 10589).

477. Similarly, in April 1997, Micron JEDEC representatives and JEDEC Council member Terry Walther thought "that is old technology." (RX 920 at 1). Another Micron JEDEC representative, Terry Lee, testified that when he learned that Rambus planned "to request royalties on all DDR memory efforts" (RX 920 at 2) in April 1997, he "didn't believe this was true," and he did nothing to follow up. (Lee, Tr. 6981).

478. Certain JEDEC members, especially the leadership of the 42.3 committee, held views that the Patent Office often issued patents for "old technology," as Walther put it, and the 42.3 committee even considered offering its services as "a source of expert opinions on memories to the patent office." (JX 32 at 2). JEDEC 42.3 members therefore, might well have believed that any Rambus patents on features as on-chip PLL or dual edge clocking would be invalid because of prior art. (*See*, *e.g.*, CX 711 at 37).

479. In late 1996, Intel announced that its future chipsets for main system memory in personal computers would support exclusively Rambus's RDRAM. (Tabrizi, Tr. 9134-35). As a result of that decision, DRAM manufacturers expected SyncLink to be relegated to non-PC applications, including servers, Apple-based computers, and systems using UNIX-based processors. (Tabrizi, Tr. 9134-35, 9137).

480. Following Intel's announcement of its decision to support only RDRAMs for main memory in future PC systems, Tabrizi organized a meeting of executives representing the SyncLink Consortium members in January 1997 to determine the future of the SyncLink Consortium. (Tabrizi, Tr. 9138-39; RX 808 at 1-2).

481. At the meeting, the level of support for the SyncLink Consortium varied from company to company; the participants agreed to continue at least to support the SyncLink Consortium's development work, but not to commit major resources to it. (Tabrizi, Tr. 9139-40).

482. Because Intel supported Rambus, Hyundai executive, Dr. Oh believed he had no choice but to produce RDRAM. (CX 2107 at 117 (Oh, Dep.)). In order to produce RDRAMs, Dr. Oh believed that Hyundai needed to have support from Rambus. (CX 2107 at 118-19 (Oh, Dep.)).

483. Dr. Oh thereafter instructed Tabrizi to resign from the competing SyncLink Consortium. (CX 2107 at 117 (Oh, Dep.)).

484. By the fall of 1998, Intel informed Tabrizi that "they would like to start working on Intel next generation memory solution beyond RDRAM as soon as possible," and that they wanted to develop that post-Rambus device *with the DRAM manufacturers*, instead of continuing to develop further generations of Rambus memory. (RX 1361 at 1).

485. In a December 1998 email to Dr. Oh, Tabrizi said: "I am no longer head of SLDRAM Inc. as of 12/17/98, and I believe the organization will die slowly from here on. Job accomplished." (RX 1361 at 1).

486. The SyncLink architecture was not accepted within the industry and never went into volume production. (Appleton, Tr. 6319; Tabrizi, Tr. 9184; Peisl, Tr. 4492). An IBM engineer had pointed out as early as 1996, the SyncLink device appeared to be "vaporware compared to Rambus." (RX 839 at 1).

C. Rambus's Relationships With Intel and DRAM Manufacturers

1. Rambus Sought Licenses and Support for RDRAM From DRAM Manufacturers After Intel Endorsed RDRAM Technology

487. In late 1995, Intel made an internal decision that it would support the proprietary Rambus RDRAM technology with the next generation of Intel microprocessors. (RX 1532 at 1). The decision was followed by a lengthy period of meetings and negotiations with Rambus and with DRAM manufacturers. (RX 1532 at 1-2).

488. Intel and Rambus signed a contract in November 1996 and Intel announced that its future desktop PC chipsets would only work with RDRAM. (RX 1532 at 2; Tabrizi, Tr. 9135; Crisp, Tr. 3432-33; CX 2634 at 1). During this time, Intel controlled about eighty percent of the market for microprocessors used in personal computers. (Tabrizi, Tr. 9138-39).

489. During the beginning of the Rambus-Intel partnership, Intel hoped that Rambus would be a "value-added part of this whole industry infrastructure." (MacWilliams, Tr. 4870-71). Intel envisioned an industry infrastructure where DRAM vendors built DRAMs, Intel built chipsets, and "Rambus provide[d] all of the

glue to make the enabling pieces work and therefore would be perceived as valuable." (MacWilliams, Tr. 4871).

490. Projected demand for RDRAM increased sharply after Intel announced it would produce chipsets that used RDRAM. (Hampel, Tr. 8677-78).

491. According to an April 21, 1996 Microprocessor Report article: "Intel's move was motivated by the incessant need to provide more system-level performance" and "Rambus had a proven track record of delivering cheap, high-bandwidth systems." (CX 2634 at 1).

492. In the Microprocessor Report article, Rambus's royalties were noted as being:

> an emotional issue for many in the DRAM industry, yet these royalty relationships are commonplace in the DRAM industry. Texas Instruments, for example, currently derives more income from its DRAM patent portfolio than Rambus can reasonably expect to generate within the next decade. The aggravating issue is not so much royalties *per se*, but new and blatantly aboveboard royalties. Also, because Rambus is an intellectual-property company, its licensing relationships do not have the same sense of reciprocity and *quid pro quo* as do other licensing arrangements in the industry.

(CX 2634 at 3).

493. Micron Chairman Steve Appleton was surprised about Intel's decision to endorse Rambus. (Appleton, Tr. 6344).

494. After Intel's support of RDRAM, Micron engaged in licensing negotiations with Rambus because "the probabilities of

customers in the marketplace actually using it increased quite a bit, and as a result, we also then believed that some customers would use RDRAM and that we needed to then engage to negotiate for a license." (Appleton, Tr. 6345-46).

495. [redacted] (CX 2699 at 1 (*in camera*)).

496. In February 1997, Mitsubishi signed a license agreement with Rambus covering Direct RDRAM. (CX 1609 at 1-19). The subject matter of the Mitsubishi agreement was limited to Rambus-compatible DRAMs, interfaces and matters such as design and development support. (CX 1609 at 1-2).

497. In March 1997, Hyundai amended its RDRAM license agreement with Rambus to include Direct RDRAM. (CX 1612 at 1-7; CX 1599 at 1-23; CX 1600 at 1-22). Hyundai's new agreement included royalties on Direct RDRAM ranging from 1.5% to 2.0% depending on the sale date and the relative revenue for the sales. (CX 1612 at 5).

498. In March 1997, Micron signed a license agreement with Rambus covering Direct RDRAM. (CX 1646 at 1-20). Micron agreed to pay a royalty rate up to 2% on next generation RDRAM and included a provision to buy down the royalty rate. (CX 1646 at 11).

499. Micron decided to sign a license agreement for Direct RDRAM because "we felt that with Intel's endorsement, that there would be a customer base that would use the product, and we needed to be in a position to make whatever product that the customer decided that they were going to use for their platforms." (Appleton, Tr. 6346-47).

500. In July 1997, Siemens signed a license agreement with Rambus covering RDRAM. (CX 1617 at 1-22; CX 2088 at 62 (Tate, Infineon Trial Tr.)).

2. Intel and RDRAM Royalty Rates

501. Intel wanted to keep the cost of RDRAM low so that DRAM vendors would be motivated to build RDRAM. (MacWillaims, Tr. 4849-50).

502. Intel's contract with Rambus capped the royalty rate that Rambus could charge for RDRAM technology at two percent. (CX 2634 at 3-4).

503. Intel sought to persuade Rambus to keep its royalty rates low throughout the 1996-1998 time frame. (CX 936 at 1; CX 912 at 2; CX 952 at 2; Farmwald, Tr. 8404).

504. In September 1997, Rambus CEO Geoffrey Tate and Rambus Vice President David Mooring met with Intel executives Gerry Parker and Pat Gelsinger. (CX 952 at 1). Intel requested that Rambus, among other things, lower its RDRAM royalties even further to help overcome DRAM maker resistance to producing RDRAM devices. (CX 952 at 2). Intel explained that if Rambus did not lower its RDRAM royalties, this could cause DRAM makers "to find alternate solutions to avoid paying rambus a royalty" and could cause Intel to "rearchitect things to be completely different if necessary." (CX 952 at 2).

505. In October 1997, Rambus CEO Geoffrey Tate had a meeting with Pat Gelsinger, the senior Intel executive responsible for the Rambus relationship. The purpose of the meeting was to follow up on Gelsinger's earlier request that Rambus "lower our rdram royalties to <0.5%," and his suggestion that if Rambus failed to do so DRAM makers would insist on developing alternatives to RDRAM. (CX 961 at 1).

506. The October 1997 Rambus-Intel meeting focused in part on the extent to which DDR had "GAINED ground" with PC manufacturers and thus was a "threat" to RDRAM. (CX 961 at 2-3). Intel believed that at least one DRAM maker was promoting

DDR because of Rambus's royalty rates on RDRAM. (CX 961 at 5).

507. Intel did not believe that there was a problem with Rambus's business model other than the fact that many of the DRAM manufacturers disliked it. (CX 1016 at 3-4).

3. Design, Manufacture, and Supply of Memory Architectures by Micron and Other DRAM Manufacturers

508. From approximately 1996-1999, some companies, such as Micron and Hynix felt the DRAM industry was developing different memory architectures for different market segments. Companies planned to use RDRAM as main memory in mid-range and high end personal computers; DDR as main memory in servers and for graphic applications; and SyncLink as the possible next generation main memory in PCs. (CX 2718 at 45; Lee, Tr. 6727-28; CX 2297 at 3, 81).

509. Hyundai made commitments to deliver RDRAM to customers based on customer needs. (CX 2303 at 7; Tabrizi, Tr. 9164-66). However, in 1998, Hyundai's RDRAM production commitments were not met. (Gross, Tr. 2327-29).

510. Compaq planned to transition to RDRAM because of Intel's roadmap and planned to introduce RDRAM throughout its product line. (Gross, Tr. 2318, 2326-27).

511. Micron's CEO Steve Appleton, testified that Micron devoted many resources to developing RDRAM after Micron signed a license for Direct RDRAM in 1997. (Appleton, Tr. 6354-57). He stated that Micron formed a large design team to work on RDRAM and offered the team cash incentives to meet certain milestones. (Appleton, Tr. 6355-56).

512. In October 1998, however, Micron proposed to other DRAM manufacturers that they agree to a "common roadmap" that the manufacturers would then provide to chipset companies and PC original equipment manufacturers ("OEMs"). (RX 2191 at 1; RX 2192 at 3; Soderman, Tr. 9354). The "main target" of such a joint roadmap would be to remove the "current uncertainty about the supply situation" among the chipset companies and PC OEMs. (RX 2191 at 1). A proposed joint market forecast was later circulated to numerous DRAM manufacturers by Micron. (RX 1423 at 1-2).

513. In an April 1999 email exchange among Micron Vice President Bob Donnelly, Micron DRAM Marketing Manager Jeff Mailloux, and Micron JEDEC representatives Kevin Ryan and Terry Lee, an article was attached describing Samsung's plans to produce as much as forty million Rambus devices in 1999. (RX 1444 at 3). In response, Ryan complained that Samsung had "broken ranks with the other suppliers and sold their soul to the devil." (RX 1444 at 1). One of the recipients of the email, Mike Seibert, responded that "these guys [Rambus] are big trouble for us all. If this thing gets into an oversupply mode with RDRAM things could get really ugly." (RX 1444 at 1). Seibert then asked Micron Vice-President Bob Donnelly if Samsung understood "what the Rambus/Intel biz model will do to our autonomy?" (RX 1444 at 1). Vice-President Donnelly responded that he had "certainly made the point with the officers that Intel . . . ultimately could control the DRAM industry." (RX 1444 at 1).

514. In April 1999, Micron completed its higher 144Mb Rambus design and taped out the part, meaning Micron sent it off for fabrication. (CX 2735 at 24, 29; Lee, Tr. 6744-45). Micron indicated that it expected to release its 144Mb samples in June 1999. (CX 2735 at 31). However, according to an Intel analysis of Micron's RDRAM performance as of May 1999, "[t]echnically, they are well behind." (RX 1453 at 1). As a result, Intel felt, Micron was only "marginally able to ship anything at all in '99." (RX 1453 at 1).

515. Intel concluded in May of 1999 that Micron's plan was intended to "create as much turmoil to prevent rdram as possible." (RX 1453 at 1). The Intel analysis stated:

> *Marketing* - they [Micron] are aggressively rallying the industry on alternate technologies. They are clearly driving the Sdram-133 alternatives, they are strongly driving ddr and the only player left driving sync-link. Their advertising implies that the rest of the industry is blindly following the Intel roadmap (sheep, communism etc). Should make you mad...
>
> *Relationship* - we've tried to broker a deal with rambus (fixing contract in area of ip pooling, royalties and marketing) and per earlier mails, with their advertising and aggressive drive to alternatives, they pissed rambus off enough that any hope of an agreement is pretty dead. They have also ignored our attempts to work with them on enabling, design reviews, roadmap alignment etc.

(RX 1453 at 1).

516. By October 1999, an Intel manager explained to Intel's Peter MacWilliams, "[s]o far all our discussions with Appleton have had zero benefit for us. . . . [w]e have gone out of our way to help them resolve Rambus contract issues and in return we have gotten nothing but deception. Micron is working very hard to do everything against RDRAM." (RX 1515 at 2).

4. Cost Issues Associated With RDRAM

517. In the 1998 time frame, DRAM manufacturers estimated that RDRAM would be more costly to produce than other

DRAMs. (Gross, Tr. 2364-66). This impression had come from DRAM suppliers and Intel. (Gross, Tr. 2367-68).

518. Hyandai executive Tabrizi admitted at trial that in October 1998, Hyundai gave RDRAM production forecasts to Intel that were deliberately inflated. "Intel was not happy with our ramp up, so we gave them a very optimistic number on our side. (Tabrizi, Tr. 9092; *see also* RX 1295 at 1 (internal Hyundai email, copied to Tabrizi, that states that, from the perspective of the Hyundai America marketing group, "we can overstate our Direct Rambus production so Intel can feel we are more aggressive on the ramp up.")).

519. In a February 2000 email asking Micron to supply it with RDRAM, Dell similarly stated that it was "committed to Rambus" but that its ability to incorporate Rambus devices in its PCs was "clearly limited by supply." (RX 1560 at 1). Looking ahead to the second half of 2000, Dell projected that with lower pricing, up to forty percent of its market demand would be satisfied with RDRAM technology. (RX 1560 at 1).

520. Several factors might have contributed to the high cost of producing RDRAM including "the packaging, handlers, burn-in equipment, die size, licensing, and test. Some of these areas will require the purchase of new manufacturing equipment, and some areas have an inherently higher manufacturing cost." (CX 2716 at 1; CX 2083 at 132-33). However, this does not explain why DDR SDRAM prevailed in the marketplace in lieu of RDRAM, for all of these issues were present in connection with the product introduction of the DDR device, as Micron CEO Appleton confirmed in an analyst call in September 2002. (*See* RX 2067 at 7).

521. As Craig Hampel, Technical Director of Rambus explained, test cost analyses that focus on capital expenditures depend in large part on the volume of devices tested. Assuming equivalent volume production of the RDRAM and SDRAM

devices, test costs would be at least equivalent, and because of the high speeds at which the Rambus device could be tested, could even be less for the RDRAM devices. (Hampel, Tr. 8703-04).

522. Dell understood that the RDRAM cost premium inhibited the development and production of RDRAM. (CX 2180 at 1, 4).

523. As Compaq executive Gross testified, and as Compaq's documents show, OEMs were facing a shortage of RDRAM created because the "suppliers have not invested to support current Rambus demand for 1999." (RX 1287 at 4; Gross, Tr. 2346).

524. Intel had concerns about the cost of RDRAM. (CX 974 at 1). In or around 1998, Intel had concerns regarding whether the cost of manufacturing RDRAM would ever be comparable to the cost of making SDRAM because the price of SDRAM had dropped significantly. (CX 2541 at 1; CX 2887 at 1; RX 1532 at 2).

525. Elpida Memory, Inc. ("Elpida") expected lower projected RDRAM costs than DDR costs in 2002 and 2003. (RX 1762 at 42). The same Elpida presentation described RDRAM as the most competitive leading process available. (RX 1762 at 43).

5. Actions by DRAM Manufacturers

526. In September 1996, Hyundai executive and SyncLink Consortium chairman Farhad Tabrizi wrote an email that expressed a concern that "the real motive of Intel is to control DRAM manufacturers . . . ." (RX 778 at 1). According to Tabrizi, Intel's actions would give it "control of DRAMs and other CPU makers. We will become a foundry for all Intel activities and if Intel would like and desires to do business with us then we may get a small share of the their total demand." (RX 778 at 1). Tabrizi concluded his email stating: "I urge you to please educate others

and get their agreement to say 'NO TO RAMBUS AND NO TO INTEL DOMINATION.'" (RX 778 at 1).

527. Tabrizi sent this email to Jim Sogas at Hitachi, for comments. (RX 778 at 1; Tabrizi, Tr. 9035, 9037-38).

528. In December 1996, at a SyncLink Consortium meeting attended by various manufacturers, Tabrizi stated that "[m]any suppliers are paranoid over the prospect of a single customer, e.g., Intel, having control of market. We can't resist such a possibility individually. We need some united strategy." (RX 808 at 2).

529. At that same meeting, the assembled manufacturers agreed to hold a meeting of DRAM manufacturer executives in Japan in January 1997. (Tabrizi, Tr. 9041). Prior to the meeting, Tabrizi sent an email to other DRAM manufacturers that stated that the "Intel decision to go on a Rambus route was pure political and domination and control over the DRAM suppliers and not technical." (RX 802 at 3; Tabrizi, Tr. 9041-42). He then stated: "As I have mentioned many times before, Intel does not make DRAMs, we do. And if all of us put our resources together, we do not have to go on this undesirable path. The path of control and domination by Intel." (RX 802 at 3). He urged the DRAM manufacturers to "stick together on this matter." (RX 802 at 3; Tabrizi, Tr. 9042-43).

530. Tabrizi's January 1997 presentation also stated that if Rambus became the next generation memory solution, "ALL DRAM COMPANIES WILL BECOME FOUNDRIES for a single source CPU manufacturer." (RX 849 at 44). The phrase "single source CPU manufacturer" was a reference to Intel. (Tabrizi, Tr. 9046).

531. Micron engineer Terry Lee participated in the January 1997 DRAM executive meeting; his notes reflect that Siemens stated that "[c]ontrol concerns are realistic." (CX 2250 at 2; Tabrizi, Tr. 9047-48). Lee's notes were later made available to all members of the SyncLink Consortium (which was renamed the

"SLDRAM Consortium" around this time). (Tabrizi, Tr. 9050; RX 855 at 1).

532. After the January 1997 DRAM executive meeting, Tabrizi set up an email "reflector" so that the DRAM supplier executives could communicate with each other. (Tabrizi, Tr. 9052-53; RX 938 at 1).

533. In February 1998, Jeff Mailloux of Micron wrote an email to Tabrizi stating that Mailloux had spoken to a reporter for an industry publication called EE Times. (RX 1105 at 1). Mailloux stated that "I told him that at any density, and any process that is available in 1999, RDRAM is at least 30% cost adder for Micron," and then encouraged Tabrizi to call the reporter with Hyundai's views. (RX 1105 at 1).

534. Two months later, Mailloux sent another email to Tabrizi, attaching an article in an industry publication that had been written by Tabrizi's boss at Hyundai, Mark Ellsberry. (RX 1155 at 1; Tabrizi, Tr. 9055-56). His email states, "Mark seems to give a message at the end here, he only refers to DDR as a 'long shot' and does not even mention SLDRAM. Hope Hyundai has not caved in to the 'dark side.'" (RX 1155 at 1).

535. In April 1998, Bert McComas, an industry consultant, gave an exclusive seminar for DRAM manufacturers about Intel's selection of RDRAM. (RX 1138 at 1; Tabrizi, Tr. 9061-62). McComas pre-cleared his seminar invitation and list of topics with Tabrizi. (Tabrizi, Tr. 9064).

536. McComas's invitation asked its recipients not to forward the invitation to Rambus or Intel. (RX 1138 at 1).

537. During his April 1998 seminar presentation to the DRAM manufacturers, McComas stated that a manufacturer that chose to build RDRAMs was making a "guaranteed bad bet for margin enhancement," and he stated that RDRAM deepens the

manufacturer's financial dilemma. (RX 1482 at 12, 26). As a "possible strategy[y]," McComas suggested that DRAM manufacturers "[t]ape out but do not fully productize or cost reduce" the RDRAM device, in an effort to "resist popular deployment" of RDRAM. (RX 1482 at 34-35).

538. After the seminar, McComas accepted an invitation to speak at the next SLDRAM Consortium Executive Meeting, so-called because company executives attend in addition to engineers and marketing personnel. (Tabrizi, Tr. 9066-68). In an April 17, 1998 email extending the invitation, Roberto Cartelli of Texas Instruments wrote to McComas, "I personally believe that your story on Intel and its relationship to Rambus, is an excellent 'case for action' story to stimulate discussion among industry executives." (RX 1166 at 1; Tabrizi, Tr. 9068).

539. McComas spoke at the June 25, 1998 SLDRAM Executive Summit about the problems faced by DRAM manufacturers. One of the tactical issues he identified was how to "Manage Price Competition, Profitability." (RX 1188 at 1). He also talked about how manufacturers could "Respond to the Strategic Threat of Intel/Rambus," and he asked the question, "Who will control the DRAM industry?" (RX 1188 at 1). McComas stated that "Intel/Rambus are using your money to take control of the DRAM industry" and that Intel would "[o]rchestrate early oversupply situation," and he emphasized that "[f]ragmented competition undermines all DRAM manufacturers." (RX 1188 at 2, 6; Tabrizi, Tr. 9073).

540. Another industry consultant, Victor de Dios, also gave a presentation at the June 25, 1998 SLDRAM Executive Summit. (Tabrizi, Tr. 9071-72). De Dios told the assembled executives that "many of the problems are industry problems, not company problems. Competition will not resolve them." (RX 1204 at 4 (capitalization omitted)).

541. During his presentation at the June 1998 "Executive Summit," McComas suggested that the DRAM manufacturers share their RDRAM production plans to determine whether there would be a demand-supply imbalance. (Tabrizi, Tr. 9073-74).

542. In an August 1998 email to Tabrizi, McComas sent a draft message to DRAM manufacturers which stated that "[d]uring the critical production ramp-up phase of Direct Rambus, DRAM vendors will need a constant flow of information to help make wise decisions and to walk the fine line between a pleasant shortage and a disastrous over-supply." (RX 1232 at 1).

543. Tabrizi agreed that a shortage of RDRAM would please DRAM manufacturers because "[p]rices go up." (Tabrizi, Tr. 9077).

544. The PC OEMs recognized that for RDRAM to succeed, output of RDRAM had to increase. They tried to influence the DRAM manufacturers to increase RDRAM output. (RX 1287 at 4 ("Intel and major users have been trying to influence improve [sic] RDRAM output")). As Gross of Compaq testified, Intel, Compaq, and other PC OEMs were trying to influence DRAM manufacturers to increase output of RDRAM and to align roadmaps with Intel's roadmap. These OEMs wanted an RDRAM production ramp-up so that they would have sufficient availability and lower RDRAM prices. (Gross, Tr. 2318-20).

545. It was important to Intel and to the PC OEMs that the DRAM vendors increase the volume of RDRAM because the highest volume parts have a cost advantage. (RX 1532 at 1).

546. In response, DRAM manufacturers agreed to manufacture RDRAM in larger volume. For example, in 1998, Hyundai committed to produce 30,000 RDRAM units for Compaq. (RX 1302 at 6). Similarly, Micron committed to produce 15,000 RDRAM units for Compaq. (RX 1302 at 6). Neither company, however, met these commitments. (Gross, Tr. 2327-29).

According to Compaq, the DRAM manufacturers would not "increase their output at the rate at which we needed to support our systems." (Gross, Tr. 2345-46).

547. Tabrizi, in 1998, believed that Intel would not change course unless RDRAM failed to obtain market penetration. (Tabrizi, Tr. 9082-83). He admitted that one way to cause RDRAM to fail to obtain market acceptance was if the OEMs were convinced that even if volumes went up, prices would not fall. (Tabrizi, Tr. 9083). If the OEMs were convinced of this, they would not adopt RDRAM. (Tabrizi, Tr. 9083).

548. In the fall of 1998, Hyundai gave RDRAM price projections to its customers that were significantly higher than those reflected in its internal pricing documents. (Tabrizi, Tr. 9085-90; RX 1280; RX 1293A). "Intel was telling everybody [that RDRAM is] only going to be a 5 percent premium . . . . I wanted to make sure my OEM knows it's going to cost them more than 5 percent . . ." (Tabrizi, Tr. 9091-92).

549. A report prepared by an Infineon engineer about an October 1998 meeting reportedly attended by Tabrizi, along with engineers from Micron and Infineon, states that "[a]ccording to Farhad Tabrizi, Hyundai has given Rambus ASP projections for end of next year of 2 to 3 times of todays SDRAM prices; they also gave to Intel a production projection of three times their actual plans => They encourage every DRAM manufacturer to do the same in order to let Intel not generate a Rambus oversupply." (RX 2192 at 2). Tabrizi denied at trial that he had made the statements attributed to him in the Infineon trip report. (Tabrizi, Tr. 9097).

550. In January 1999, Desi Rhoden sent a proposal to all of the major DRAM manufacturers regarding the transformation of the former SyncLink Consortium (by then called "SLDRAM Inc.") into a marketing-oriented organization called Advanced Memory Inc. ("AMI2"). (RX 1373 at 1-3). Rhoden became the

President and Chief Executive Officer of AMI2. (Rhoden, Tr. 260, 696-97, 1235). Rhoden stated that the focus of the new organization would be to "co-ordinate instead of developing new technology." (RX 1373 at 3). He also stated that "[i]n the DRAM industry, we are clearly stronger together than we are individually." (RX 1373 at 1).

551. In a July 1999 email, Mario Martinez of Hyundai recommended to Tabrizi and others at Hyundai that "[w]ith Samsung building significant amounts of product, we need to work with them to limit the supply in the market, otherwise we both will be competing for market share which will result in an oversupply. We have to meet with Samsung and discuss our and their production plan, TAM analysis and targeted market share." (RX 1487 at 4; Tabrizi, Tr. 9103).

552. Another Hyundai employee responded in the same email: "[I] have connection in samsung, if i know, what time you are available, i will try setup meeting with key persion [sic] in samsung in seoul korea. [A]nd i will try persuade them. [A]ctually they also have same idea for rambus business compare with you." (RX 1487 at 4; Tabrizi, Tr. 9104).

553. Tabrizi admitted at trial that he had told Sang Park, then the President and Chief Operating Officer of Hyundai, that he wanted to "kill" Rambus and force RDRAM from the market. (Tabrizi, Tr. 9105-07). Tabrizi subsequently testified that what he meant by "killing" Rambus was really just "Rambus suicide, [with] me watching on the sideline." (Tabrizi, Tr. 9109). In his June 2000 email to Park, Tabrizi stated: "[i]f Intel does not invest in us, I really want to ask you to let me go back to my old mode of RDRAM killing. I think we were very close to achieving our goal until you said we are absolutely committed to this baby." (RX 1661 at 2).

554. Gross of Compaq subsequently testified that because the price of RDRAM did not decrease and because Compaq did not

believe that it would decrease in the future, Compaq decided to abandon its plans and to shift to DDR. (Gross, Tr. 2339).

555. Similarly, Advanced Micro Devices ("AMD") shelved plans to adopt RDRAM because, based on what they were told by DRAM manufacturers, it was clear that DDR, not RDRAM would become a commodity product. (Polzin, Tr. 4013).

556. By May 2000, the situation had not improved, and Dell was considering moving into "a low key Rambus mode." (RX 1636 at 1). The Dell "message" was "pretty straightforward":

> Dell has booked our products over the last year around the assumption that RDRAM prices would decline and close on SDRAM. This would help us create demand . ... The memory vendors have shown no desire to drop prices, therefore we are reevaluating our strategies ... so the message to them is drop prices or we will continue to decrease our RDRAM forecasts and we will architect next generation systems around DDR ... we will give the memory vendors till the end of May to reply to our request ... if they still have no desire to drop prices, we should push ahead rearchitecting chipsets around DDR.

(RX 1636 at 1).

557. RDRAM failed to command significant market share despite the fact that it was considered by some to be the "best solution." (RX 1762 at 5). As Peter MacWilliams of Intel put it:

> [redacted]

(MacWilliams, Tr. 5075 (*in camera*)).

558. Subsequently, in a November 26, 2001 email, a Micron manager named Kathy Radford described the efforts of Infineon and Samsung to raise DDR prices, and stated that Micron intended to try to raise its prices to all of the OEM customers. (RX 1922A at 1). Radford then reported that "[t]he consensus from all suppliers is that if Micron makes the move, all of them will do the same and make it stick." (RX 1922A at 1).

559. Prices did, in fact, increase in the months after Radford's email. On March 1, 2002, [redacted] (RX 1991 at 1 (*in camera*)).

6. The DRAM Industry's Approach to Addressing RDRAM Problems

560. Intel and Rambus executives discussed ways to fix Rambus's relationship with the DRAM manufacturers. (MacWilliams, Tr. 4871-72). Rambus "seemed to be sensitive to the fact that they needed to fix" problems with DRAM manufacturers. (MacWilliams, Tr. 4873).

561. In 1998, Intel continued its work to make RDRAM a market success by investing in DRAM companies that developed and supplied RDRAM. (CX 1006 at 1; CX 2522 at 2-3).

562. Intel did not succeed in mending the relationship between Rambus and the DRAM manufacturers. (MacWilliams, Tr. 4874).

7. By 1998 the Rambus-Intel Relationship Was Deteriorating

563. On April 14, 1998, Rambus CEO Geoffrey Tate and Chairman William Davidow met with Pat Gelsinger of Intel to discuss Intel's concerns about Rambus. (Farmwald, Tr. 8402; CX 1016 at 1; CX 2109 at 175-76 (Davidow, Dep.)). The basic message of the meeting was that in the intermediate term Intel would continue to support RDRAM, but Intel might support a competing architecture for the next generation. (CX 1016 at 1-4).

564. After the April 14, 1998 Rambus-Intel meeting, Tate began strategizing about how to address Intel's announcement that it would compete with Rambus. (CX 1016 at 1-4).

565. On April 15, 1998, Farmwald responded to Tate's concerns about Intel's commitment to RDRAM emailing: "I'm not even sure we want to agree to work together on the next generation memory interface." (Farmwald, Tr. 8406-07; CX 1021 at 1).

566. On April 16, 1998, Rambus Chairman William Davidow responded to Farmwald's email by urging a more measured approach. (Farmwald, Tr. 8407; CX 1022 at 1). Davidow suggested that Rambus "try to negotiate something" with Intel. (CX 1022 at 2).

8. Technical Problems and Product Delays With RDRAM

567. During this period, the Camino Chipset, also called the Intel 820 Chipset, "was the first chipset that Intel was developing to interface between their processor and direct Rambus." (MacWillaims, Tr. 4853; Tabrizi, Tr. 9166, 9185). The Camino Chipset was intended to interface exclusively with RDRAM. (Tabrizi, Tr. 9185-86).

568. In the second half of 1998, Intel encountered electrical issues with RDRAM. (RX 1532 at 2; MacWilliams, Tr. 4852-53). Technical problems with RDRAM forced Intel to delay the Camino Chipset launch several times. (MacWilliams, Tr. 4852-53; Tabrizi, Tr. 9185).

569. Similarly, the design and ramp up phases of DDR SDRAM's launch experienced delays and difficulties. (Reczek, Tr. 4349-51 (transition to DDR was a major change, and Infineon had to implement three major redesigns before it could achieve

acceptable performance); Shirley, Tr. 4208-09 ([redacted]) (*in camera*)).

570. In April 1999, Intel's microprocessor rival, AMD, suspended development work on its RDRAM product due to continuing bad news about RDRAM. (CX 2158 at 1-2). Steven Polzin, of AMD, testified that the information regarding RDRAM costs and yields came from what he was hearing from the memory manufacturers. (Polzin, Tr. 4013). In late summer or fall of 1998, AMD shifted its focus to DDR because AMD believed Rambus was going to fail as a commodity part, and that ultimately even Intel would have to go DDR. (Heye, Tr. 3704-05, 3799).

571. In May 1999, Intel's customers were skeptical that the cost and availability issues with RDRAM could be resolved although some were waiting to see progress. (CX 2529 at 1; MacWilliams, Tr. 4884)).

572. In May 1999, Intel considered adding DDR SDRAM to Intel's server memory roadmap because it was concerned that RDRAM would not achieve the cost points in time to be competitive for the server products. (MacWilliams, Tr. 4883-84; CX 2529 at 1).

9. Intel's Announcement That It Would No Longer Support RDRAM

573. By mid-October 1999, Intel's road map included SDRAM and DDR SDRAM solutions as well as RDRAM. (CX 2540 at 1).

574. In late October 1999, Intel told Rambus that it wanted to have a comprehensive review of their business relationship. (CX 2887 at 1).

575. Intel announced in its October 26, 1999 letter to Rambus that its chipset roadmap now included alternatives to RDRAM. (CX 2541 at 2; CX 2887 at 2-3).

576. In June 1999, Intel publicly ceased its exclusive support of RDRAM and announced that the Pentium III chipset would support SDRAM. (Tabrizi, Tr. 9201-03; CX 2338 at 57 (*in camera*)).

577. This was the first time Intel indicated that SDRAM could compete with RDRAM as the interface with Pentium III. (Tabrizi, Tr. 9201-03).

578. In August 1999, Intel confirmed that it would provide support for SDRAM in the Pentium III chipset. (Tabrizi, Tr. 9201-03).

579. After Intel announced its support of SDRAM, Rambus's percentage of market penetration dropped because customers could choose between SDRAM and Rambus's technologies. (CX 2338 at 57 (*in camera*); Tabrizi, Tr. 9203-08).

580. During 1999 and 2000, Intel revised downward its estimates for the total available market for RDRAM multiple times. (CX 2338 at 79 (*in camera*)).

581. Intel reduced its estimates for the total available market for RDRAM the second and third quarters of 2000. (CX 2338 at 79 (*in camera*); Tabrizi, Tr. 9193-97).

582. Micron never introduced RDRAM into the market for commercial sale. (Appleton, Tr. 6371-74).

583. On September 2001, Micron Vice-President Sadler [redacted] (RX 1883 at 1 (*in camera*)).

584. As projections for RDRAM declined in the 1999-2000 time frame, the anticipated market share shifted to SDRAM and DDR SDRAM. (Tabrizi, Tr. 9214-15).

585. Samsung, the world's largest DRAM producer, began commercialization and full production of RDRAM. (Appleton, Tr. 6373).

586. In February 2001, nearly a year and half later, Intel was still announcing that its memory strategy was to shift from SDRAM to RDRAM for desktop space. (RX 1762 at 4). According to Intel's presentation at the Intel Developer Forum, Spring 2001, RDRAM was the best solution, the best technology for the Intel Pentium 4 Processor Platform, and "RDRAM Remains the Primary Desktop Memory Solution." (RX 1762 at 5). In its summary, Intel stated, "RDRAM Provides the Best Pentium 4 Processor Platform Now and in the Future." (RX 1762 at 24). According to Pete MacWilliams of Intel, this statement accurately summarized Intel's position as of February 2001. (MacWilliams, Tr. 4935).

VI. EIA/JEDEC PATENT POLICY

A. Good Faith Obligations

587. Complaint Counsel rely on the EIA Legal Guides, Section C, for their contention that JEDEC participants were required to act in good faith. (CCPFF 310 *citing* CX 204, CX 206).

588. The EIA Legal Guides Section C, labeled "Basic Rules For Conducting Program," states that "[a]ll EIA standardization programs shall be conducted in accordance with the following rules: (1) They shall be carried on in good faith under policies and procedures which will assure fairness and unrestricted participation; . . ." (CX 204 at 5; CX 202 at 6 (earlier version of same document)).

589. Section C continues by requiring that participation be extended to all technically qualified members of the industry and that programs serve the public interest objectives of EIA. (CX 204 at 5). The balance of Section C prohibits collusion and price fixing and limits representatives to technical personnel without marketing responsibilities. (CX 204 at 5).

590. The EIA Legal Guides explicitly address patents in Section B, which states that "[s]tandards are proposed or adopted by EIA without regard to whether their proposal or adoption may in any way involve patents on articles, materials, or processes." (CX 205 at 4).

591. Given the context of Section C, especially when compared with Section B, it is apparent that the "good faith duty" is not directed to individual members, but rather is a general directive to the administrators who "conduct" the EIA's standardization activities, directing them to adopt "policies and procedures which will assure fairness and unrestricted participation." (*See* CX 204 at 5).

592. Complaint Counsel rely on "An Overview of JEDEC Patent Policy" written by John Kelly and dated March 26, 2002 to further support their contention that a good faith duty required Respondent to disclose intellectual property. (CCPFF 310 *citing* CX 449).

593. This 2002 Overview is not persuasive in interpreting JEDEC patent policy during the time period at issue as it was written after the fact and cites JEDEC Manual 21K, published after Rambus withdrew from JEDEC. (*See* CX 449 at 1-2).

594. No contemporaneous documents were provided by Complaint Counsel to support their contention that JEDEC members had a duty of good faith or a duty to comply with the spirit of the patent policy. (*See* CCPFF 310-315).

595. At trial, JEDEC members testified that there was a good faith duty imposed on members of JEDEC. (J. Kelly, Tr. 1841 ("companies need to participate in the process openly and honestly and fairly and in good faith and not in bad faith, because bad faith undermines the confidence of everyone in the process."); G. Kelley, Tr. 2397 ("my mind translated [good faith] to fair treatment for all members"); Rhoden, Tr. 305-06 ("The term 'good faith' as used in [the Legal Guides] is that the people . . . are coming under the premise that they're going to . . . work toward the benefit of the end user of the industry itself, and operating in good faith means that you would expect other people to do the same thing."); Sussman, Tr. 1330 ("Good faith, we're all competitors, we're all about ready to dice each other in the marketplace, but seeing we're talking about or about to talk on intellectual property, I trust you to do something, and I expect that same set of trust back.")).

596. Despite their trial testimony, some JEDEC members, including those in leadership positions, did not always conduct themselves in a manner consistent with a duty to disclose intellectual property or to act in good faith. (*See* F. 686-717). For example, G. Kelley, IBM representative and JC 42.3 Committee Chair, on multiple occasions, indicated that IBM would not disclose patents to JEDEC (F. 691-93) and JEDEC Chairman Rhoden failed to disclose a patent application on which he was listed as an inventor. (F. 711-17).

597. Viewing the trial testimony in conjunction with the conduct of JEDEC members and leaders, there is not sufficient evidence to find a duty of good faith imposed on participants of JEDEC. (F. 587-96).

B. Open Standards

598. The goal of JEDEC is to develop open standards. (CX 419; Rhoden, Tr. 301, 536; J. Kelly, Tr. 1776-78, 1782, 1787).

599. Open standards may, and often do, include patented features or technologies. The EIA Legal Guides, which governed JEDEC, provide that "[s]tandards are proposed or adopted by EIA without regard to whether their proposal or adoption may in any way involve patents on articles, materials, or processes." (*See* CX 204 at 4; CX 206 at 6; J. Kelly, Tr. 1829-30).

600. JEDEC Chairman Rhoden testified that "open standards inside of JEDEC essentially means that we want to set up a mechanism where everyone can participate that wants to, and in the end, the end product is then available to everybody in the world. So, open participation, open accessability, if you will." (Rhoden, Tr. 300-01).

601. JEDEC does not include known patented material in JEDEC standards without written assurances from the owner of the intellectual property that it will grant licenses on reasonable and nondiscriminatory ("RAND") terms to all applicants. (CX 203A at 11; CX 208 at 19; JX 54 at 9; CX 2191 at 8; *see also* F.1536-81).

602. JEDEC does not determine what is a reasonable royalty rate because JEDEC does not "have the expertise to be able to determine what's commercially reasonable in the context of any industry, no less semiconductors. . . That expertise resides in the industry. So, that's why in the first instance we leave it to the parties themselves to work out what's reasonable." (J. Kelly, Tr. 1882-83; *see also* CX 2089 at 174-75 (Meyer, Infineon Trial Tr.)).

603. Determination of a reasonable royalty rate is left to negotiation and market forces or the courts. (CX 2089 at 174-75 (Meyer, Infineon Trial Tr.); J. Kelly, Tr. 1882-83, 2073-74).

604. Hans Wiggers, a JEDEC representative from Hewlett-Packard in the early to mid-1990's, testified that it was his understanding that the JEDEC patent policy was that, as long as a

company licensed its patents after they issued on RAND terms to all interested parties, the company had no obligation to disclose its intellectual property. (Wiggers, Tr. 10591).

605. In 1996, in its correspondence to the Commission regarding the *Dell* case, EIA recognized that by "allowing standards based on patents, American consumers are assured of standards that reflect the latest innovation and high technology the great technical minds of this country can deliver. . . . There is a positive and pro-competitive benefit to incorporating intellectual property in standards." (RX 669 at 2-3).

C. Manuals

1. JEP 21-H

606. JEDEC Manual of Organization and Procedure 21-H ("JEP 21-H"), dated July 1988, which was still in effect when Rambus joined JEDEC in 1992, contains the following legend: "Electronic Industries Association. Engineering Department." (CX 205 at 1).

607. JEP 21-H includes in Appendix D a non-liability disclaimer to be incorporated into JEDEC standards. This disclaimer states that "JEDEC standards are adopted without regard to whether or not their adoption may involve patents on articles, materials or processes. By such action JEDEC does not assume any liability to any patent owner, nor does it assume any obligation whatever to parties adopting the Standards." (CX 205 at 20).

608. JEP 21-H states that "[a]ll meetings of the JEDEC Solid State Products Engineering Council and its associated Committees, Subcommittees, Task Groups and other units shall be conducted within the current edition of EIA Legal Guides adopted by the EIA Board of Governors and incorporated herein by reference." (CX 205 at 14).

609. The 21-H Manual does not provide any guidance regarding intellectual property rights or an obligation to disclose patents, patent applications, or the intent to file patent applications. (*See* CX 205).

2. JEP 21-I

610. JEDEC Manual of Organization and Procedure 21-I ("JEP 21-I"), dated October 1993, contains the following legend: "Electronic Industries Association. Engineering Department" and displays the trademarks of both JEDEC and EIA. (CX 208 at 1).

611. Section 9.1, JEP 21-I states: "[a]ll meetings of the JEDEC Solid State Products Engineering Council and its associated committees, subcommittees, task groups and other units shall be conducted within the current edition of EIA legal guides adopted by the EIA Board of Governors and incorporated herein by reference." (CX 208 at 18).

612. Section 9.3, JEP 21-I discusses the use of patented products in EIA Standards as follows:

> EIA and JEDEC standards and nonproduct registrations (e.g., package outline drawings) that require the use of patented items should be considered with great care. While there is no restriction against drafting a proposed standard in terms that include the use of patented item [FN 1] if technical reasons justify the inclusion, committees should ensure that no program of standardization shall refer to a product on which there is a known patent unless all the relevant technical information covered by the patent is known to the formulating committee[,] subcommittee, or working group. If the committee determined that the standard requires the use of

> patented items, then the committee chairperson must receive a written assurance from the organization holding rights to such patents that a license will be made available without compensation to applicants desiring to implement the standard, or written assurance that a license will be made available to all applicants under reasonable terms and conditions that are demonstrably free of any unfair discrimination. Additionally, when a known patented item is referred to in an EIA/JEDEC standard, a cautionary note, as outlined in this document, shall appear in the EIA/JEDEC standard (see 9.3.1.).
>
> All correspondence between the patent holder and the formulating committee, subcommittee, or working group, including a copy of the written assurance from the patent holder discussed above, shall be transmitted to the EIA Engineering Department and the EIA General Counsel at the earliest possible time and, in any case, before the standard is otherwise ready for subcommittee or committee ballot circulation. (See the Style Manual, EP-7-A, 3.4 for the required language in an EIA Standard that cites a product with a known patent.)
>
> [FN 1]: For the purpose of this policy, the word "patented" also includes items and processes for which a patent has been applied and may be pending.

(CX 208 at 19).

613. Section 9.3 of JEP 21-I describes the requirements of incorporating known patented products in EIA/JEDEC standards

– namely, that all technical information should be known and RAND assurances obtained. (CX 208 at 19).

614. Although this section, through a footnote, defines "patented" to include pending patents, the section also expressly recognizes that it only applies to "known patents." (CX 208 at 19).

615. This section does not impose an obligation to disclose intellectual property. Rather, it explains the procedure and information necessary for including a known patent into a standard. (CX 208 at 19).

616. Section 9.3.1, JEP 21-I states:

> *9.3.1 Committee Responsibility Concerning Intellectual Property*
>
> The Chairperson of any JEDEC committee, subcommittee, or working group must call to the attention of all those present the requirements contained in the EIA Legal Guides, and call attention to the obligation of all participants to inform the meeting of any knowledge they may have of any patents, or pending patents, that might be involved in the work they are undertaking. Appendix E (Legal Guidelines Summary) provides copies of viewgraphs that should be used at the beginning of the meeting to satisfy this requirement. Additionally, all participants must be asked to read the statement on the back of each EIA Sign-in/Attendance Roster.

(CX 208 at 19).

617. Section 9.3.1 of JEP 21-I is ambiguous because it refers to the EIA Legal Guides immediately before and immediately

after mentioning an "obligation to inform the meeting of . . . patents, or pending patents." (CX 208 at 19). The EIA Legal Guides to which this section refers, however, do not support such an obligation. (*See* CX 208 at 26-29; CX 204).

618. To satisfy the requirement to call attention to the obligation to disclose patents and patent applications, section 9.3.1 refers to Appendix E and the EIA sign-in/attendance roster. (CX 208 at 19).

619. Appendix E, JEP 21-I explains that "[t]he following material may be made into viewgraphs that can be shown at JEDEC meetings to summarize EIA legal guidelines covering the areas of improper activities and programs, patents, and copyright protection. More detailed information in each area is available from the EIA Legal Office." (CX 208 at 26).

620. Appendix E, JEP 21-I includes the following procedure for incorporating patented technology in standards:

> *EIA/JEDEC PATENT POLICY SUMMARY*
>
> Standards that call for use of a patented item or process may not be considered by a JEDEC committee unless all of the relevant technical information covered by the patent or pending patent is known to the committee, subcommittee, or working group. In addition, the committee Chairperson must have received written notice from the patent holder or applicant that one of the following conditions prevails:
>
> * A license shall be made available without charge to applicants desiring to utilize the patent for the purpose of implementing the standards(s),or

> * A license shall be made available to applicants under reasonable terms and conditions that are demonstrably free of any unfair discrimination.
>
> In either case, the terms and conditions of the license must be submitted to the EIA General Counsel for review.
>
> An appropriate footnote shall be included in the standard identifying the patented item and describing the conditions under which the patent holder will grant a license.

(CX 208 at 27).

621. Appendix E of JEP 21-I, which describes itself as an "EIA/JEDEC Patent Policy Summary," indicates that "a patented item or process may not be considered . . . unless all of the relevant technical information covered by the patent or pending patent is known" and that RAND assurances must be obtained. (CX 208 at 27). This statement does not impose a duty to disclose upon members. Rather, it explains the procedure to follow in utilizing known patented items consistent with the requirements of section 9.3.

622. Appendix E does not distinguish between EIA and JEDEC patent policies; it is labeled the "EIA/JEDEC patent policy." (CX 208 at 27).

623. Appendix F, JEP 21-I states:

> *F1. PATENT POLICY APPLICATION GUIDELINES*
>
> The following points describe the application of the JEDEC patent policy:

* Committee discussion of pending or existing patents is a permissible activity and is encouraged when the committee feels that the patented item or process represents the best technical basis for a standard.

* Discussion of a pending or existing patent does not constitute an acknowledgment of the validity of the patent, because validity is based on prior art and determination of who first made the invention or applied for the patent. The committee's concern is with technical merits and whether the technical proposal is a sound basis for standardization.

* By its terms, the EIA Patent Policy applies with equal force to situations involving: 1) the discovery of patents that may be required for use of a standard subsequent to its adoption, and 2) the initial issuance of a patent after the adoption of a standard. Once disclosure is made, the holder is obligated to provide the same assurances to EIA as are required in situations where patents exist or are known prior to approval of a proposed standard.

Thus, if notice is given of a patent that may be required for use of an already approved EIA Standard, a standards developer may wish to make it clear to other standards-making participants that the JEDEC procedures require the patent holder to provide the assurances contained in the

> Patent Policy or suffer the withdrawal of EIA's approval of the standard as an EIA Standard and, ultimately, as an American National Standard.

(CX 208 at 29).

624. Appendix F of JEP 21-I recognizes that (1) discussion of intellectual property issues is allowed, (2) a disclaimer that such discussions do not constitute an acknowledgment of the validity of the patents, and (3) the policy applies to (a) the discovery of patents after a standard is adopted and (b) the issuance of a patent after the standard is issued. This section makes clear that EIA will pursue the same procedure in these situations as if the patent were known during the standardization procedure. Finally, this section provides the penalty for failure to provide RAND assurances: that the standard may be withdrawn. (CX 208 at 29).

625. At the September 1993 JC 42.3 meeting, the committee chairman showed a viewgraph containing proposed language from an appendix to the not-yet-published JEP 21-I manual. This viewgraph was expressly marked "DRAFT" and contained a footnote stating that the "material is a proposed revision" that "has not been approved by JEDEC." (JX 17 at 12). Although this draft did refer to a "patent or pending patent," it did not mention an obligation to disclose intellectual property, nor did it instruct the chairperson to call attention to such an obligation. (JX 17 at 12).

626. The committee chairman also showed a different draft of the 21-I Manual at the December 1992 JEDEC JC 42.3 meeting similarly marked as a draft. (Crisp, Tr. 2983-88; *see* JX 14 at 3, 25).

627. It is not clear that JEP 21-I was ever formally adopted by JEDEC. John Kelly, EIA Legal Counsel, testified that JEP 21-I needed a final stamp of approval from EIA's EDEC and that he

did not know whether JEP 21-I ever received that approval. (J. Kelly, Tr. 2104-05).

628. Complaint Counsel did not provide sufficient evidence to find that JEP 21-I received the approval from EDEC necessary for JEP 21-I to become the controlling manual.

629. Rambus did not receive a copy of 21-I until the summer of 1995. (Crisp, Tr. 3475).

630. JEDEC did not maintain a log of who received copies of manuals and it was not the practice of JEDEC to mail all documents as they were revised. (CX 317 at 1; Grossmeier, Tr. 10944-45).

631. Although JEP 21-I refers to an obligation to disclose intellectual property, it does not provide a basis for the obligation, or a discussion of the extent of the obligation. Moreover, it is facially inconsistent with the EIA sections to which it refers. (*See* CX 208 at 19).

632. JEP 21-I is ambiguous and can not be construed to impose a clear obligation to disclose intellectual property. (*See* CX 208).

3. EIA Legal Guides

633. The EIA Legal Guides include a non-liability disclaimer that "[s]tandards are proposed or adopted by EIA without regard to whether their proposal or adoption may in any way involve patents on articles, materials, or processes. By such action, EIA does not assume any liability to any patent owner, nor does it assume any obligation whatever to parties adopting EIA standards." (CX 204 at 4).

634. The EIA Legal Guides do not contain any specific reference to any disclosure obligation in connection with a member's intellectual property. (*See* CX 204).

4. EP-3-F and EP-7-A

635. The October 1981 EIA manual known as "EP-3-F" provides the following procedure for using patented items in standards:

> 8.3 Reference to Patented Products In EIA Standards
>
> Requirements in EIA Standards which call for the use of patented items should be avoided. No program of standardization shall refer to a product on which there is a known patent unless all the technical information covered by the patent is known to the Formulating committee, subcommittee, or working group. The Committee Chairman must have also received a written expression from the patent holder that he is willing to license applicants under reasonable terms and conditions that are demonstrably free of any unfair discrimination. Additionally, when a known patented item is referred to in an EIA Standard, a Caution Notice, as outlined in the Style Manual, EP-7, shall appear in the EIA Standard.

(CX 203A at 11).

636. The 1990 EIA manual known as "EP-7-A" provides information about obtaining RAND assurances:

> 3.4 Patented Items or Processes

> Avoid requirements in EIA standards that call for the exclusive use of a patented item or process. No program [of] standardization shall refer to a patented item or process unless all of the technical information covered by the patent is known to the formulating committee or working group, and the committee chairman has received a written expression from the patent holder that one of the following conditions prevails:
>
> (1) a license shall be made available without charge to applicants desiring to utilize the patent for the purpose of implementing the standard, or
>
> (2) a license shall be made available to applicants under reasonable terms and conditions that are demonstrably free of any unfair discrimination.
>
> . . . An appropriate footnote shall be included in the standard identifying the patented item and describing the conditions under which the patent holder will grant a license (*see* 6.5.2).

(JX 54 at 9-10).

637. The EP-3-F manual and the EP-7-A manual, which were in effect when Rambus joined JEDEC, both contain a requirement that no standard shall refer to a product on which there is a known patent unless all the technical information covered by the patent is known to the committee or working group. (CX 203A at 11-12; JX 54 at 9).

638. The EP-3-F manual and the EP-7-A manual make no explicit reference to an obligation on the part of EIA members or others to disclose patents or patent applications. (*See* J. Kelly, Tr. 1824-25, 1905-06, 2082-83; CX 203A; JX 54).

5. ANSI Patent Policy

639. The ANSI Patent Policy Guidelines were attached to the May 1992 JC 42.3 meeting minutes and were circulated to JC 42.3 members in 1994. (CX 34 at 19).

640. J. Kelly circulated the ANSI Guidelines to JC 42.3 members in 1994 because he "thought they provided insight into the proper interpretation of the EIA and JEDEC patent policy." (J. Kelly, Tr. 1950).

641. J. Kelly was a member of the ANSI patent policy working group from 1990 until 2002 and was personally involved in the discussions and deliberations leading to the final approval of the ANSI guidelines. (J. Kelly, Tr. 1950-51).

642. At the time that the ANSI Guidelines were circulated to JC 42.3 members in 1994, the language of the EIA patent policy and the ANSI patent policy was essentially identical. (J. Kelly, Tr. 2077-78).

643. The ANSI patent policy guidelines "seek to encourage the early disclosure and identification of patents that may relate to standards under development." (RX 1712 at 6).

644. The ANSI patent policy guidelines specify that "it is desirable to encourage disclosure of as much information as possible concerning the patent, including the identity of the patent holder, the patent's number, and information regarding precisely how it may relate to the standard being developed." (RX 1712 at 8).

645. The ANSI patent policy guidelines indicate that "a standards developer may wish to encourage participants to disclose the existence of pending U.S. patent applications relating to a standard under development. Of course, in such a situation

the extent of any disclosure may be more circumscribed due to the possible need for confidentiality and uncertainty as to whether an application will mature into a patent and what its claimed scope will ultimately be." (RX 1712 at 8).

D. Committee Forms

1. Membership Application

646. The application completed by Rambus upon joining JEDEC does not impose an obligation on members to disclose intellectual property. (CX 601 at 1-2). Indeed, there is no mention of intellectual property in the application. (CX 601 at 1-2).

647. Complaint Counsel did not present sufficient evidence to support their allegation (Complaint ¶ 15) that the JEDEC membership application included an obligation to abide by JEDEC's rules. (*See* CX 601).

2. Meeting Attendance Roster (Sign-In Sheet)

648. Participants at each JEDEC meeting were required to record their names on the sign-in sheet or meeting attendance roster. (CX 306; CX 3136 at 135).

649. Sign-in/attendance rosters were not considered an "official form" because they "vary from division to division and almost year-to-year." (CX 317 at 1).

650. The sign-in/attendance roster states in relevant part: "Subjects involving patentable or patented items shall conform to EIA Policy (reverse side). Consult the EIA General Counsel about any doubtful question." (CX 306 at 1).

651. The sign-in/attendance roster states on the reverse side:

REFERENCE TO PATENTED PRODUCTS IN EIA STANDARDS

Requirements in EIA Standards that call for the use of patented items should be considered with great care. While there is no objection in principle to drafting a proposed standard in terms that include the use of a patented item, if it is considered that technical reasons justify this approach, Committee Chairmen should ensure that no program of standardization shall refer to a product on which there is a known patent unless all relevant and reasonably necessary technical information covered by the patent is known to the formulating committee, subcommittee, or working group. The Committee Chairmen must have also received a written assurance from the patent holder that a license will be made available without compensation to the applicants desiring to utilize the license for the purpose of implementing the standard; or a written assurance that a license will be made available to applicants under reasonable terms and conditions that are demonstrably free of any unfair discrimination.

Additionally, when a known patent item is referred to in an EIA Standard, a Caution Notice, as outlined in the Style Manual, EP-7, shall appear in the EIA Standard.

All correspondence between the patent holder and the formulating committee, subcommittee, or working group, including a copy of the written assurance from the patent holder mentioned above, shall be transmitted to the EIA Engineering Department and the EIA General Counsel at the earliest possible time, but no later than the point

> when the EIA Standard Proposal is ready for Committee ballot. (See the Style Manual for EIA Publications, EP-7, Section 3.4 for required language in an EIA Standard that cites a known patented product).

(CX 306 at 2).

652. The sign-in/attendance roster was modified to include the term "patentable" in the early 1990's around the time of the *Wang* litigation. (J. Kelly, Tr. 1934-35). For discussion of the *Wang* litigation, *see infra* F. 689-90.

653. The reference to "patentable or patented items" on the front page of the sign-in/attendance roster is ambiguous because it refers to the EIA guides. The EIA Guides which appear on the reverse side, however, apply only to issued patents. (CX 306 (EIA Legal Guides use the terms: "patented items," "known patent," "technical information covered by the patent," and "patent holder")).

3. Committee Ballots

654. The committee ballots used by JEDEC to record votes on standardization proposals contained a variety of voting options, including an option which read: "I do not approve the content of the [ballot topic]. Attached are my detailed reason(s) for this disapproval. (We need your reason(s) in order to understand your view on this matter.) MANDATORY." (CX 252A at 2).

655. The committee ballots also stated: "If anyone receiving this ballot is aware of patents involving this ballot, please alert the Committee accordingly during your voting response." (CX 252A at 2).

656. When this language regarding patents was first added to the committee ballots, a JEDEC member asked during a JEDEC meeting about the purpose of the new language. The minutes of the JC 42.1 meeting held on September 13, 1989 state that:

> Council discussed patent issue at their June meting [sic] at the request of JC-42.3. The result was not to change EIA legal requirements as outlined in document EP-7, but to add some wording on JEDEC ballot voting sheets about informing the Committee if any patent covers the balloted material.
>
> TI was concerned that Committee members could be held liable if they didn't inform Committee members correctly on patent matters. Committee responded that the question was added on ballot voting sheets for information only and was not going to be checked to see who said what.

(CX 3 at 6).

657. Sussman explained the options on ballots as follows:

> Yeah, I can approve the ballot. I can not approve the ballot. I can abstain on the ballot. I can approve it with comments. And the bottom one is saying that regardless of what I do, ignoring any of the above things, I can also point out that I know of or I believe there might be a patent that could read on the – on this concept, on this ballot.

(Sussman, Tr. 1391).

658. It is clear from the plain language of the committee ballot that a no vote mandates an explanation, while patent disclosure is only requested on a voluntary basis. (*See* CX 252 at 2).

4. Members' Manual

659. The introduction to the "JC 42 Members' Manual," dated September 1994, states that "[t]his manual was compiled to assist new (and established) members in achieving full effectivenes [sic] in the standards making process." (RX 507 at 2).

660. The members' manual was a document created by Jim Townsend, JC 42 Chairman, and does not display the JEDEC or EIA trademarks or otherwise purport to be an official EIA publication. (RX 507).

661. The members' manual was not approved by the JEDEC Council and the meeting minutes indicate that "[s]ome of this material is not approved by JEDEC . . . It should be clear that this manual is not a publication of JEDEC because it has not been balloted by Committee or Council." (JX 31 at 4).

662. The members' manual patent policy section states: "Committees adhere rigidly to the EIA patent policy as given in EIA publication EP-7-A, August 1990, Pars. 3.4 & 3.5 and in EIA Publication EP-3-F, October 1981, Par 8.3 which require intellectual property disclosure and discussion if proposed [*213] standards are affected." (RX 507 at 15).

663. The members' manual states that "[a]ll first presentations must be accompanied by written handouts for all companies present giving complete details of the material being presented. In addition, the presenter must reveal any known or expected patents, within his company, on the material presented." (RX 507 at 15).

664. The members' manual is ambiguous because it states that the committee "adheres rigidly to the EIA patent policy" which it describes as requiring intellectual property disclosure. (RX 507 at

15). However, the EIA patent policy to which it refers does not *require* disclosure of intellectual property. (See F. 633-38).

665. The members' manual is also ambiguous because the patent policy section suggests a requirement of intellectual property disclosure without indicating who is required to disclose, while the "First Presentation" section limits disclosure to those making presentations. (*See* RX 507 at 15).

5. Patent Tracking List

666. A patent tracking list, which was a compilation of patents and patent applications of which Townsend had been made aware through the course of the work inside JEDEC, was maintained by Chairman Townsend. (Rhoden, Tr. 325; Sussman, Tr. 1355).

667. Townsend "began the patent tracking list . . . in May of 1991." (G. Kelley, Tr. 2407). The patent tracking list had multiple purposes, including record-keeping, a reminder to other participants of the patent issues that were on, and as an educational tool for those who were newcomers to the committee. (G. Kelley, Tr. 2407-08).

668. The patent tracking list was an informal, incomplete list of patents and patent applications disclosed to the JC 42.3 committee. (G. Kelley, Tr. 2408). Rhoden explained that it "was Mr. Townsend's personal list, and I'm not sure that everything was included in it." (Rhoden, Tr. 334-35).

669. The cover sheet accompanying the patent tracking list included the term "patentable matters" which JEDEC Chairman Rhoden testified he understood to mean "anything that would be in the patent process. Essentially if you believe that you have ownership of a particular topic or a particular item, then that is what he's referring to. Patentable, whether a patent had actually been applied for or not." (Rhoden, Tr. 336).

E. Contemporaneous Correspondence

1. The McGhee Memorandum

670. ETSI is the European Telecommunications Standards Institute. As indicated in the EIA letter to the Federal Trade Commission commenting on the *Dell* consent order, ETSI undertook efforts "to force compulsory licensing on an extraterritorial basis." (RX 669 at 3).

671. On March 29, 1994, JEDEC Secretary Ken McGhee sent a memorandum to JC 42 Chairman Jim Townsend regarding the "ETSI Policy within JEDEC" that stated that JEDEC's legal counsel had said that:

> [H]e didn't think it was a good idea to require people at JEDEC standards meetings to sign a document assuring anything about their company's patent rights for the following reasons:
>
> (1) It would have a chilling effect at future meetings
>
> (2) A general assurance wouldn't be worth that much anyway
>
> (3) It needs to come from a VP or higher within the company – engineers can't sign such documents
>
> (4) It would need to be done at each meeting slowing down the business at hand.

(RX 486 at 1).

2. Correspondence Regarding the Dell Consent Agreement

672. The Commission issued a complaint and entered into a consent agreement with Dell Computer Corporation ("Dell") which prohibited Dell from enforcing its patent rights against computer manufacturers using the VL-bus. The Commission placed upon the public record the executed consent decree with a request for public comments. *In re Dell Computer Corp.*, 121 F.T.C. 616, 619 (May 1996).

673. In January 1996, a letter was submitted to the FTC on behalf of EIA and its unincorporated divisions and departments (including JEDEC), as well as on behalf of the Telecommunications Industries Association ("TIA"), in response to the *Dell* action. EIA General Counsel J. Kelly's name and title appear in the signature block. (RX 669 at 5; J. Kelly, Tr. 2092-93).

674. The EIA's January 1996 comment letter to the Commission states in relevant part:

> Both EIA and TIA encourage the early, voluntary disclosure of patents that relate to the standards in work. Committee and subcommittee chairs ask during the meetings whether any parties are aware of any patents that relate to the contributions under discussion. When potential patents are disclosed, EIA and TIA staff contact the patent holders to ensure that essential patents will be licensed in accordance with the EIA, TIA and ANSI IPR policies.

(RX 669 at 3).

675. The EIA's January 1996 comment letter to the FTC clarifies that the "EIA, TIA and ANSI IPR policies relate to

essential patents" and that "even if knowledge of a patent comes later in time due to the pending status of the patent while the standard was being created, the important issue is the license availability to all parties on reasonable, non-discriminatory terms." (RX 669 at 3, 4).

676. In July 1996, the FTC, in a letter signed by FTC Secretary Donald Clark, responded to the EIA's January 1996 letter. The FTC's letter states in relevant part that: "EIA and TIA, following ANSI procedures, encourage the early, voluntary disclosure of patents, but do not require a certification by participating companies regarding potentially conflicting patent interests." (RX 740 at 1).

677. The FTC's statement distinguishing the EIA's patent policy from the policy at issue in the *Dell* matter, and the FTC's explanation that the differences in the two patent policies meant that the "expectations of participants in the two standard-setting processes differ," indicate that FTC Secretary Clark interpreted the EIA's January 1996 letter to mean that the EIA encouraged, but did not require, the disclosure by members of intellectual property interests. (RX 740 at 2; *see* RX 669 at 2).

678. On July 10, 1996, JEDEC Secretary Kenneth McGhee sent a memorandum to Jim Townsend, addressed to "JEDEC Council Members and Alternates," regarding the FTC's Final Consent Order in the *Dell* case, which stated in part that: "the FTC emphasized that it was not intending to signal a general duty to search for patents when a company engages in standards setting (ANSI and EIA do however, encourage early, voluntary disclosure of any known essential patents.)" (RX 742 at 1).

679. These letters clearly state JEDEC's patent policy was limited to encouraging early, voluntary disclosure of any known essential patents. (RX 669; RX 742).

3. Correspondence Regarding Micron Disclosure

680. On January 28, 2000, Micron drafted a written disclosure of a patent application relating to a proposed standard under consideration in the JC 42.4 subcommittee. (RX 1559 at 2).

681. On February 1, 2000, JEDEC Secretary McGhee sent an email to members of the subcommittee stating, "I would like to point out that this letter is well intentioned, but lacks a patent number, so it does not complete the requirements for JEDEC patent policy. If, however, a follow-up letter is issued after the patent is issued, then it would comply with JEDEC's patent policy." (RX 1559 at 1).

682. Upon receiving McGhee's email that Micron had not complied with the patent policy because Micron's disclosure did not include a patent number term, Terry Walther of Micron caused the matter to be placed on the agenda for the next JEDEC board meeting. (RX 1568 at 25).

683. The minutes of the February 2000 meeting of the JEDEC Board of Directors state:

> D. Disclosure on Patents Pending
>
> Mr. Walther noted that Micron had sent a letter indicating they have patents pending on items that may affect committee standards. The issue was whether companies should make public that a patent is pending. The BoD discussed it and noted they encourage companies to make this kind of disclosures even though they were not required by JEDEC by laws.

(RX 1570 at 13).

684. In an email written a few days after the February 2000 board meeting, JEDEC Secretary Ken McGhee, who had been present at the meeting (RX 1570 at 2), reported to a JEDEC subcommittee that the JEDEC Board had discussed Micron's "patent pending" disclosure. Secretary McGhee stated that:

> The JEDEC patent policy concerns items that are known to be patented that are included in JEDEC standards. Disclosure of patents is a very big issue for Committee members and cannot be required of members at meetings. However, if a company gives early disclosure on a patent they are working on, it definitely gives a lot of assurance to the Committee members regarding development of any standards affecting it.
>
> Therefore, in Micron's letter, by giving early disclosure, they have gone one step beyond the patent policy and have complied with the spirit of the law. JEDEC encourages this type of activity from any member.

(RX 1585 at 1).

685. Disclosure of patent applications, or pending patents, was "not required" by JEDEC in 2000 even though disclosure was "encouraged." (RX 1570 at 13). The "spirit of the law" is to disclose patent applications even though disclosure "cannot be required of members." (RX 1585 at 1).

F. Conduct of Parties in JEDEC

1. SEEQ Issue

686. A company named SEEQ proposed a JEDEC standard called silicon signature. (Sussman, Tr. 1338). SEEQ owned two patents related to the technology, but disclosed and offered to

license only one. (Sussman, Tr. 1338-39 (SEEQ "was telling us about silicon signature and offering it as a royalty-free license to anyone who wanted it, hoping that just as soon as we standardized this, the second patent, which would be die trace, which he had not said anything about, but because it was almost identical, would be insisted upon by the customers, and [SEEQ] could put a tax on us.")).

687. Upon learning of SEEQ's second patent, the committee was willing to standardize the SEEQ technology, provided that SEEQ agreed to reasonable licensing terms. (CX 3 at 4).

688. When the committee learned that the second patent was not included in the patent release, JEDEC chose to standardize on a different technology. (Sussman, Tr. 1338-39).

2. *WANG* Litigation

689. The *Wang* litigation involved allegations of a failure to disclosure a patent application on the part of a company that had promoted its technology for standardization. (CX 711 at 188). Wang was "part of the committee, they had helped set a standard, and then they went out and enforced their patents against everybody in the industry who used a SIMM module." (Williams, Tr. 787).

690. Wang failed to disclose a patent relating to memory modules and later attempted to enforce the patent against the industry which "ended up in a rather lengthy litigation, crossed multiple houses and cost the industry millions of dollars before the patent was found to be invalid." (Sussman, Tr. 1338; *see also* Landgraf, Tr. 1697-98; JX 20 at 4).

3. IBM's Patent Position

691. The minutes of the March 1993 meeting of JC 42.3 state in part that "IBM noted that their view has been to ignore [the]

patent disclosure rule because their attorneys have advised them that if they do then a listing may be construed as complete." (JX 15 at 6).

692. In an August 1993 memo to JEDEC leaders entitled "BGA Patent/License Rights," IBM JEDEC representative (and JEDEC 42.3 subcommittee chair) Gordon Kelley stated that:

> IBM Intellectual Property Law attorney's [sic] have informed me that we will not use JEDEC as a forum for discussing this subject. It is the responsibility of the producer to evaluate the subject and to workout the proper use of rights. So, I can not confirm or deny any IPL rights.

(RX 420 at 2).

693. The December 1993 JEDEC 42.3 minutes state in part that "[a]s a side issue, IBM noted that in the future they will not come to the Committee with a list of applicable patents on standards proposals. It is up to the user of the standard to discover which patents apply." (JX 18 at 8).

694. Between December 1993 and December 1995 (Rambus's last meeting), no IBM patent or patent application was added to the "patent tracking list" maintained by JC 42 Chairman Jim Townsend. (*See* JX 18 at 14-21; JX 19 at 17-23; JX 20 at 15-18; JX 21 at 14-18; JX 22 at 12-17; JX 25 at 18-26; JX 26 at 15-24; JX 27 at 20-25; JX 28 at 12-23).

695. Regarding IBM, Cray representative Grossmeier testified that "IBM said they didn't feel they had the resources to review their entire patent portfolio every time a proposal was made to see if there was anything in there that was applicable. So, they would not disclose any patents that they had that were related to the standard." (Grossmeier, Tr. 10956). His opinion was that "I think

they all understood the policy. I think they just elected not to practice it." (Grossmeier, Tr. 10956-57).

696. A Hewlett-Packard representative to JEDEC, Hans Wiggers, testified that he had attended a JEDEC meeting where IBM representative and Committee Chair Gordon Kelley said:

> Look, I cannot disclose – my company would not let me disclose all the patents that IBM is working on because, you know, I just can't do that. The only thing we will do is we will follow the JEDEC guidelines and – or rules on whatever and we will make them available.

(Wiggers, Tr. 10592-93).

697. This is consistent with Gordon Kelley's testimony. G. Kelley testified that he did not disclose IBM patents relating to "toggle mode" in 1990 in part because IBM was "prepared to meet the requirements of the JEDEC committee" to license the patents on reasonable and nondiscriminatory terms. (G. Kelley, Tr. 2715-16).

698. Complaint Counsel did not present sufficient evidence from which to find that IBM was ever sanctioned for announcing its refusal to disclose the company's intellectual property.

4. Hewlett Packard's Patent Position

699. Hewlett Packard's representative, Wiggers, testified that when JC 42.3 Chair G. Kelley stated his position at the JEDEC meeting regarding IBM's nondisclosure of patent applications, Wiggers told the meeting attendees that HP took the same position. (Wiggers, Tr. 10593-94).

700. Complaint Counsel did not present sufficient evidence from which to find that Hewlett-Packard was ever sanctioned for

announcing its refusal to disclose the company's intellectual property.

5. Texas Instruments' QUAD CAS Issue

701. On March 9, 1994, Texas Instruments presented a letter to JEDEC regarding ambiguities in the JEDEC patent policy. This letter began "Texas Instruments believes that the JC 42.3 Committee on RAM Memories should review and clarify its interpretation of the JEDEC Patent Policy." The letter further states that "TI is concerned that the committee, or at least some of its members, have interpreted the scope of the JEDEC Patent Policy in a manner that is not only incorrect but unworkable as well. The resulting confusion has made it impossible for TI and other members to determine the appropriate course of conduct." (CX 352 at 1).

702. A memorandum to JC 42 committee members dated May 12, 1994 says that TI's request for clarification of the patent policy was referred to EIA's legal counsel J. Kelly for response. The memorandum attached a copy of J. Kelly's response. (CX 355 at 1).

703. John Kelly's response indicates that "[w]ritten assurances must be provided by the patent holder when it appears to the committee that the candidate standard *may require* the use of a patented invention." (CX 355 at 2 (emphasis in original)).

704. The meeting minutes indicate that at the close of a discussion on patents at the March 1994 Committee meeting, the committee felt the patent policy was clear and that discussion would be closed on the subject. (JX 19 at 4-5; Kellogg, Tr. 5028-30).

705. Gordon Kelley indicated: "I believe that the litigation between Micron and Texas Instruments was resolved, and I believe that the ballots that were on hold were removed from hold

and the ballots that were in recision were reconstituted." (G. Kelley, Tr. 2483). In addition, he stated that Texas Instruments "apologized for their representative who had not disclosed – I personally know that they removed him from the committee, he did not come back, and they settled their dispute with Micron and as far as the committee was concerned, the issue was at this point resolved." (G. Kelley, Tr. 2485).

706. Cray representative Grossmeier testified that "some members agreed that [TI] didn't need to [disclose] and other[s] felt that they were in violation of the JEDEC policy by not [disclosing]." (Grossmeier, Tr. 10955).

707. This is clear evidence that by 1994, the patent policy was ambiguous. Indeed, in 1994 Texas Instruments explicitly recognized the "confusion" created when some members of the committee "interpreted the scope of the JEDEC Patent Policy in a manner that is not only incorrect but unworkable as well." (CX 352 at 1).

6. Micron's Presentation on Burst EDO

708. Brett Williams, of Micron, put together a presentation on Burst EDO that was presented at a January 1995 JEDEC DRAM task group meeting. (JX 23 at 68-77; Williams, Tr. 825-26). Williams was present at the meeting and was aware that Micron's Burst EDO patent application, on which he was a named inventor, was not on the patent tracking list. (JX 23 at 1; Williams, Tr. 963-64). Nevertheless, Williams did not disclose the pending patent application on Burst EDO in connection with that presentation and vote. (Williams, Tr. 936-37; *see* RX 585 at 3-4).

709. It was not until April 1996 that Micron's Burst EDO patent application was disclosed to JEDEC when Micron offered to license the patents under reasonable terms and conditions, demonstrably free of any unfair discrimination, if the patents were

issued and were required for use of the standard. (CX 364; Williams, Tr. 937).

710. At trial, Williams was questioned about the potential perception of his actions:

> Q: Okay, So once the patent issued in June of '96, if somebody had gone back and looked at that patent, they would have seen – by just looking at the patent, they would have seen, well, Micron cited as prior art early JEDEC meetings, and Micron applied for the patent in December '94, after some of the early meetings and before – right before the January '95 presentation that you and Mr. Fusco attended, and the patent issued in June of '96, and Micron made the disclosure to JEDEC in April of '96. That's the facts they would have seen.
> A: Yes.
>
> Q: And to your knowledge, nobody seeing those facts, no JEDEC member, came to Micron and said, you guys acted in a way inconsistent with the JEDEC policy, did they?
> A: I'm not sure if anybody talked to Micron about that or not. Nobody talked to me about it.

(Williams, Tr. 941-42.)

7. Hyundai and Mitsubishi's Presentation on SLDRAM

711. On May 24, 1995, Hyundai and Mitsubishi made presentations at a meeting of the JC 42.3 subcommittee regarding a type of DRAM known as SLDRAM. (JX 26 at 10-11; Rhoden, Tr. 469-71). The minutes note that "[t]he proposal was brought to JEDEC for a pinout standard." (JX 26 at 10). The Mitsubishi

presentation showed the pinout for an SLDRAM. (JX 26 at 111; Rhoden, Tr. 471).

712. At a JEDEC meeting on December 9-10, 1997, the SLDRAM pinout standard ballot was approved by the JC 42.3 subcommittee. (JX 41 at 22, 24; RX 1114 at 1; Rhoden, Tr. 1206-08).

713. United States Patent No. 6,442,644 (the '644 patent) issued on August 27, 2002. (RX 2086 at 1). Among the inventors named on the patent were JEDEC representatives Hans Wiggers of Hewlett-Packard, Kevin Ryan and Terry Lee of Micron, and JEDEC Chairman Desi Rhoden, formerly of VLSI. (RX 2086 at 1).

714. Rhoden testified that claim 3 of the patent claims the SLDRAM pinout that had been standardized by JEDEC. (RX 2086 at 41; Rhoden, Tr. 1211).

715. The '644 patent claims priority to a number of provisional applications, including provisional application 60/069,092 which was filed on December 10, 1997, the very same day that the JEDEC meeting approving the SLDRAM patent was being held. (RX 2086 at 1; RX 2099-43).

716. Wiggers, Ryan and Rhoden were all present at the December 1997 JC 42.3 subcommittee meeting where the SLDRAM pinout standard was balloted and approved. (JX 41 at 2). They were each involved in or affiliated with the "SLDRAM Consortium" or SLDRAM Inc., which subsequently became AMI2, and was assigned the '644 patent. (RX 870 at 1; Rhoden, Tr. 696-97, 1235; RX 2086 at 1).

717. The minutes of the meeting do not indicate that any of the three disclosed the '092 provisional application, (*see* JX 41 at 22, 24), even though Rhoden testified at trial that even non-member guest scientists or engineers from foreign countries were

"absolutely" obligated to disclose patents and patent applications that were related in some general way to a subject being discussed at JEDEC. (Rhoden, Tr. 624-25).

G. Trial Testimony

1. A Policy in Transition

718. The evidence suggests an unsuccessful attempt by some members of JEDEC to redefine the patent policy after SEEQ and *Wang*. (*See* CX 46 at 9). Complaint Counsel, however, did not produce evidence sufficient to find an announced, formal change in policy.

719. Some members of the committee treated the spirit of the policy as the actual policy. Williams testified that between late 1991 to 1993, "[i]t was discussed how to revise the wording to ensure that the patent policy was clear so that new members, when they came on board, would know exactly the spirit of the patent policy." (Williams, Tr. 791).

2. Creation of Ambiguity and Confusion Regarding the Policy

720. IBM's representative Mark Kellogg disclosed, at least twice, an intention on the part of IBM to file a patent application related to a product or feature under consideration for standardization at JEDEC. At his deposition, Kellogg testified that he did not believe the disclosure was required under the JEDEC patent policy. He contradicted this testimony at trial:

> A: I would appreciate a chance to clarify because there's a written policy, there was an in-process modified policy, there is an expected policy, there are – there are – so in answer to your question, this refers to the written policy at the time in this document.

> Q: In the deposition?
> A: And I do apologize for differing interpretations of policy.
>
> Q: When I asked you in the deposition whether you believed your disclosure was required under the JEDEC patent policy, what JEDEC patent policy were you referencing when you answered no?
> A: The written policy at the time.
>
> Q: Were there more than one JEDEC patent policy that related to the obligations to disclose intent to file patent applications?
> A: I believe so.

(Kellogg, Tr. 5306-07).

721. Cray representative Grossmeier was unclear on JEDEC's patent disclosure rules, as evidenced by his trial testimony that in the 1991-96 time frame "[i]t was not real clear on the definition of what patents should be disclosed. Clearly if the *sponsor* presented information that they were developing and patenting, they would disclose it, but other parties, it was pretty vague." (Grossmeier, Tr. 10947 (emphasis added)).

722. Intel representative Sam Calvin testified that:

> There was – and I don't know when it occurred or how early it occurred, but there was a concern about not only patents, but applications for patents. And I'm then real foggy on this, because I knew it was an issue, but when exactly it went from an issue to understanding that to be JEDEC policy is unclear in my mind.

(Calvin, Tr. 1006).

723. The JEDEC patent policy was not clear. (Kellogg, 5306 ("there's a written policy, there was an in-process modified policy, there is an expected policy"); Grossmeier, Tr. 10947 (patent policy was "not real clear . . . . it was pretty vague"); Calvin, Tr. 1006 (describing patent policy as "unclear")). This lack of clarity stemmed from an unsuccessful attempt, by some, to redefine the patent policy.

3. Unsuccessful Efforts to Expand the Patent Policy

724. The February 1991 minutes from the 42.5 subcommittee meeting note that "Townsend made a presentation on patent issues in general and made some suggestions as to what could be done in the future to avoid these problems." (CX 13 at 4).

725. Attached to the meeting minutes were handwritten notes. These notes include a section labeled "Expectations of Participants" which includes as the only expectation regarding disclosure that "[f]ull disclosure of *sponsors* regarding restrictions on intellectual property at conceptual phase of draft standard." (CX 13 at 31 (emphasis added)).

726. The notes include a section labeled "Possible Solutions on Intellectual Property" which includes the following suggestions:

> Require each member and alternate, each year, to sign an affadavit that they will disclose all knowledge of patents affecting a draft ballot.
>
> Requiring a legal statement from the sponsoring company's Intellectual Property counsel to be attached to an approved ballot when submitted to Council for final approval.

> Expulsion from JEDEC of a company who attempts to achieve commercial advantage from standardization if they have not disclosed at the beginning their patent position, intention, and royalty objectives on a draft 'patent.'
>
> Censure by the supplier community of any such company.
>
> Establish equivalent standards to provide royalty-free alternatives to the industry.

(CX 13 at 32).

727. In a March 11, 1991 letter copied to John Kelly, John Kinn, Vice President of Engineering at JEDEC, in response to a letter from Jim Townsend regarding JEDEC's patent policy, indicated that "[t]he basic documents containing our policy on patents are: EP-3, EP-7, The JEDEC Manual JEP-21-H, and the EIA Legal Guide." (CX 317).

728. Kinn attached a draft revision of the ANSI policy, indicating that it was "arrived at following two years of discussion among legal representatives, from Standard developers and users. Many individuals feel they do not go far enough – others feel they go too far – a classic case of our inability to harmonize conflicting opinions in areas outside those that must obey the laws of physics." (CX 317 at 1).

729. Kinn noted a discussion from the previous council meeting although "no definitive conclusions were reached other than to await the results of the ANSI work." (CX 317 at 1). Kinn stated "I agree this issue should be continually reviewed at Council level until we arrive at the best possible policy given modern circumstances and technology. Perhaps JEDEC should sponsor a special workshop . . . and perhaps achieve a consensus on future directions for our policy." (CX 317 at 2).

730. Meeting minutes from the May 9, 1991 JC 42.3 meeting indicate, regarding intellectual property, that:

> Toshiba noted that some of the procedure documents have been issued a long time ago but because of high Committee turnover many reps don't know what the policies are. Toshiba recommended that at each meeting a showing be made to explain what the intellectual property policies are. Toshiba would also like to have a note on each ballot before it goes to Council from the company lawyer. It was a Council issue, but Toshiba wanted the Committee to deal with it.

(JX 5 at 3).

731. G. Kelley, JC 42.3 Chair, testified that "Jim Townsend had suggested that we begin to include patent applications in the concept of a patent and that was brought to the committee in May of 1991 and the vote was taken to agree that the committee would work to that new definition of patents," although there is no evidence of such a vote in the May 1991 minutes. (G. Kelley, Tr. 2691; *see* JX 5).

732. JEDEC Council Minutes from May 18-19, 1992 state that a "discussion was held concerning patent policy. The Secretary outlined the genesis for changes and the fact that a new set of policy statements and guidelines have been written that will be circulated to Council for review and comment." (CX 35 at 9).

733. "Consensus was expressed that more strength is needed in our policy, however under existing laws, it seemed difficult to do. This item will be discussed further in the revision of 21-H," according to the minutes of the January 19-20, 1993 JEDEC Council meeting. (CX 46 at 9).

734. Some members wanted to redefine the patent policy to include patent applications and the intent to file patent applications. "Consensus was expressed that more strength is needed in our policy" was understood by JC 42.3 Chair G. Kelley to mean "the more strength concept to be the inclusion of patent applications and material that might become patents to the concept of patent requirements within the previous document." (G. Kelley, Tr. 2421).

735. Existing EIA policy, which controlled JEDEC policy, did not permit such an expansive definition. "However, under existing laws, it seemed difficult to do" was interpreted by JC 42.3 Chair G. Kelley as follows: "[i]n my understanding, the difficulty was that the EIA Legal Guides did not include the patent application and material that might become patents concept, and the question before council was could we expand the definition under JEDEC Council control without endangering our position under the EIA control." (G. Kelley, Tr. 2422).

736. This helps explain why the possible solutions on intellectual property were never implemented. (*See* CX 13 at 32).

737. Instead of explicitly and formally changing the JEDEC policy from the EIA policy, the Council unsuccessfully attempted to redefine the word "patent." JC 42.3 Chair G. Kelley stated that "[a]t the JEDEC council, which was struggling with the change in wording of the JEDEC policy, we discussed the conflict between the EIA wording of their patent policy and the change that we were making, which was patents and patent applications, and we believed as a group that the concept of patents includes patent applications, that the concept of patents is a concept which says avoid patents or material that could become patents, and if you can't avoid them, then you must deal with the RAND requirements." (G. Kelley, Tr. 2696).

738. This attempted redefinition of the policy marked a departure both from established JEDEC policy and from EIA

patent policy and caused confusion by creating ambiguity in the policy. (See F. 606-38, 718-47).

739. Toshiba representative and JEDEC JC 42 Chairman Jim Townsend led the unsuccessful attempt to redefine JEDEC's patent policy. Townsend was described as "a general with a flagpole patent" (G. Kelley, Tr. 2401-02), as "very sensitized by the WANG case" (Sussman, Tr. 1353), and as someone on "a personal crusade." (CX 2079 at 38 (Karp Micron Dep.)). Townsend and the rest of the board wanted to ensure that *Wang* never happened again, so that "the industry was not held hostage again." (Williams, Tr. 786-87).

4. Changes in Policy Language

a. EIA Patent Policy

740. Between 1991 and 1996, JEDEC "was an activity within the EIA engineering department" (J. Kelly, Tr. 2075) also described as "until early 2000, JEDEC was part of the EIA corporate structure." (J. Kelly, Tr. 1915). "If there was a conflict, the broader rules of EIA would govern." (J. Kelly, Tr. 1916). J. Kelly testified that in the event of a conflict, any JEDEC manual would be subordinate to the EIA manuals. (J. Kelly, Tr. 1915-6).

741. Gordon Kelley, who was the chair of the JEDEC Council and of the JC 42.3 subcommittee during much of the relevant time, testified that he understood there to be a basic conflict between the JEDEC and EIA manuals, for the EIA manuals intended the word "patents" to mean simply "patents," while the JEDEC manual (at least by 1993) allegedly intended the word "patents" to mean "patents and patent applications." (G. Kelley, Tr. 2686-87; 2695-97). Up until late 1996, G. Kelley understood that EIA's definition of "patent" had not changed. (G. Kelley, Tr. 2697).

742. This contradicted testimony by EIA General Counsel John Kelly that EIA rules and JEDEC rules concerning disclosure and licensing of patents were consistent. (J. Kelly, Tr. 1915-16, 1919-20). J. Kelly testified that he believes that EIA's interpretation has always been that the term "patents" as used within EIA and JEDEC includes patent applications. (J. Kelly, Tr. 1887).

743. JEDEC manuals regarding the patent policy consistently refer the reader to the EIA Legal Guides and both JEP 21-H and JEP 21-I state that EIA Legal Guides are controlling. Nothing in the EIA Guides indicates that patents refers to anything other than issued patents. (F. 633-38).

b. Changes Found in JEP 21-I

744. Both Gordon Kelley and John Kelly testified that the textual change in the 21-I manual to include a reference to pending patents "was a restatement of the patent policy, and it in no way varied the policy itself." (J. Kelly, Tr. 1925; *see also* G. Kelley, Tr. 2415-16).

745. However, G. Kelley contradicted his own testimony regarding whether 21-I represented a change in policy, stating that in January of 1992, "[t]he council was dealing with this revision of 21-I, and some major changes were going to be taking place in the committees as a result of this revision." He indicated that the changes included "the inclusion of patent applications in the wording of the patent section." (G. Kelley, Tr. 2411). G. Kelley later explained that the expanded wording "did not change the substance of the practice that we had been performing to this point, it just brought this document up to date to that practice." (G. Kelley, Tr. 2423). Later he explained, "[w]e were including the words in this document which added the requirement of disclosing patent applications to the document as we had been practicing in JC-42 for several years at this point." (G. Kelley, Tr. 2431).

746. G. Kelley explained this contradiction as based on the ambiguous definition of the word "patent." When initially asked about his understanding in 1993 of the EIA patent policy as it related to patent applications, G. Kelley stated: "[t]he reason I'm struggling is that I understood after the beginning of 1991 that the concept of patent included material that might become published patents and that changing the document [ie 21-I] to include patent applications was just a clarification but not a change in the policy, whether it was JEDEC, EIA or ANSI." (G. Kelley, Tr. 2679). He explained "what happened with me is my definition of 'patents' changed. . . . [T]he patent policy in the JEDEC manuals, EIA manuals and ANSI manuals only specified 'patents,' which in my mind before 1991 meant issued patents. However, beginning in early 1991, it was very clear on the committee that the committee considered the issue of patents to be issued patents as well as material that might become issued patents." (G. Kelley, Tr. 2694-95).

747. According to JEDEC Chairman Rhoden, the footnote in JEP 21-I which states that "the word 'patented' also includes items and processes for which a patent has been applied and may be pending" was "added to further emphasize for anyone reading the document and to myself the word 'patent' has always applied to all things within the patent process inside of JEDEC, and that's the explanation that has always been given by myself inside of JEDEC committees, and the footnote was added to add – make sure that everyone understood the word 'patent' involved everything within the patent process." (Rhoden, Tr. 316-17).

5. Conflicts in the Trial Testimony

748. The EIA/JEDEC patent policy cannot be based upon a common understanding of the policy, as the conflicts in the trial testimony show that there was no common understanding. JEDEC members testified not only to different understandings of the

policy, but some witnesses' testimony was not credible and even contradicted their own prior testimony. (*See* F. 749-65).

a. Trial Testimony Conflicts Regarding Whether the Patent Policy Applied to Patent Applications and Intentions to File Patent Applications

749. There was conflicting testimony from JEDEC members regarding whether the patent policy applied to patent applications and intentions to file patent applications. One opinion that was expressed was that the word *patents* includes *patent applications*. (Calvin, Tr. 1006-07; J. Kelly, Tr. 1886-88, 1896-97; Landgraf, Tr. 1695-96; Lee, Tr. 6595-96; Williams, Tr. 771, 909-11).

750. Another opinion was that the policy extended to include an intent to file a patent application. For example, JC 42.3 Chair G. Kelley testified that when JC 42 Chairman Townsend used the term "patents," "I understood him to mean an issued patent that was available from the patent office, patent applications that were being worked on with the patent office, and items that were probably going to become patents." (G. Kelley, Tr. 2406-07).

751. JEDEC Chairman Rhoden testified that in his "understanding of the policy, the term 'patent' applies to the patent process, anything in that patent process." (Rhoden, Tr. 636-38). Rhoden was unable to cite a JEDEC or EIA manual that expressly stated that disclosure had to be made of an intention to file a patent application, explaining that "I have seen in those manuals the wording that would say that it is a requirement for patents, and then it would be my interpretation of that that – operating in the committee and in the guise of standardization that that would be covered and would be included." (Rhoden, Tr. 639-40).

752. Moreover, there was testimony that *presenters* were required to disclose intellectual property before they advocated a particular technology which implies that non-presenting *members*

were not under the same obligation. (*See* McGrath, Tr. 9273-74). For example, Intel representative Calvin testified:

> The reason I alluded to two different periods, and I can't tell you specific dates, is that I was aware initially that there was a policy that any applicable patents that might have effect on standard or development should be disclosed. I was also aware during that early period, and I don't know whether it was '92 or '93, but I was aware that the primary obligation was upon the presenting advocate of the standard, but that the secondary obligation, or almost to the same extent, I shouldn't say almost, it was to the same extent, was to anyone within the body that knew of patents that might have effect upon the standard.

(Calvin, Tr. 1004.)

b. Trial Testimony Conflicts Regarding Whether Members Should Disclose Actual Claims or Whether a Patent Number Was Sufficient

753. There was a conflict in the trial testimony regarding what should be disclosed under the policy. For example, one view was that the patent policy required a participant to disclose sufficient information to put the committee on notice as to the nature of the relationship between the proposed standard and the intellectual property that might relate to the proposed standard. (J. Kelly, Tr. 1870-71; Calvin, Tr. 1010-12; Rhoden, Tr. 627; Williams, Tr. 771-72, 774-75, 793-94).

754. In contrast, other JEDEC members, including Board Chairman Desi Rhoden, testified that it would be sufficient for a member simply to state that it "might have IP relating" to its presentation. (Rhoden, Tr. 1304-05).

755. JC 42.3 Chair G. Kelley testified at trial to a disclosure obligation in direct contradiction to his own prior testimony. At the hearing, he testified that upon disclosure, a company must "describe the claims of the patent, probably paraphrased, sometimes handed out as a handout the published patent but more often paraphrased so that the committee understood why the issues of that patent material applied to the discussion in JEDEC" and specifically stated that disclosure of a patent number alone was not enough. (G. Kelley, Tr. 2697-98). However, when asked, in reference to his own prior testimony in a Micron transcript, "[d]id you testify that you believed the giving of the patent number would be enough and that that would give you the information that you needed to go back and research the details on the patent?" he responded "[t]he patent number would be enough." (G. Kelley, Tr. 2700).

c. Trial Testimony Conflicts Regarding Whether More Than Essential Patents Were Included in the Policy

756. There was conflicting testimony regarding what should trigger disclosure. For example, JC 42.3 Chair and IBM representative Gordon Kelley testified that disclosure was triggered by a patent claim that "reads on or applies" to the standard, meaning that "if you exercise the design or production of the component that was being standardized [it] would require use of the patent." (G. Kelley, Tr. 2706-07).

757. Another IBM JEDEC representative, Mark Kellogg, testified that his understanding was that "you have to disclose intellectual property that reads on the standard." (Kellogg, Tr. 5311). Kellogg also stated that "[s]ometimes we disclose intellectual property that doesn't [read on the standard] and one would question why. It adds confusion." (Kellogg, Tr. 5311).

758. Another opinion was that the EIA/JEDEC patent policy extended to patents and patent applications that "might be

involved" in the standards under development. (CX 208A at 19 ("obligation of all participants to inform the meeting of any knowledge they may have of any patents, or pending patents, that might be involved in the work they are undertaking"); G. Kelley, Tr. 2705 ("there were many work items that occurred on the committee that did not become standards . . . My definition says that any claim that might apply to the work of the committee it was required to disclose."); Landgraf, Tr. 1693-94 (disclose patents or applications "that would potentially be impacting the standard or proposed standard."); Lee, Tr. 6595-96; Rhoden, Tr. 307; Sussman, Tr. 1346 (participants must disclose where there is a "gray" area); CX 2057 at 203-04 (Meyer, Dep.) (disclosed patent when "sufficiently close" to work of JEDEC); Williams, Tr. 910-11 (if "there would be a reasonable possibility that the patent was going to be associated with the work of JEDEC, that you ought to say, hey, I've got something I'm patenting here or there's something that you're talking about that I've got some IP on.")).

759. Yet another opinion was that the policy applies "if the intellectual property has any relevance to the work that's going on, it might be involved – we're not asking the people that are disclosing to actually try to do a determination of whether it applies or doesn't apply. We're saying if it's related, in the same general area, . . ." (Rhoden, Tr. 322-23).

760. This conflict in trial testimony highlights the ambiguity of the JEDEC policy. (F. 718-39).

d. Trial Testimony Conflicts Regarding the Timing of Disclosure

761. Consistent with the EIA patent policy which encourages disclosure of essential patents, early disclosure was encouraged at JEDEC. (J. Kelly, Tr. 1955-56; Williams, Tr. 772; 910-11).

762. Some members understood this to mean that disclosure was expected "[i]f there is any suggestion that the committee's work should move in a certain direction." (Williams, Tr. 1984).

763. Another opinion was that any obligation that may have existed was not triggered until the time that a proposal was balloted for approval. (G. Kelley, Tr. 2707). JC 42.3 Chair G. Kelley testified "[t]he policy at JEDEC was that the disclosure should occur as soon as possible in the discussion of the material and certainly by the time it was balloted." (G. Kelley, Tr. 2702; *see also* CX 2057 at 211 (Meyer, Dep.) (testimony by Siemens JEDEC representative Willi Meyer that although it was "good practice" to notify the committee before balloting, "the ballot was considered the deadline when it should have been done")).

764. Cray representative Grossmeier, although he testified that "if a patent holder has a patent that in any way was applicable to a proposed standard, they were to disclose that at the time of balloting within the committee," pointed out that "[t]here's probably thousands of patents that are applicable to every device that's built, basically semiconductor technology patents that undoubtably are being duplicated by other companies. You can't disclose every – I mean, there would be lists of thousands of patents on every standard." (Grossmeier, Tr. 10945, 10956).

765. Yet another opinion was that disclosure was not tied to any procedural formality in the JEDEC process. (J. Kelly, Tr. 1983-85; Rhoden, Tr. 488-89).

H. The Scope of the EIA/JEDEC Patent Policy

1. Disclosures Were Encouraged and Voluntary

766. The controlling EIA manuals do not refer to or impose a mandatory obligation to disclose intellectual property. (*See* CX 204 at 4; CX 203A at 11; JX 54 at 9-10; *see supra* F. 633-38).

767. JEDEC manuals also do not impose any mandatory disclosure duty. JEP 21-H, in effect when Rambus joined JEDEC, states that "JEDEC standards are adopted without regard to whether or not their adoption may involve patents" and does not provide any further guidance regarding intellectual property. (CX 205 at 20; *see supra* F. 606-32). JEP 21-I refers to, but does not impose, an obligation to disclose intellectual property. (CX 208 at 19, 26; *see supra* F. 610-32).

768. The committee forms including the membership application, sign-in/attendance roster, committee ballot, members' manual, and patent tracking list do not refer to or impose an obligation to disclose intellectual property, although the committee ballot requests those aware of patents involved in the ballot to "please" alert the committee. (CX 601 at 1-2; CX 306 at 1-2; CX 252A at 2; RX 507 at 15; *see supra* 646-69).

769. The contemporaneous correspondence also shows that disclosure was voluntary. (RX 669 at 3 (EIA, on behalf of JEDEC, told the FTC in a January 22, 1996 letter that it "encourage[s] the early, voluntary disclosure of patents that relate to the standards in work."); RX 742 at 1 (statement in JEDEC Secretary's 7/10/96 memorandum to JEDEC Council members that the EIA "encourage[s] early voluntary disclosure of any known essential patents"); RX 1585 at 1 (statement in JEDEC Secretary's 2/11/00 email that "[d]isclosure of patents is a very big issue for Committee members and cannot be required of members at meetings")).

770. Moreover, there is no evidence that any JEDEC member objected when Gordon Kelley of IBM and Hans Wiggers of Hewlett-Packard announced at JEDEC meetings that they would not be disclosing any intellectual property from their companies. (JX 15 at 6; RX 420 at 2; JX 18 at 8; Wiggers, Tr. 10592-94; *see supra* F. 691-700).

771. Complaint Counsel did not provide sufficient evidence from which to find that the EIA/JEDEC patent policy in effect while Rambus was a member did anything more than encourage the disclosure of patents essential to the standards at balloting.

2. Patent Applications or Intentions To File Patent Applications Were Not Covered by the Policy

772. The controlling EIA manuals refer to "patents," "known patents," and "patented item or process," but never refer to patent applications. (*See, e.g.*, CX 204 at 4; CX 203A at 11; JX 54 at 9-10; *see supra* F. 633-38). In addition, there was testimony from G. Kelley that EIA's definition of the word "patent" did not include patent applications. (G. Kelley, Tr. 2686-87; 2695-97).

773. The contemporaneous documents show that the JEDEC patent policy encouraged the disclosure of patents, not patent applications or intentions to file patent applications. The minutes of the February 2000 meeting of the JEDEC Board of Directors state that disclosure of patent applications is "not required under JEDEC bylaws." (RX 1570 at 13). A few days after the meeting, JEDEC Secretary Ken McGhee explained to the members of JEDEC 42.4 that the disclosure of patent applications went "one step beyond" the policy and that even disclosure of patents could not be required: "Disclosure of patents is a very big issue for Committee members and cannot be required of members at meetings." (RX 1582 at 1).

774. The most that the record evidence can be understood to support is an argument that *presenters* were expected to disclose patent applications that related to technologies they were asking that JEDEC standardize. (RX 507 at 15; McGrath, Tr. 9273-74).

3. Members Were Encouraged To Disclose Patents That Were Essential To Practice the Standard

775. Disclosure was only encouraged of patents that were "essential" to a standard, i.e., those patents that were necessary for the manufacture or use of a product that complied with the standard. (CX 203A at 11 (standards that "call for the use of patented items); JX 54 at 9 (standards "that call for the exclusive use of a patented item or process"); CX 208 at 19 (standards that "require the use of patented items"); RX 742 at 1 ("known essential patents")).

776. Hewlett-Packard representative Thomas Landgraf testified that he understood the patent policy to involve disclosure if "the standard required someone else's idea to be used . . . in order for it to operate." (Landgraf, Tr. 1695).

777. JC 42.3 Chair and IBM representative Gordon Kelley testified that the disclosure duty was triggered by a patent claim that "reads on or applies" to the standard, meaning that "if you exercise the design or production of the component that was being standardized [it] would require use of the patent." (G. Kelley, Tr. 2706-07).

778. Another IBM JEDEC representative, Mark Kellogg, testified that his understanding was that "you have to disclose intellectual property that reads on the standard." (Kellogg, Tr. 5311). Kellogg also stated that "[s]ometimes we disclose intellectual property that doesn't [read on the standard] and one would question why. It adds confusion." (Kellogg, Tr. 5311).

4. There Was No Duty To Search for Intellectual Property Issues

779. It was undisputed at trial that JEDEC representatives had no obligation to do any investigation, research or inquiry of their own company or its lawyers regarding possible intellectual

property interests relating to JEDEC work. (Rhoden, Tr. 623-24; G. Kelley, Tr. 2451, 2700-01; J. Kelly, Tr. 1966-68; CX 2057 at 189, 193 (Meyer, Dep.); *see also* RX 1712 at 8 (no duty to search under ANSI Guidelines)).

5. The Policy was Limited To Participants With Actual Knowledge

780. The patent policy applied only to people with "actual knowledge." (Rhoden, Tr. 623-24). JEDEC Board Chairman Desi Rhoden testified that the disclosure obligations under the JEDEC patent policy were "triggered by the actual knowledge of the people that were involved, and that would not be just the representative at the meeting, but all of the people that would have been involved in . . . The knowledge of the people that are involved in the process." (Rhoden, Tr. 624; J. Kelly, Tr. 1970).

781. Rambus's JEDEC representative, Richard Crisp, testified that during the time that Rambus was a JEDEC member, he: (1) had not seen any Rambus patent application with claims over an SDRAM that used any of the four features at issue here; and (2) did not know one way or the other whether Rambus's pending patent applications covered JEDEC-compliant SDRAMs using any of those features. (Crisp, Tr. 3540-43; 3461-66).

6. The Patent Policy Did Not Apply After a Company Withdrew From JEDEC

782. After a company left JEDEC it had no obligations under the patent policy. (*See* G. Kelley, Tr. 2700-01).

7. If Disclosure Was Made, It Was Encouraged No Later Than the Time of Balloting

783. Consistent with EIA patent policy to encourage early disclosure of relevant patents, early disclosure was encouraged at JEDEC. (J. Kelly, Tr. 1955-56; Williams, Tr. 772, 910-11).

784. The committee ballot was considered the deadline for disclosure. (G. Kelley, Tr. 2707; Grossmeier, Tr. 10945). JC 42.3 Chair G. Kelley testified "[t]he policy at JEDEC was that the disclosure should occur as soon as possible in the discussion of the material and certainly by the time it was balloted." (G. Kelley, Tr. 2702; CX 2057 at 211 (Meyer, Dep.) (testimony by Siemens JEDEC representative Willi Meyer that although it was "good practice" to notify the committee before balloting, "the ballot was considered the deadline when it should have been done")).

785. This is consistent with the patent tracking list which asked the committee chair to "resolve patent status prior to (choose one)," followed by a list of events, from presentation to balloting. (CX 34 at 7; CX 711 at 169; JX 27 at 7-8; JX 28 at 15-18).

VII. JEDEC 42.3 COMMITTEE MEMBERS WERE NOT MISLED BY RAMBUS ON ISSUES RELATING TO RAMBUS INTELLECTUAL PROPERTY

A. JEDEC Committee Leaders and Members Were Fully Aware of Rambus's Patents With Respect To Features Being Considered for Incorporation into JEDEC Standards

1. Crisp Did Not Mislead JEDEC At the May 1992 Committee Meeting Regarding Rambus's Intent To Seek Patent Rights Over Certain SDRAM Features

a. IBM and Siemens

786. In the spring of 1992, IBM and Siemens (whose former semiconductor division is now called Infineon Technologies) were cooperating on a joint venture to develop and produce a new DRAM design. (G. Kelley, Tr. 2532; CX 2088 at 277-78, 310 (Meyer, Infineon Trial Tr.)).

787. Both the Siemens JEDEC representative, Willi Meyer, and the IBM JEDEC representative, Gordon Kelley, were involved in the Siemens/IBM DRAM development efforts in the spring of 1992. (G. Kelley, Tr. 2620-21). The efforts included a consideration of the Rambus technology. (G. Kelley, Tr. 2627).

788. In March 1992, G. Kelley prepared a memorandum regarding Rambus. (RX 240 at 1). G. Kelley's March 19, 1992 memorandum refers to "unique (and probably patented) Rambus protocol" and "special Microprocessor and DRAM interface (other than industry standard)." (RX 240 at 1). G. Kelley's memorandum also states that he had asked an IBM in-house lawyer "to get me a copy of Rambus patents." (RX 240 at 1).

789. On April 23, 1992, G. Kelley attended a presentation at IBM by Rambus founder Mike Farmwald and Rambus executive David Mooring. (G. Kelley, Tr. 2631; RX 273 at 1).

790. According to handwritten notes of the April 23, 1992 Rambus/IBM meeting a Rambus representative stated at the meeting that Rambus intended to obtain "license fee + royalties from IC company." (CX 2355 at 1). The notes also state that Rambus "want[s] to set industry std." (CX 2355 at 1).

791. In April 1992, Gordon Kelley prepared a "Rambus Assessment" along with two other IBM employees, Dr. Beilstein and Michael Clinton. (RX 279 at 1). The "Rambus Assessment" is dated April 24, 1992, the day after Kelley had attended the presentation by Rambus. (RX 279 at 1; G. Kelley, Tr. at 2635).

792. The April 1992 "Rambus Assessment" that G. Kelley co-authored refers to "Unique Rambus Features/Attributes." (RX 279 at 1). The "Rambus Assessment" also states that "Intel is Rambus licensee" and notes a "potential future Intel memory strategy to marry . . . 586/686 processor with Rambus protocol to corner PC/notebook market with state of the art performance." (RX 279 at 4).

793. The "Rambus Assessment" states that "Rambus can work technically" and notes "the risk is whether it becomes a standard for the low end – bulk of DRAM bit volume – and that it provides a simple low end solution for anyone to get into the PC business." (RX 279 at 8).

794. The "Rambus Assessment" states that "[i]f Rambus fails to become standard, then it is business as usual for BTV [the acronym for IBM's Burlington, Vermont operations] and the SDRAM has a significant chance of being standard." (RX 279 at 7).

795. It is apparent from G. Kelley's March and April 1992 analyses of Rambus that he was aware of Rambus technology, and its prospects for success in the spring of 1992. (See RX 279; RX 273; RX 240).

796. One week after G. Kelley finalized the April 24, 1992 "Rambus Assessment," he participated in a conference call with Siemens JEDEC representative Willi Meyer. The call included a discussion of Rambus. (RX 286A at 1).

797. Meyer prepared an April 30, 1992 memorandum reflecting the conference call which states in part: "Rambus: Visited key in-house IBM users. IBM is still keeping its eye on RAMBUS. RAMBUS has announced a claim against Samsung for USD 10 million due to the similarity of the SDRAM with the RAMBUS storage device architecture. For that reason, IBM is seriously considering to preemptively obtain a license as soon as possible (at an introductory price)." (RX 286A at 2; CX 2088 at 317-19 (Meyer, Infineon Trial Tr.)).

798. Meyer testified that during the conference call, Gordon Kelley had provided the Rambus-related information contained in Meyer's April 30, 1992 memorandum. (RX 286A; CX 2088 at 317-19 (Meyer, Infineon Trial Tr.)).

799. Siemens executive Martin Peisl similarly testified that the information regarding Rambus that is contained in Meyer's April 30, 1992 memorandum "seems to be information coming from IBM or Gordon Kelley." (Peisl, Tr. 4517).

800. G. Kelley and Meyer were both aware, as of April 30, 1992, of a possibility that Rambus might assert some intellectual property claims "due to the similarity of the SDRAM with the RAMBUS storage device architecture." (RX 286A at 2).

801. An April 16, 1992 IBM memorandum referenced the fact that an-in house lawyer, J. Walter, had been asked to review and comment upon Rambus related intellectual property issues. (RX 272 at 2).

802. Meyer also wrote a separate memorandum dated April 30, 1992 that stated in part that "[t]he original idea behind the SDRAM is based on the basic principle of a simple pulse input (IBM toggle pin) and the complex RAMBUS structure." (RX 285A at 5). This memorandum also demonstrates Meyer's awareness of similarities between the SDRAM device and the "RAMBUS structure." (*See* RX 285A at 5).

803. On May 6, 1992, Meyer prepared a chart showing the "Pros" and "Cons" of "Sync DRAM," "Rambus DRAM," and "Cached DRAM." (RX 289 at 1).

804. In his May 6, 1992 "Pros" and "Cons" chart, Meyer stated that the "2-bank" synchronous DRAM "may fall under Rambus patents." (RX 289 at 1). Meyer testified that he did not think Rambus had patents at the time covering 2-bank synchronous DRAM but that there was the potential it could obtain such patents. (CX 2089 at 44 (Meyer, Infineon Trial Tr.)).

805. Meyer testified that at the time, he thought there was a potential that Rambus would obtain patents covering two-bank

features that may be included in SDRAMs. (CX 2089 at 44 (Meyer, Infineon Trial Tr.)).

806. Meyer also testified that in 1992, "we were absolutely sure that Rambus was trying to get patents." (CX 2088 at 75 (Meyer, Infineon Trial Tr.)).

b. The May 1992 JC 42.3 Meeting

807. On May 7, 1992, Meyer and G. Kelley attended a JC 42.3 subcommittee meeting in New Orleans, Louisiana. (CX 34).

808. The May 1992 meeting was Richard Crisp's first formal JC 42.3 subcommittee meeting as Rambus's JEDEC representative, (CX 34 at 1; Crisp, Tr. 2929), although he had attended a JC 42.3 task group meeting on April 9 and 10, 1992. (Crisp, Tr. 3009-10).

809. At the meeting, Gordon Kelley asked Crisp if he would like to comment on whether Rambus had patents or potential patents covering two bank design. Crisp declined to comment. (CX 673 at 1; CX 2089 at 136-37 (Meyer, Infineon Trial Tr.)).

810. Howard Sussman of NEC commented to the group that he had seen a copy of a Rambus's foreign patent application. (CX 2092 at 128 (Crisp, Infineon Trial Tr.)). According to Crisp, the essence of the comment was that Sussman had obtained a copy of the application from the foreign patent office, had read it and concluded that it should not be a concern for the JEDEC standardization effort because, according to Sussman, "many, many claims . . . are anticipated by prior art." (CX 673 at 1).

811. The witnesses who testified about the May 1992 exchange between G. Kelley and Crisp were Kelley, Crisp, Siemens representative Willi Meyer, IBM representative Mark Kellogg and Intel representative Samuel Calvin. (G. Kelley, Tr.

2662; Crisp, Tr. 3066; Kellogg, Tr. 5055-56; Calvin, Tr. 1066-69; CX 2089 at 169, 136 (Meyer, Infineon Trial Tr.)).

812. Calvin, the Intel representative, testified that he recalls that at the JEDEC meeting, Crisp was asked if he cared to comment about whether Rambus had patents or intellectual property that covered a particular subject. (Calvin, Tr. 1068-69). Calvin recalls that Crisp declined to comment. (Calvin, Tr. 1068-70).

813. Meyer, who was Siemens's primary JEDEC representative between 1992 and 1996, testified that at the May 1992 meeting, he asked G. Kelley to ask Crisp "whether [he] would like to comment" about whether Rambus had patents relating to the use of two banks in a DRAM. (CX 2089 at 133-34 (Meyer, Infineon Trial Tr.); CX 2057 at 66 (Meyer, Infineon Dep.)).

814. Meyer testified that "[t]he way how Kelley formulated the question was: Do you want to give a comment on this?" (CX 2088 at 136, 164 (Meyer, Infineon Trial Tr.)). Meyer testified that Crisp "just shook his head." (CX 2088 at 136, 164 (Meyer, Infineon Trial Tr.)).

815. Meyer's trip report of the May 1992 meeting states in part: "Siemens and Philips concerned about patent situation with regard to Rambus and Motorola. No comments given." (RX 297 at 5).

816. Crisp sent an email on May 6, 1992 that described his exchange with Kelley in this manner: "Siemens expressed concern over potential Rambus Patents covering designs. Gordon Kelley of IBM asked me if we would comment which I declined." (CX 673 at 1).

817. Gordon Kelley testified that Siemens representative Willi Meyer had raised an "issue of concern with Rambus and Rambus

patents" at the May 1992 meeting. (G. Kelley, Tr. 2662). Kelley recalls that Meyer had asked Crisp if he knew whether Rambus "had patentable material on the concept of the synchronous DRAM." (G. Kelley, Tr. 2543). Kelley recalls that Crisp declined to comment in response to that question. (G. Kelley, Tr. 2662).

818. G. Kelley testified that he could not recall whether he had said anything at the May 1992 JEDEC meeting about possible Rambus patent claims. (G. Kelley, Tr. 2544).

819. G. Kelley also testified that a "no comment" from a JEDEC member in response to a question about intellectual property is "unusual" and "surprising" and "is notification to the committee that there should be a concern. . . ." (G. Kelley, Tr. 2579).

820. IBM representative Mark Kellogg prepared contemporaneous handwritten notes at the May 1992 JEDEC meeting that refer to the concerns Meyer had raised. (RX 290 at 3). Kellogg's notes state: "Siemens: Kernel of chip similar to Rambus. Patent concerns? (No Rambus comments)." (RX 290 at 3).

821. Kellogg testified that when he used the phrase "kernel of the chip" in his notes, he was referring to Meyer's concern that "the fundamental architecture of the SDRAM device" was "similar to Rambus." (Kellogg, Tr. 5324).

822. Kellogg testified that he took his notes at the May 1992 meeting in part to act as "a log of events" and "also to initiate action on my part or the part of others." He said that this discussion "would have been a flag, which is why I wrote it down." (Kellogg, Tr. 5322).

823. Kellogg testified that he considered the discussion a "flag" because JEDEC members were "describing possible intellectual property concerns which may affect our decision

process for synchronous DRAM." He testified that "[t]hat is a concern" and that "[t]he lack of response by Rambus is also a concern." (Kellogg, Tr. 5323).

824. The chairman of the meeting, Gordon Kelley, testified that prior to the May 1992 meeting Crisp had spoken to him about the possibility of Rambus scheduling a presentation concerning DRAM design. (G. Kelley, Tr. 2553). G. Kelley also testified that he had refused to allow Rambus to present its technology for standardization at JEDEC on this and another occasion, even though he had never barred any other member company from presenting its technology. (G. Kelley, Tr. 2649-58).

825. G. Kelley had a clear conflict of interest; he made and enforced his unilateral decision to bar Rambus from presenting its technology *two weeks* after he wrote in an internal company document that his company's interests were threatened by the Rambus technology and were best served if Rambus "fails to become standard." (RX 279 at 7). He did not disclose this conflict to Crisp or to anyone else. (G. Kelley, Tr. 2656-57).

c. PCT Application

826. A "PCT" application is an international patent application filed pursuant to the Patent Cooperation Treaty. (CX 1454 at 1). Rambus had filed a PCT application on April 16, 1991 that was identical in all material respects to the '898 application it had filed at the same time in the U.S. (Fliesler, Tr. 8811; *see* CX 1451; CX 1454).

827. Pursuant to the procedures governing applications filed under the Patent Cooperation Treaty, Rambus's PCT application became publicly available as of October 31, 1991. (CX 1454 at 1; First Set of Stipulations, Stip. 8).

828. NEC's Sussman testified that he did not find anything in the PCT application that "related to the work ongoing at JEDEC." (Sussman, Tr. 1445).

d. After the May 1992 JC-42.3 Meeting

829. Roughly one week after the May 1992 meeting, Siemens's JEDEC representative Willi Meyer also reported that: "Siemens and Philips: concerned about patent situation with regard to RAMBUS and MOTOROLA. No comments given. Motorola patents have priority over RAMBUS'. RAMBUS patents filed but pending." (RX 297 at 5).

830. In June 1992, G. Kelley gave a presentation about Rambus to a group of about 30 engineers. Half of the engineers were from IBM; half were from Siemens. (G. Kelley, Tr. 2658-59).

831. In connection with his June 1992 presentation, G. Kelley prepared a chart entitled "COMPARE ALTERNATIVES for Future High Performance, High Volume DRAM Designs." The chart listed "Pros" and "Cons" of Sync DRAMs and Rambus DRAMs. One of the two "cons" listed for Sync DRAMs was "Patent Problems? (Motorola/Rambus)." (RX 303 at 1; G. Kelley, Tr. 2545).

832. Kelley testified that he included the reference to possible "patent problems" involving Motorola and Rambus in his June 1992 "Pros" and "Cons" chart because he "was notifying the people involved in the design of the joint work that was going on between IBM and Siemens that there was concern about potential patent problems as I had heard at the JEDEC meeting about Motorola and Rambus intellectual property, and I wanted the group to recognize that there was this concern." (G. Kelley, Tr. 2545).

833. Meyer testified that in September 1992 he had prepared a presentation entitled "What Is Rambus?" (RX 321 at 1; CX 2089 at 66-67 (Meyer Infineon Trial Tr.)). Meyer delivered this presentation to, among others, Dr. Schumacher, the current CEO of Infineon. (CX 2089 at 66-67 (Meyer, Infineon Trial Tr.)).

834. In his September 1992 presentation, Meyer referred to Rambus as a "deadly menace to the established computer industry." (RX 321 at 2). He also suggested that to "protect" the computer industry, someone could "buy Rambus and dump it." (RX 321 at 3). Meyer testified that he thought some of his competitors were so worried about Rambus that they might purchase the entire company and "bury the technology." (CX 2089 at 89 (Meyer Infineon Trial Tr.)).

835. G. Kelley testified, in a 2001 deposition, that he had had conversations with Meyer after 1992 regarding the potential applicability of Rambus patents to SDRAM devices. At trial, he could not recall the substance of these conversations. (G. Kelley, Tr. 2664-65).

2. PCT Application Discussed At the September 1993 Meeting

836. At the September 1993 meeting Crisp disclosed to the Committee the issuance to Rambus on September 7, 1993, of United States Patent No. 5,243,703. (Crisp, Tr. 3173; First Set of Stipulations, Stip. 11).

837. The '703 patent was the first Rambus patent and had issued shortly before the meeting. The '703 patent resulted from a divisional application of an original application, Serial No. 07/510,898 ('898 application), filed in April 1990. (First Set of Stipulations, Stip. 11).

838. The specification and drawings of the ‘703 patent are substantially the same as those contained in the ‘898 application. (Fliesler, Tr. 8812, 8817; *see* RX 425 at 1; CX 1451 at 1).

839. There was an additional discussion of Rambus’s PCT application at a JEDEC meeting in September 1993, after Rambus representative Richard Crisp disclosed that Rambus had obtained its first U.S. patent (the ‘703 patent). According to Siemens’s JEDEC representative Willi Meyer:

> During the meeting, which was the same meeting in which the Rambus ‘703 patent was disclosed with its full patent number, and a participant, I’m not quite sure, either the participant or the chairman or the JEDEC official, somebody at the meeting said by the way, there is also something called like a WIPO, World Intellectual Property, and he offered to anybody who was interested in it to get the number from him, the reference number, and to step up to him after the meeting to do so.

(CX 2058 at 298 (Meyer, Infineon Dep.)).

840. Meyer also testified that he obtained the serial number for Rambus’s WIPO application at the JEDEC meeting and “sent it back to the [Siemens] patent department.” (CX 2089 at 112 (Meyer, Infineon Trial Tr.)).

841. A few months later, in March 1994, Meyer prepared a memorandum about Rambus for a Siemens engineering manager named Penzel. The memorandum stated in part that “[a]ll computers will (have to be) built like this some day, but hopefully without royalties to RAMBUS.” (RX 488A at 1; CX 2089 at 124 (Meyer, Infineon Trial Tr.)).

3. The May 1995 JC 42.3 Meeting

842. At the May 24, 1995 JEDEC meeting, presentations were made by several JEDEC members regarding a "next generation" memory technology called "SyncLink." (JX 26 at 10-11). At this meeting there were a number of inquiries about possible patent issues pertaining to SyncLink. G. Kelley of IBM asked whether or not HP, Hyundai, Mitsubishi or TI had any patents covering any of the matters being presented; all of these companies stated that they did not. (CX 711 at 72; Crisp, Tr. 3265-66).

843. At this same meeting, Sam Calvin of Intel and G. Kelley also inquired whether there were any Rambus patents covering the SyncLink technology. (CX 711 at 73; Crisp, Tr. 3266). When Crisp did not respond to this inquiry at the meeting he was asked by Kelley to go back to Rambus and then report back to the Committee whether Rambus knew of any patents, especially Rambus patents, that may read on the SyncLink technology. (CX 711 at 73; CX 794 at 4; Crisp, Tr. 3267-68).

844. Crisp wrote an email informing the Rambus executives, engineering managers and business development and marketing groups of this development. In that email he listed a few ideas he had of Rambus intellectual property relating to SyncLink. (CX 711 at 68, 73). He also suggested that Rambus review its current issued patents and see what it had to work against SyncLink. (CX 711 at 68, 73). He recommended that Rambus consider responding to the JEDEC request by "simply provid[ing] a list of patent numbers which have issued" and telling members to decide for themselves what does and does not infringe. He added, however, that if the Rambus patents were "not a really key issue . . . Then it makes no sense to alert them to a potential problem they can easily work around," and that "we may not want to make it easy for all to figure out what we have especially if nothing looks really strong." (CX 711 at 68, 73).

845. Rambus executives heeded Crisp's advice and Crisp testified at trial that at the September meeting, he made "no statement to the 42.3 subcommittee that [he] believed that SyncLink would violate Rambus patents." (Crisp, Tr. 3316).

846. A few days after the May 1995 meeting, Crisp sent an email to Reese Brown, a JEDEC consultant, that included a reference to "Ramlink," the foundation for the proposed SyncLink device. (CX 711 at 80-82; Gustavson, Tr. 9281-83). Crisp's email stated in part that he took exception to the fact that Brown had posted a copy of the ballot for the proposed IEEE Ramlink standard on the JEDEC reflector. (CX 711 at 76-78; Crisp, Tr. 3280-82).

847. When Brown responded to Crisp and suggested that Crisp's exception was partly due to the fact that Crisp saw the standard as competition to Rambus, Crisp responded that the proposed IEEE standard was not real and had patent issues associated with it. (CX 711 at 79-80; Crisp, Tr. 3282-83). Crisp admitted that he had not planned ahead of time to disclose this but did it in the heat of the moment. (Crisp, Tr. 3282-83).

848. Brown forwarded Crisp's email to Hans Wiggers, the JEDEC representative for Hewlett-Packard, who was chairing the Ramlink/Synclink working group. (CX 711 at 88-91; Gustavson, Tr. 9282-83).

849. On June 10, 1995, Wiggers copied his response to Crisp's comments to, among others, Gordon Kelley, the Chairman of the JC 42.3 subcommittee, along with a request that Crisp clarify his comments about patents relating to Ramlink. (CX 711 at 90-91).

850. On June 12, 1995, Kelley prepared an internal IBM memorandum that stated with respect to the SyncLink device that "the Rambus patents should be closely reviewed." (RX 575 at 7).

851. On June 13, 1995, Crisp sent an email to Wiggers that stated:

> [R]egarding patents, I have stated to several persons that my personal opinion is that the Ramlink/Synclink proposals will have a number of problems with Rambus intellectual property. We were the first out there with high bandwidth, low pincount; DRAMs, our founders were busily at work on their original concept before the first Ramlink meeting was held, and their work was documented, dated and filed properly with the US patent office. Much of what was filed has not yet issued, and I cannot comment on specifics as these filings are confidential.

(RX 576 at 2).

852. Crisp's email to Wiggers also stated that:

> I was asked at the last JEDEC meeting to report on our patent coverage relative to SyncLink as proposed at JEDEC at the next meeting in Crystal City in September. Our attorneys are currently working on this, so I think I will be in a position to make some sort of official statement at that time and plan to do so. In the meantime, I have nothing else to say to you or the rest of the committee about our patent position. If you want to search for issued patents held by Rambus, then you may learn something about what we clearly have covered and what we do not. But I must caution you that there is a lot of material that is currently pending and we will not make any comment at all about it until it issues.

(RX 576 at 2).

853. In August 1995, Rambus warned the SyncLink working group that its work might infringe Rambus's intellectual property. The minutes of the August 22, 1995, meeting of the SyncLink working group state in part as follows:

> Richard Crisp, of RamBus, informed us that in their opinion both RamLink and SyncLink may violate RamBus patents that date back as far as 1989. Others commented that the RamLink work was public early enough to avoid problems, and thus might invalidate such patents to the same extent that they appear to be violated. However, the resolution of these questions is not a feasible task for this committee, so it must continue with the technical work at hand.

(RX 592 at 2).

854. Although the August 21, 1995 SyncLink meeting was held under the auspices of the standards setting body IEEE, not JEDEC, each of the seven companies represented at the SyncLink meeting was also a JEDEC member company, and at least five of the engineers present at the SyncLink meeting were JEDEC representatives who attended the next JEDEC 42.3 meeting on September 11, 1995. (*See* First Set of Stipulations, Stip. 21).

4. The September 1995 JC 42.3 Meeting

855. At the September 1995 JEDEC meeting, Crisp presented a written response to the questions about intellectual property that had been raised at the May 1995 meeting. The statement included this passage:

> At this time, Rambus elects to not make a specific comment on our intellectual property position relative to the SyncLink proposal. Our presence or silence at committee meetings does not constitute an endorsement of any proposal under the

> committee's consideration nor does it make any statement regarding potential infringement of Rambus intellectual property.

(JX 27 at 26). Rambus's statement was published in full in the official JEDEC minutes of the September 1995 meeting. (JX 27 at 26).

856. A September 1995 meeting report prepared by Motorola JEDEC representative Mark Farley noted that "Rambus made a non-statement statement to the committee saying that Rambus has been developing this technology for five+ years and has a substantial number of patents related to high-bandwidth DRAMs." (RX 615 at 1). Farley also reported that "SyncLink told Motorola confidentially that there were very likely patents violated by their proposal." (RX 615 at 1).

857. Intel representative Samuel Calvin testified that at that time, he understood from Rambus's September 11, 1995 statement that any silence by Rambus at JEDEC meetings should not be taken as an indication that it did not have intellectual property relating to JEDEC's work. (Calvin, Tr. 1070).

5. Rambus Met With Manufacturers and Suppliers

858. In the course of the discussion of the Rambus letter at the September 1995 Committee meeting, Crisp reminded the Committee that Rambus in the past had reported a Rambus patent to the Committee, referring to the disclosure to the Committee of the Rambus '703 patent in September 1993. (Crisp, Tr. 3312). Crisp "reminded them of the 14 patents relating to SDRAMs, and that our silence was not an agreement that we have no IP related to SyncLink, . . . [and I] reminded them that the member companies are constantly receiving patents on things they are standardizing and that they seldom report the patents." (CX 711 at 167).

859. During a meeting in Korea in October 1995, Rambus informed LG Semiconductor that Rambus had or might obtain intellectual property rights that might apply to SDRAMs. (CX 2111 at 315-16 (Tate Dep.)).

860. During a meeting in Korea in October 1995, Rambus informed Samsung that SyncLink and fast SDRAMs were heading in the direction where they might infringe future Rambus patents. (CX 2111 at 317 (Tate Dep.)).

861. During a meeting in Japan in October 1995, Rambus informed NEC that SyncLink and new SDRAMs (SDRAMs using a PLL or dual-edge clock) might end up in a position where they infringed future Rambus patents. (CX 2111 at 320-21 (Tate Dep.)).

862. During a meeting in Japan in October 1995, Rambus informed OKI of the possibility that there would be Rambus intellectual property that might apply to SyncLink and new SDRAMs. (CX 2111 at 320-22 (Tate Dep.)).

863. During a meeting with Intel in October 1995, Rambus informed Intel that it did not see how future memory chips could meet performance goals without using some or all of Rambus's inventions. (CX 2111 at 323-26 (Tate Dep.)).

864. DRAM manufacturer Micron Technology demonstrated its concern about Rambus's patents in 1995 and 1996. On November 7, 1995, Micron executive Jeff Mailloux sent a memo entitled "RAMBUS Inc. patents" to several other Micron employees, including JEDEC representative Terry Walther. (RX 630 at 1). Mailloux's memorandum stated in part as follows: "[a]ttached are abstracts for the patents that have been granted to RAMBUS Inc. so far . . . . Please consider both the quality (is there prior art?) and the breadth (apply to more than just RAMBUS?) of the patents." (RX 630 at 1).

865. Mitsubishi's Japanese patent department was also apparently considering any prior art to Rambus's patents in November 1995. (RX 1041A at 1 ("we have obtained CRAY Corporation's patents to investigate the prior art for the patents owned by Rambus Inc. . . .")).

866. In January 1996, the concerns of Micron and others about Rambus's intellectual property were reflected in the minutes of the SyncLink Consortium: "Rambus has 16 patents already, with more pending. Rambus says their patents may cover our SyncLink approach even though our method came out of early RamLink work. Micron is particularly concerned to avoid the Rambus patents, though all of us share this concern." (RX 663 at 2).

867. Others who took a close look at Rambus's intellectual property in this time period included Dr. David Gustavson, the Secretary of the SyncLink Consortium, who reviewed several European patent applications that Rambus had filed. (Gustavson, Tr. 9286). Dr. Gustavson has testified that he recognized immediately upon reviewing the Rambus patent applications that they had a broad scope that would apply to virtually any memory device, but that he believed the applications would never be allowed in light of their breadth. (Gustavson, Tr. 9287).

868. Two Apple engineers, David James and Glen Stone, reviewed the Rambus patent applications along with Gustavson. (Gustavson, Tr. 9286).

6. JEDEC Members Viewed Rambus's Patents As a Collection of Prior Art

869. Crisp's May 6, 1992 email states that:

> In response to the patent issue, Sussman stated that our patent application is available from foreign patent offices, that he has a copy, and noted many, many claims that we make that are anticipated by prior art. He also stated the Motorola patent

> predated ours (not the filing date!) and it too was anticipated by prior art.

(CX 673 at 1).

870. The handwritten notes taken contemporaneously at the May 1992 meeting by IBM representative Mark Kellogg similarly indicate: "NEC: Rambus International Patent 150 pages, Motorola patents/Rambus patent – suspect claims won't hold." (RX 290 at 3).

B. The Dell Consent Order and Rambus's Last JEDEC Meeting – December 1995 To January 1996

871. The final JEDEC meeting attended by Rambus was the meeting in December 1995. (CX 2104 at 853-54 (Crisp, Micron Dep.)). Rambus did not pay in response to a dues invoice sent by JEDEC in January 1996. (CX 887). Rambus responded to the dues invoice by a letter dated June 17, 1996, in which it informed JEDEC that it was not renewing its membership in the organization. (CX 887).

872. Also in December 1995, Rambus's patent counsel, Lester Vincent, sent Diepenbrock, Rambus's IP manager, materials relating to a proposed FTC consent order involving Dell Computer. (CX 1990 at 1; Diepenbrock, Tr. 6222). Vincent described the case as involving charges that Dell restricted competition in the personal computer industry and undermined the standard setting process by threatening to exercise undisclosed patent rights against computer companies adopting standard technology. (CX 1990 at 1).

873. "[L]egal guidance not to attend JEDEC escalated" after the "situation with Dell." (CX 2112 at 222 (Mooring, Dep.)). Rambus's lawyers felt that, although Rambus's situation was not the same as the situation in the Dell case, the risk that an equitable estoppel defense might be raised justified withdrawing from

JEDEC, assuming that the benefits of attendance did not outweigh the risks. (CX 3124 at 196-97 (Vincent Infineon Dep.)).

874. Rambus's separation from JEDEC was formalized on June 17, 1996, when Rambus sent a letter to the JEDEC office that stated:

> I am writing to inform you that Rambus Inc. is not renewing its membership in JEDEC.
>
> Recently at JEDEC meetings the subject of Rambus patents has been raised. Rambus plans to continue to license its proprietary technology on terms that are consistent with the business plan of Rambus, and those terms may not be consistent with the terms set by standards bodies, including JEDEC. A number of major companies are already licensees of Rambus technology. We trust that you will understand that Rambus reserves all rights regarding its intellectual property. Rambus does, however, encourage companies to contact Dave Mooring of Rambus to discuss licensing terms and to sign up as licensees.
>
> To the extent that anyone is interested in the patents of Rambus, I have enclosed a list of Rambus U.S. and foreign patents. Rambus has also applied for a number of additional patents in order to protect Rambus technology.

(*See* CX 887).

875. Rambus included with the letter a list of patents but did not include any reference to patent applications. Nor did the list include the '327 patent. (CX 887).

876. The evidence is inconclusive regarding whether the '327 patent was left off of the list intentionally or inadvertently. (CX 887).

C. Ongoing Discussions of Rambus Patents by JEDEC Members After June 1996

877. In October 1996, [redacted] (RX 781 at 2 (*in camera*)).

878. In December 1996, Micron executive Jeff Mailloux wrote a memorandum to Micron CEO Steve Appleton that stated in part that:

> We have been investigating high speed DRAMs and the intellectual property associated with them for some time now. . . . We have also been investigating the prior art related to the area of high-speed DRAMs. From our research, we think many RAMBUS patents read on prior art or other patents.

(RX 829 at 2).

879. The minutes of the March 1997 JC 42.3 meeting reflect that during a presentation regarding an NEC proposal involving DDR SDRAM, a representative stated that "[s]ome on the committee felt that Rambus had a patent on that type of clock design." (JX 36 at 7).

880. Micron representative Terry Lee was present at the March 1997 JC 42.3 meeting. Lee had raised the concern about a possible Rambus patent at the meeting that is reflected in the minutes. (Lee, Tr. 6957-58; JX 36 at 7).

881. The NEC representative's trip report for the March 1997 JEDEC meeting supports Lee's recollection, for it includes the

following summary of the discussion regrading the NEC DDR proposal:

Company	*Comments*
Micron	This technique is patented by RAMBUS and they will not agree to the JEDEC patent policy.
Mosaid/VLSI	This may be a future bus concept. Future bus was invented before RAMBUS became a company, so this may not be a valid patent.

(RX 880 at 25).

882. The NEC DDR proposal, however, did not involve a "narrow bus" and was not "packetized." (Lee, Tr. 6961).

883. Lee agreed that by March 1997, he thought that Rambus might have intellectual property claims relating not just to RDRAMs but to the work of the JC 42.3 committee as well. (Lee, Tr. 6962-64).

884. On April 16, 1997, a Micron employee, Keith Weinstock, sent an email to various Micron employees that stated in part that "Rambus plans legal action to request royalties on all DDR memory efforts." (RX 920 at 2).

885. At the time he prepared his April 16, 1997 email, Weinstock was a Micron account representative with responsibility for Intel. (Lee, Tr. 6700).

886. Weinstock sent his April 16, 1997 email, and its statement that "Rambus plans legal action to request royalties on all DDR memory efforts," to Jon Biggs, with a copy to Terry

Walther, Jeff Mailloux, Terry Lee, Kevin Ryan, Gary Welch and Steve Trick. (RX 920 at 1).

887. At the time, Biggs was Weinstock's predecessor as the Micron account representative for Intel. (Lee, Tr. 6967). Mailloux was Micron's DRAM Marketing Manager at the time. (CX 3133 at 44-45 (Mailloux, Micron Dep.)). Walther was a JEDEC representative for Micron. (Lee, Tr. 6594, 6953). Welch was in Product Marketing at Micron, with responsibility for Rambus products. (Lee, Tr. 6967). Trick was a Micron employee responsible for module development. (Lee, Tr. 6973). Lee was in the Strategic Marketing department at Micron, reporting to Mailloux. He also attended JEDEC meetings frequently in the 1997-2000 time period. (Lee, Tr. 6591-95). Ryan was in a similar position as Lee and also attended JEDEC meetings in this time period. (Lee, Tr. 6601).

888. On April 17, 1997, Micron JEDEC representative Terry Walther responded to Weinstock's email and asked him to confirm the report about Rambus's intellectual property claims, asking "Does Rambus believe they have a patent on changing data on both edges of the clock? .. I think that is old technology. Can you find out what they think they have?" (RX 920 at 1).

889. Weinstock responded to Walther's question: "Yes, Rambus feels DDR for any memory is under their patent coverage. James [Akiyama, an Intel employee] said that Rambus has more IP than Intel has seen. He further stated the determining factor would be whether the courts take a 'broad or a narrow view of the patents.'" (RX 920 at 1).

890. The April 17, 1997 response by Weinstock was copied to Mailloux, Lee and all of the other recipients of Weinstock's original email. (RX 920 at 1).

891. Lee testified that he understood Weinstock's statement about Rambus's intellectual property claims over "DDR for any

memory" to be a reference to the DDR SDRAM device that was then being discussed at JEDEC. (Lee, Tr. 6968).

892. Lee also understood that Weinstock was referring to possible patent infringement lawsuits by Rambus when Weinstock wrote: "Rambus plans legal action to request royalties on all DDR memory efforts." (Lee, Tr. 6971-72; *see* RX 920 at 2).

893. Lee testified that he did nothing at all to follow up on the reference to Rambus's intellectual property claims regarding "DDR for any memory." (Lee, Tr. 6702, 6972; *see* RX 920 at 1).

894. Lee testified that as far as he knows, none of the other recipients of Weinstock's April 17, 1997 email did anything to follow up on the reference to Rambus's intellectual property claims. (Lee, Tr. 6972-73).

895. Lee explained that he had not followed up with respect to the information regarding Rambus's possible intellectual property claims, and did not consider asking JEDEC to request "RAND" assurances from Rambus, because he "didn't believe this was true." (Lee, Tr. 6981).

896. After reviewing the April 16 and 17, 1997 Micron emails during trial, 42.3 chairman Gordon Kelley testified that he believed that the Micron JEDEC representatives who received the emails were obligated under the JEDEC patent policy to tell the JC 42.3 committee the information about Rambus's claims that is contained in the emails. (G. Kelley, Tr. 2748-49).

897. In May 1997, Rambus engineer Richard Crisp met with the Vice President of Engineering for VIA Technologies, a chipset manufacturer based in Taiwan. (RX 924 at 1).

898. Crisp's email regarding the May 1997 meeting states in part that the VIA executive had:

> ". . . Told me that he thinks that SyncLink is going to be stepping all over Rambus patents. I told him that no one can know for sure about any of that until chips exist, but that since we were first and have a lot of fundamental patents, it would not be a surprise to find that to be the case, and if it were, that I felt quite sure we would pursue protection of our IP rights."

(RX 924 at 1).

899. In July 1997, the official SyncLink Consortium minutes reflect a concern that the Consortium should "collect information relevant to prior art and Rambus filings" in anticipation that "Rambus will sue individual companies" for patent infringement. (RX 966 at 3).

900. In July 1998, a Hynix executive sent an email containing "a list of Rambus patents" to a large group of DRAM engineers and JEDEC representatives from such companies as Micron, Texas Instruments, IBM, VLSI, Compaq, Mosaid and Siemens. (RX 1214 at 1).

901. The list of patents provided by the Hynix executive included the '327 patent that Rambus had left off the list of patents submitted with its JEDEC withdrawal letter. (RX 1214 at 1).

VIII. RAMBUS WAS NOT IN VIOLATION OF ANY JEDEC RULES

A. Rambus Was Not in Violation of the JEDEC Patent Policy

902. Rambus was not in violation of the JEDEC patent policy because that policy merely encouraged the voluntary disclosure of patents essential to practice JEDEC standards. (*See* F. 766-85,

supra). Not disclosing patents conformed not only to the policy but also was consistent with the conduct of other JEDEC members. (*See* F. 686-717, *supra*).

B. There Is No Evidence that Crisp, During the Time Rambus Participated in JEDEC, Had Actual Knowledge that Rambus Had Claims that Could Be Asserted Against JEDEC-Compliant SDRAM or DDR SDRAM Products

903. Complaint Counsel have asserted that "when a JEDEC member company understands or believes that its patents bear upon specific aspects of JEDEC's standardization work, that knowledge on the part of the company triggers a duty to disclose." (Opening Statement, Tr. 17).

904. There is substantial evidence that it was a JEDEC representative's "actual knowledge," not his beliefs, that triggered whether disclosure obligations might exist. (Rhoden, Tr. 624; J. Kelly, Tr. 1970, 2171-72; *see also* RX 669 at 3).

905. Rambus CEO, Geoff Tate, testified that a statement in the June 1992 draft plan that "we believe that Sync DRAMs infringe on some claims in our filed patents" was based on a "feeling" that "synchronous DRAMs sure looked like they stem[med] from [our] inventions." (CX 543A at 17; CX 2073 at 221-22 (Tate, Micron Dep.)). Tate had "assumed" that broad patent applications had been filed to protect all of Rambus's inventions. (CX 2073 at 222 (Tate, Micron Dep.); CX 2088 at 57 (Tate, Infineon Trial Tr.)).

906. Crisp is not among the individuals listed as receiving the June 1992 draft plan. (CX 543A at 11).

907. After the 1992 Business Plan was prepared, a Rambus employee was assigned the task of determining what filed claims would be infringed by SDRAMs. (CX 2073, Tate Micron Dep. at

222-23). The employee subsequently informed Tate that the filed claims were not as broad as previously thought and did not cover the full range of what had been invented and described in the '898 application. (CX 2073 at 222-24 (Tate, Micron Dep.); CX 2088 at 57-58 (Tate, Infineon Trial Tr.)).

908. Complaint Counsel also point to a June 1993 email by Rambus engineer Fred Ware that states that a claim in a Rambus patent application was "directed against SDRAMs." (CX 1959 at 1). Complaint Counsel did not contend at trial, however, that in June 1993 Rambus had any claim in a pending application that covered any feature of SDRAMs. The only Rambus patent claims that are alleged by Complaint Counsel to cover SDRAMs are claims in the '961 and '490 applications; these claims were not filed until 1995. (*See supra* F. 960-62).

909. In their opening statement, Complaint Counsel asserted that Ware's June 1993 email referred to a May 1993 "amendment to Rambus's pending '651 application [application serial no. 07/847,651] related to the concept of programmable CAS latency and that this amendment was intended to cover programmable CAS latency when used in DRAMs generally, including SDRAMs that were the subject of JEDEC work." (Opening Statement, Tr. 84-85). However, all the claims in the May 1993 amendment to the '651 application contained the limitation that data, address, and control information be "in the form of packets," a feature that is not found in SDRAMs. (CX 1458 at 5-8). SDRAMs, unlike RDRAMs, do not receive information in the form of packets. (Rhoden, Tr. 402; Sussman, Tr. 1431-32; G. Kelley, Tr. 2573-74; Kellogg, Tr. 5298; Jacob, Tr. 5466-67). Complaint Counsel did not contend at trial that the claims contained in the May 1993 amendment to the '651 application covered programmable latency as used in JEDEC-compliant SDRAMs.

910. Rambus's JEDEC representative, Richard Crisp, testified that during the time that Rambus was a JEDEC member, he: (1) had not seen any Rambus patent applications with claims over an

SDRAM that used any of the four features at issue here; and (2) did not know one way or the other whether Rambus's pending patent applications covered JEDEC-compliant SDRAMs using any of those features. (Crisp, Tr. 3461-66, 3540-43).

911. In March 1998, Joel Karp informed Rambus's board of directors of the potential weakness of Rambus's existing patent claims. (Farmwald, Tr. 8231-34; CX 615 at 2). Karp also informed the board that he believed that he could improve the strength of the patent portfolio, but that it would take a year or two to do so. (Farmwald, Tr. 8231-32).

912. By July 1999, "Mr. Karp reviewed the Company's strategic portfolio of current IP and plans for an additional strategic portfolio for extending the life of Rambus IP." (CX 622 at 2). He observed a number of weaknesses that could be addressed including a lot of new patent applications or amendments that could be filed, and was actively working on these projects. (Farmwald, Tr. 8237-38; CX 622 at 2).

913. It was not until mid-1999 that a Rambus patent issued with claims that were infringed by JEDEC-compliant SDRAMs or DDR SDRAMs. (Farmwald, Tr. 8239-40; CX 623 at 4).

C. Rambus Did Not Misappropriate Information From JEDEC

914. Rambus began attending JEDEC meetings, in part, to learn what its competition was working on. (CX 837 at 1-2).

915. JEDEC 42.3 Chairman Gordon Kelley testified that he and Siemens's JEDEC representative Willi Meyer were each reporting on JEDEC activities to a joint DRAM development team that IBM and Siemens had created. (G. Kelley, Tr. 2620-21).

916. Kelley testified that he "did not understand that the use of JEDEC confidential information was an abuse as long as the

people using the information were members." (G. Kelley, Tr. 2626).

917. Even today, JEDEC tries to enlist new members by pointing to the competitive advantages of membership, or perhaps the *dis*advantages of *non*-membership. (CX 302 at 17 (Rhoden presentation states that "[i]f you are not there, your competition may be deciding your future.")).

918. Rambus used the information it obtained at JEDEC to help refine the claims in its pending patent applications to ensure that its claims would cover the JEDEC standards. (CX 2092 at 192 (Crisp, Infineon Trial Tr.).

D. There Were No Prohibitions Which Precluded Rambus From Seeking Patent Protection For Inventions that Related to JEDEC Standards

919. The EIA Legal Guides, which governed JEDEC standardization activities while Rambus was a JEDEC member, state explicitly that "[s]tandards are proposed or adopted by EIA without regard to whether their proposal or adoption may in any way involve patents on articles, materials, or processes." (CX 204 at 4).

920. The EIA's January 22, 1996 comment letter to the FTC in connection with the *Dell* litigation states in part that "[a]llowing patented technology in standards is procompetitive." (RX 669 at 2). The letter explains that "[b]y allowing standards based on patents, American consumers are assured of standards that reflect the latest innovation and high technology the great technical minds can deliver." (RX 669 at 2-3).

921. The EIA's January 22, 1996 comment letter to the FTC also states that "[s]tandards in these high-tech industries must be based on the leading edge technologies. Consumers will not buy second-best products that are based only on publicly available

information. They demand and deserve the best technology these industries can offer." (RX 669 at 4).

922. The EIA's January 22, 1996 comment letter to the FTC also states that "[e]ven if knowledge of a patent comes later in time due to the pending status of the patent while the standard was being created, the important issue is the licensing availability to all parties on reasonable, non-discriminatory terms." (RX 669 at 4).

923. EIA General Counsel John Kelly testified that even though EIA would prefer not to include patented technologies in EIA standards, there is no objection to having standards that incorporate patented technologies, as long as the patents are available to all potential licensees on reasonable and nondiscriminatory terms. (J. Kelly, Tr. 2072).

924. Throughout the time period that Rambus was a member, JC 42.3 routinely passed ballots to adopt technology as part of its standards despite its awareness of patent-related issues. At the March 1993 JC 42.3 meeting, for example, the committee voted to pass a ballot on Mode Register Timing for the SDRAM draft specification even though Hitachi raised a "patent alert." (JX 15 at 5).

925. At the March 1993 JC 42.3 meeting, the committee also considered ballots for Self-Refresh Entry/Exit, DQM Latency Reads/Writes, and Auto-Refresh for the SDRAM draft specification. (JX 15 at 8-9). The minutes state that both Hitachi and Mosaid raised a "patent alert" or a "patent concern" with respect to each of these features. (JX 15 at 8, 9). The committee voted unanimously to pass these ballots. (JX 15 at 8, 9).

926. At the March 1993 JC 42.3 meeting, the committee also considered a ballot for a Write Latency = 0 for the SDRAM draft specification. With regard to this ballot, the minutes state that Mosaid raised a patent issue. (JX 15 at 5-6). The minutes also

state, "The Committee is aware of the Hitachi patent. It was noted that Motorola has already noted they have a patent. IBM noted that their view has been to ignore patent disclosure rule because their attorneys have advised them that if they do then a listing maybe construed as complete." (JX 15 at 6). The committee voted unanimously to pass this ballot. (JX 15 at 6). At that meeting, the committee also voted unanimously to send all SDRAM ballots to the JEDEC Council for standardization. (JX 15 at 14).

927. At the very next JC 42.3 meeting, which was held *before* the SDRAM ballots had been voted on by the JEDEC Council, the 42.3 Committee reviewed an analysis of patents relating to SDRAMs. The analysis, which was prepared by Chipworks, included a discussion of several Hitachi patents related to SDRAMs that were described as "powerful" (CX 53A at 13), as well as SDRAM-related patents held by Motorola and other JEDEC members. (CX 53A at 14).

928. No witness who was present at the March and May 1993 JC-42.3 meetings testified that any criticism was leveled against JEDEC members who had obtained patents relating to SDRAMs.

E. Rambus Followed the Advice of Its Legal Counsel in Determining Its Legal Obligations to JEDEC

929. Complaint Counsel asserts that Rambus "acted with knowledge that it was violating" JEDEC's rules relating to intellectual property disclosures. (Complaint Counsel's Pre-Trial Brief, at 196).

930. Shortly after it joined JEDEC, Rambus sought the legal advice of its outside patent counsel, Lester Vincent, in connection with its participation in JEDEC including the preparation and revision of its patent applications. (CX 3125 at 279-80 (Vincent, Dep.)).

931. In March 1992, Richard Crisp and his supervisor, Allen Roberts, talked to Vincent about JEDEC-related issues. (CX 3125 at 310-315 (Vincent, Dep.)). After discussing JEDEC with Vincent, "the two key things that [Crisp] walked away from the meeting understanding was that Rambus should not go and promote a standard, and we should not mislead JEDEC into thinking that we wouldn't enforce our property rights." (Crisp, Tr. 3470-71).

932. Vincent's time sheets show that at around the time he gave Crisp this advice, he reviewed one or more "JEDEC publications." (CX 1937 at 12).

933. Crisp followed Vincent's advice and did not promote a technology for standardization at any time during Rambus's membership. (Crisp, Tr. 3470).

934. An email that Crisp wrote in December 1995, almost four years later, shows that he was still mindful of Vincent's advice at that time. He wrote that he understood that Rambus should not "intentionally propose something as a standard and quietly have a patent in our back pocket. . . ." (CX 711 at 188). As he also stated at the time, he was "unaware of us doing any of this or of any plans to do this." (CX 711 at 188). Crisp testified that this December 1995 passage referred to "what we would have to do and what we should not do in the event that we were to propose the R-module as a standard." (Crisp, Tr. 3485).

935. When Crisp was asked at JEDEC meetings on two occasions to comment about Rambus's intellectual property, he declined to comment each time, and the JEDEC members who testified at trial understood that he had declined to comment. (F. 807-25, 842-57, *supra*). Crisp also testified that no one had informed him that his refusal to comment violated any JEDEC rule or policy. (Crisp, Tr. 3490-91).

936. Crisp was also advised by Vincent, in the 1992 time frame, about the importance of keeping patent applications confidential. Crisp testified that Vincent "told us to not disclose our patent applications. They were confidential." Crisp followed this advice. (Crisp, Tr. 3496).

937. In letters transmitting copies of Rambus's patent applications, Vincent reminded Rambus employees to "keep in mind that this information is confidential." (CX 1951 at 2; CX 1945 at 2).

938. Crisp was present at a JEDEC meeting when an IBM representative stated that he would not disclose intellectual property at JEDEC meetings. Crisp indicated that he understood from that statement that such disclosures were not required. (Crisp, Tr. 3505-07).

F. During the Time of Its Participation in JEDEC Rambus Had No Intellectual Property Interests That It Would Have Been Required To Disclose Even If Disclosure Was Mandatory

1. Rambus Had No Patents That It Was Required To Disclose

939. The parties stipulated that as of January 1996, Rambus held no issued U.S. patents that were essential to the manufacture or use of any device manufactured in compliance with any JEDEC standard. (First Set of Stipulations, Stip. 10).

940. The only patent that Complaint Counsel allege Rambus should have disclosed to JEDEC is U.S. Patent No. 5,513,327 (the '327 patent). Complaint Counsel allege that disclosure of the '327 patent was required because claims 1 and 7 of the patent could have been reasonably construed by an engineer to cover a JEDEC-compliant SDRAM that also incorporated certain dual-edged clocking proposals and because those claims would read on

the JEDEC DDR SDRAM standard. (Jacob, Tr. 5541-49, 5551-60).

941. The proposals or presentations that Complaint Counsel raise in this regard are: (1) a presentation by William Hardell of IBM referenced in the May 1992 minutes of the JEDEC 42.3 subcommittee (the "Hardell presentation") (CX 34 at 32; Jacob, Tr. 5542), (2) a "Future SDRAM Features Survey Ballot" referenced in the December 1995 minutes of the JEDEC 42.3 subcommittee (the "Survey Ballot") (JX 28 at 34-35; Jacob, Tr. 5543-44), and (3) a presentation by Samsung entitled "Future SDRAM," referenced in the March 1996 minutes of the JEDEC 42.3 subcommittee (the "Samsung presentation") (JX 31 at 71; Jacob, Tr. 5544).

942. The '327 patent issued on April 30, 1996 and was publicly available as of that date. (CX 1494 at 1). All of the proposals or presentations referenced by Complaint Counsel as supposedly triggering a disclosure obligation with respect to the '327 patent were made *before* the '327 patent issued.

943. Complaint Counsel's patent law expert, Mark Nusbaum, did not testify as to whether claims of the '327 patent related to JEDEC work.

944. Professor Jacob, who testified on behalf of Complaint Counsel regarding the alleged relationship between the '327 patent and JEDEC work, has no patents to his name and has never previously done any claims analysis of the type he presented in this matter with respect to the '327 patent. (Jacob, Tr. 5624, 5650).

a. The '327 Patent Contains Various Limitations

945. Professor Jacob concedes that Claim 1 of the '327 patent "describes a specific implementation" of dual edge clocking, including the "implementation detail" that the DRAM contains

two input receivers with one receiver latching information in response to the rising edge of a clock signal and the other receiver latching information in response to the falling edge of the clock signal. (CX 1494 at 23; Jacob, Tr. 5546-47).

946. Professor Jacob also concedes that claim 7 of the '327 patent describes a specific implementation of dual edged clocking where the DRAM "toggle[s] between two output drivers through a multiplexer." (CX 1494 at 23; Jacob, Tr. 5548).

b. Rambus Had No Duty To Disclose the '327 Patent Based On the Hardell Presentation

947. The Hardell presentation related to IBM's "toggle mode" DRAM. (G. Kelley, Tr. 2514). IBM's toggle mode was an asynchronous design. (Jacob, Tr. 5608; Soderman, Tr. 9398).

948. The Hardell presentation noted that it has "A-Synchronous RAS/CAS." (CX 34 at 32). This makes it an asynchronous DRAM, according to Professor Jacob's definition of asynchronous DRAMs as "those who are driven off the RAS and CAS signals where the RAS and CAS actually control the operation of the DRAM rather than a clock." (Jacob, Tr. 5394).

949. JEDEC-compliant SDRAMs are synchronous DRAMs with synchronous RAS and CAS signals; the Hardell presentation described an asynchronous DRAM with an asynchronous RAS/CAS interface. (CX 34 at 30-32).

950. The Hardell presentation gave no details about implementation of the dual-edged clocking feature, stating simply: "dual clock edge." (CX 34 at 32).

951. The Hardell presentation was referenced in a memorandum discussing presentations at a meeting of a task group in Dallas in April 1992, and no evidence was presented at

trial that the Hardell presentation was ever balloted at JEDEC. (CX 34 at 4, 30, 32).

c. Rambus Had No Duty To Disclose the '327 Patent Based On the Survey Ballot

952. The Survey Ballot was circulated on or about October 30, 1995 to JEDEC members to determine what features JEDEC members might want to include in future DRAMs. (JX 28 at 34-48; CX 260; Lee, Tr. 6636).

953. With respect to dual-edge clocking, the result of the Survey Ballot was that there was "mixed support" for "using both edges of the clock for sampling inputs." (JX 28 at 35).

954. Complaint Counsel did not present evidence sufficient to find that the Survey Ballot was ever balloted and therefore it would not have triggered the patent policy.

d. Rambus Had No Duty To Disclose the '327 Patent Based On the Samsung Presentation

955. With respect to dual-edge clocking, the March 1996 Samsung presentation stated only that "Data in sampled at both edge [sic] of Clock into memory." The presentation went on to state: "Use both edge [sic] of the Strobe clock to sample the memory Data into Controller." (JX 31 at 71).

956. Complaint Counsel did not present evidence sufficient to find that the Samsung presentation was ever balloted and therefore it would not have triggered the patent policy.

e. Complaint Counsel Did Not Provide Sufficient Evidence to Determine Whether the Presentations Would Trigger the Patent Policy

957. Complaint Counsel has not shown that there were sufficient implementation details presented in the Hardell presentation, Survey ballot, or Samsung presentation from which to determine whether the presentations could be construed as covering claims in the '327 patent. (*See* CX 34; JX 28, JX 31).

958. Rambus has not asserted the '327 patent against any SDRAM or DDR SDRAM devices. (*See* First Set of Stipulations, Stip. 14).

2. Rambus Had No Undisclosed Patent Applications That It Was Required to Disclose, Even if the Policy Required Disclosure

959. The parties have stipulated that prior to the adoption of the JEDEC SDRAM standard in 1993, Rambus had no undisclosed claims in any pending patent application that, if issued, would have necessarily been infringed by the manufacture or use of any device manufactured in accordance with the 1993 JEDEC SDRAM standard. (First Set of Stipulations, Stip. 9).

960. Despite this stipulation, Complaint Counsel argued that the following claims of Rambus patent applications should have been disclosed to JEDEC:

(1) Claims 151, 159, 160, 164, 165 and 168 of application serial no. 07/847,961 (the '961 application), because they allegedly cover JEDEC-compliant SDRAMs (Nusbaum, Tr. 1544-45; Jacob, Tr. 5507, 5523-28);

(2) Claims 183, 184, and 185 of application serial no. 08/469,490 (the '490 application), because

they allegedly cover JEDEC-compliant SDRAMs (Nusbaum, Tr. 1572-73; Jacob, Tr. 5528-32);

(3) Claims 151, 152, 166 and 167 of application serial no. 07/847,692 (the '692 application), because they allegedly cover a presentation made by NEC that is contained in the September 1994 minutes of the JEDEC 42.3 subcommittee (JX 21 at 91; Nusbaum, Tr. 1584; Jacob, Tr. 5535, 5540); and

(4) Claim 151 and 152 of application serial no. 08/222,646 (the '646 application), because it allegedly covers the Hardell presentation, the Survey Ballot, and the Samsung presentation (Nusbaum, Tr. 1597-98; Jacob, Tr. 5550).

961. The claims of the '961 application that Complaint Counsel allege covered JEDEC-compliant SDRAMs, claims 151, 159, 160, 164, 165, and 168, were added in an amendment filed on January 6, 1995. (CX 1504 at 216-26; Nusbaum, Tr. 1544-45; Fliesler, Tr. 8847). In an office action dated April 16, 1995, the patent examiner rejected all of the claims pending in the '961 application. (CX 1504 at 227-39). Among other grounds, claims 151-165 were rejected as indefinite. (CX 1504 at 229). All of the claims in the '961 application that allegedly covered JEDEC-compliant SDRAMs were cancelled by Rambus on June 23, 1995. (CX 1504 at 258; Fliesler, Tr. 8847-48).

962. The claims of the '490 application that Complaint Counsel allege covered JEDEC-compliant SDRAMs, claims 183, 184 and 185, were added in a preliminary amendment filed on June 23, 1995. (CX 1504 at 258, 264-66; Nusbaum, Tr. 1572-73; Fliesler, Tr. 8852). After a restriction requirement from the patent office, Rambus elected to pursue other claims. Claims 183, 184

and 185 were withdrawn from further consideration as of November 27, 1995. (CX 1504 at 274-75; Fliesler, Tr. 8852-54).

963. Claims 151 and 152 of the ‘692 application were filed in a preliminary amendment mailed on June 28, 1993. (CX 1502 at 205, 208; Fliesler, Tr. 8864-65). In an amendment mailed on October 23, 1995, claims 151 and 152 were amended and claims 166 and 167 were added. (CX 1502 at 233-35; Fliesler, Tr. 8864-65).

964. Complaint Counsel has not shown that, upon a formal infringement analysis, claims 151 and 152 of the ‘692 application (whether before or after the October 23, 1995 amendment) and claims 166 and 167 might cover devices built according to the September 1994 NEC presentation. (JX 21 at 91; Fliesler, Tr. at 8866-67).

965. Claim 151 of the ‘646 application was mailed on September 6, 1994. (CX 1493 at 183-85; Fliesler, Tr. 8856). In an office action dated January 24, 1995, the patent examiner rejected claim 151 for, among other reasons, being indefinite. (CX 1493 at 212, 215). Claim 151 was canceled in an amendment filed on September 14, 1995. (CX 1493 at 243; Fliesler, Tr. 8856-57). The ‘327 patent, which issued from the ‘646 application, did not contain claim 151. (CX 1494; Nusbaum, Tr. 1617).

966. Claim 151 was filed over two years after the Hardell presentation, and before the Samsung presentation or the issuance of the Survey Ballot. (CX 1493 at 183-85; Fleisler, Tr. 8856; CX 34 at 32; JX 28 at 34-35; JX 31 at 71). Thus, claim 151 was not pending at the time of any of the presentations that allegedly triggered its disclosure.

967. Claim 152 of the ‘646 application issued as claim 1 of the ‘327 patent. (CX 1493 at 223-24; CX 1494 at 23).

G. Rambus Withdrew From JEDEC Before Formal Work On the Standardization of the DDR SDRAM Began

968. Rambus attended its last JEDEC meeting in December of 1995. On June 17, 1996, Rambus notified JEDEC that it would not pay its dues for 1996 and that it would no longer be a JEDEC member. (CX 2104 at 853-54 (Crisp, Micron Dep.); CX 887 at 1).

969. The DDR SDRAM standard received JC 42.3 committee approval in March 1998, but was not published until 2000. (CX 375 at 1-3; JX 57).

970. The DDR SDRAM standard received JEDEC Board of Director approval in 1999. (Rhoden, Tr. 743).

971. The first time that a balloted item was approved as part of the JEDEC DDR SDRAM standard was June 1997. (CX 375 at 2).

972. An email authored by JEDEC Board Chairman Desi Rhoden in March 1998 shows that the first presentation leading to the DDR SDRAM standard occurred in December 1996, after Rambus had withdrawn from JEDEC. (CX 375 at 1-2).

973. On March 9, 1998, Rhoden sent an email to Ken McGhee, the JEDEC Secretary, for forwarding to all JC 42 members. (Rhoden, Tr. 1192-93; CX 375). The email was an effort by Rhoden to recap what had transpired in the DDR SDRAM standardization process. (Rhoden, Tr. 1195).

974. Rhoden's March 9, 1998 email states in part:

> [W]e could have finished the DDR standard sooner if only we had started earlier. Let us recap what has transpired with DDR:

> 1. A lot of private and independent work outside of JEDEC for most of 1996 (here is where we missed a good opportunity to start early).
>
> 2. December 96 – A single overview presentation of a DDR proposal at a JC 42 meeting.
>
> 3. March 97 – Many (5 as I remember) presentations of very different proposals at JEDEC (no where near the consensus that was supposedly built outside of the committee). None of these were compatible with each other. At this meeting the decision was made to finally get serious and set up a special meeting for April 97.
>
> 4. April 97 – Real, focused, dedicated work begins at a special meeting. Many very good ideas and a lot of truly animated discussion.
>
> 5. June 97 – First ballots on DDR pass committee.
>
> 6. July 1997 – A second special meeting where the last of the basic concepts were articulated and sent out for ballot.
>
> 7. Sept 97 – The diamond in the rough took its basic shape (there were 2 very similar, but still different forms).

(CX 375 at 1-2).

975. Rhoden's March 1998 email thus dates the first presentation to JEDEC of a DDR SDRAM proposal to December 1996. (CX 375 at 1).

976. Rhoden's email states that the DDR device was being developed "outside of JEDEC" in 1996. (CX 375 at 1).

977. In an April 1997 presentation, Rhoden stated: "DDR & SLDRAM were Introduced in JEDEC in Dec 96." (RX 911 at 3).

978. The initial DDR SDRAM presentation that Rhoden referred to in his March 1998 email and his April 1997 presentation was made by Fujitsu in December 1996. (Rhoden, Tr. 1198; RX 911 at 3; CX 375 at 1). This presentation, identified in the minutes of the JC 42.3 subcommittee as "Fujitsu Double Data Rate SDRAM," was designated as a "first showing." (JX 35 at 6, 34-42).

979. Desi Rhoden was in a position to know about the dates described in his March 1998 email. He has played a leadership role at JEDEC for quite some time. (Rhoden, Tr. 1191). He is currently chairman of the JC 42 committee, which contains the JC 42.3 subcommittee. (Rhoden, Tr. 1191). He has also been chairman of the 42.3 subcommittee and is currently chairman of the JEDEC Board of Directors. (Rhoden, Tr. 1190). In 1998, Rhoden was very actively involved in the DDR SDRAM standardization process within the JEDEC 42 committee. (Rhoden, Tr. 1191-92).

980. There is other contemporaneous evidence that work on the DDR SDRAM device did not begin, even outside of JEDEC, until the summer of 1996. An IBM presentation on DDR SDRAM dated March 17, 1997 notes that "Industry has been working on DDR definition for 6-9 months," that is, beginning at some point between approximately mid-June and mid-September 1996. (RX 892 at 1). Initially, this work consisted of "small supplier consortiums and individual supplier/user meetings." (RX 892 at 1). Like Rhoden's testimony, the IBM document dates the first "Official DDR presentations" at JEDEC to December 1996, referring (again) to the first showing by Fujitsu. (RX 892 at 1).

981. A March 10, 1997 Mitsubishi memorandum regarding "DDR SDRAM Specification Planning History and Recent Trends" confirms that DDR efforts began outside of JEDEC in the summer of 1996, with "eight companies . . . meeting once every 2 weeks to quickly plan DDR specifications." (RX 885A at 1). The Mitsubishi memorandum's first mention of JEDEC work relating to DDR SDRAM is the first showing by Fujitsu in December 1996. (RX 885A at 1).

982. As Gordon Kelley, Chairman of the JC 42.3 subcommittee, explained, after a company left JEDEC, it had no duty to disclose anything to JEDEC. (G. Kelley, Tr. 2700).

H. Document Destruction by Rambus

983. In March 1998, there was "growing worry" within Rambus about "email back-ups as being discoverable information" in future litigation. (CX 1005 at 1).

984. Rambus executives decided to destroy emails archived on the company's backup system after three months. (CX 1744A at 94 ("3 months might be ok"); CX 1744A at 104 (May 1998 management staff meeting: "Backups kept for three months"); CX 2114 at 137 (Karp, Dep.)).

985. Rambus did not preserve emails from the early 1990's that were stored on Macintosh backup tapes. (CX 2114 at 141 (Karp, Dep.) ("those were the first tapes that were destroyed")).

986. Employees could still maintain their own email archives for whatever time period they desired. Employees were told to maintain their own archives if they wanted to maintain email files for longer than three months. (CX 2102 at 80-81 (Karp Dep.); CX 1031).

987. Rambus CEO Geoffrey Tate and Karp had a one-on-one meeting at which they discussed reviewing pre-June 1996 backup

tapes. (CX 1744A at 136 ("Review backup tapes for pre-June 1996, Check for files"); CX 2114 at 145-6 (Karp, Dep.)).

988. On May 14, 1998, Karp sent an email to all Rambus engineers and senior managers regarding "Backup Strategy/Document Retention Policy." (CX 1031 at 1). He informed them that "[e]very Rambus employee will be involved" in Rambus's document retention policy. (CX 1031 at 1). Karp announced that he expected to have "a company meeting in early June to kick off the program." (CX 1031 at 1). He invited questions in face-to-face discussions, but preferred that senders of any emails "keep the distribution narrow." (CX 1031 at 1).

989. In June 1998, Karp outlined a plan to implement Rambus's document retention policy. (CX 1744A at 126 ("Exec approval of doc. ret. policy, Presentation of details to exec, Presentation to managers and key individuals with outside counsel, Presentation to staff via division meetings, Implementation mid-August"); CX 2114 at 1442-43 (Karp, Dep.)).

990. In July 1998, Karp disseminated Rambus's two-page written document retention policy to all Rambus employees. (CX 1040 at 1-2; Diepenbrock, Tr. 6230; CX 2114 at 156-57 (Karp, Dep.)).

991. After distributing the written policy, Karp and an attorney from Cooley Godward held a meeting with all Rambus employees to "kick off" the document retention policy. (Diepenbrock, Tr. 6230; Crisp, Tr. 3419; CX 2102 at 98-99 (Karp, Dep.); CX 2114 at 157 (Karp, Dep.)).

992. While explaining the document retention policy to Rambus employees, Karp told staff to destroy emails because they could be discoverable in litigation. (CX 1264 at 1 ("EMAIL – THROW IT AWAY . Email Is Discoverable In Litigation Or Pursuant To A Subpoena . Elimination of email is an integral part

of document control . In General, Email Messages Should Be Deleted As Soon As They Are Read"); CX 2114 at 161 (Karp, Dep.) ("We know all e-mail is discoverable; there's no question about that. So the real question becomes what are you required to save and what should you not save.")).

993. The document retention instructions were also summarized in slides that Karp used when he delivered presentations to staff. The slides Karp presented to all Rambus employees instructed Rambus employees to, "LOOK FOR THINGS TO KEEP." (CX 1264 at 1).

994. Rambus's former in-house counsel Anthony Diepenbrock was told that Rambus did not want to keep documents around because they were "[d]iscoverable in a lawsuit." (Diepenbrock, Tr. 6234-35 ("Q. And when you say you were told Rambus didn't want to keep these documents around because they were discoverable, when you say 'discoverable,' you are talking about in a subsequent litigation like we are in right here, right? . . . A. Discoverable in a lawsuit, right")).

995. As a result of directives from Karp, Diepenbrock, Rambus's in-house counsel, purged his documents and files in the summer on 1998. (Diepenbrock, Tr. 6235-36).

996. In the weeks following the initial meeting, Karp held several training sessions regarding the document retention plan. (CX 2102 at 98 (Karp, Dep.)).

997. Karp explained Rambus's document retention policy to all Rambus employees. (CX 2102 at 104 (Karp, Dep.)).

998. In September 1998, Rambus celebrated a corporate-wide "Shredder Day." (CX 1044 at 1; CX 1051 at 1 ("Thursday is Shred Day 1998. . . . Please leave your burlap bags in the hallway . . . We will have a Shred Day Celebration in the new 1st floor open area . . . If you have any questions regarding our Document

Retention Policy, please see Joel [Karp]"); Crisp, Tr. 3422; CX 2102 at 106 (Karp, Dep.) ("we had one day where we had kind of a spring cleaning . . . one of the many Valley shredding companies [came] in with their kind of industrial shredders")).

999. In one day alone, in the span of five hours, Rambus destroyed as much as 20,000 pounds of business records. (CX 2102 at 108 (Karp, Dep.) (Rambus delivered "a lot of stuff" to the shredding company; the "stuff [was] being basically piled pretty high on carts."); CX 1052 at 1).

1000. Karp testified that he "did a little bit of spot checking" with Rambus employees and "sat and watched over their shoulder" to insure compliance with the document retention policy. (CX 2102 at 97-98 (Karp, Micron Dep.)).

1001. In September 1998, Karp had a one-on-one meeting with Rambus CEO Geoffrey Tate during which Karp inquired whether Tate and other board members had cleaned out their files. (CX 1744A at 141 ("Doc. Retent, Geoff files?, Board members?"); CX 2114 at 148 (Karp, Dep.)).

1002. Rambus instructed Lester Vincent, an attorney with its outside patent law firm Blakely, Sokoloff, Taylor & Zafman, to destroy Rambus-related files. (CX 3129 at 530 (Vincent, Dep.) ("[Karp] discussed the Rambus document retention policy that he wanted me to implement."); CX 3126 at 410 (Vincent, Dep.); CX 2114 at 183-84 (Karp, Dep.)).

1003. At Rambus's request, Vincent destroyed a variety of documents from the left hand side of his files, including various "prosecution documents" such as "patent prosecution files for issued patents . . . claiming priority to the 1990 Farmwald, Horowitz application." (CX 3126 at 408 (Vincent, Dep.); CX 3129 at 530-33, 536, 539-40 (Vincent, Dep.)).

1004. Vincent also destroyed various "drafts, handwritten notes, letters or faxes, and maybe drawings," including correspondence from Rambus to Blakely, Sokoloff and vice versa, Vincent's own handwritten notes and those of other lawyers from his firm, drafts of patent applications and amendments, draft handwritten drawings or informal drawings, electronic versions of such documents, and audio tapes of meetings with inventors. (CX 3129 at 531-33 (Vincent, Dep.); CX 3126 at 425-26 (Vincent, Dep.)).

1005. Some of the copies Vincent destroyed were the "only documents in existence." (CX 3129 at 539-40 (Vincent, Dep.)).

1006. Vincent carried out the document destruction at various points in time, beginning several months after the initial instructions he received from Rambus in 1997 and early 1998. (CX 3126 at 418, 422 (Vincent, Dep.)).

1007. Vincent briefly suspended the document destruction after Rambus filed a lawsuit against Hitachi in 2000. (CX 3129 at 534-35 (Vincent, Dep.)).

1008. After the hiatus in document destruction during the pendency of the Hitachi litigation, Vincent's law firm recommenced destroying documents. (CX 3129 at 535 (Vincent, Dep.)). Document destruction continued at least until Rambus filed the Infineon suit in August 2000. (CX 3126 at 424 (Vincent, Dep.)); CX 1329 at 542 (Vincent, Dep.)).

1009. CX 711 is a 199 page collection of emails authored by Richard Crisp that were preserved on Rambus's main server when Crisp transferred the messages from one laptop computer to another via the server. (Crisp. Tr. 3587-91). These documents were preserved, were produced in discovery, and were admitted into evidence. (Crisp, Tr. 3572-76, 3588-92).

IX. RAMBUS HAS MONOPOLY POWER IN THE RELEVANT MARKETS

A. Relevant Markets

1. Product Markets

1010. Technology markets are markets for ideas or inventions where technology itself is a product. (McAfee, Tr. 7324). The demand for DRAM technology is derived from the demand for DRAMs, and the demand for DRAMs is derived from the final products in which DRAM is used. Ultimately the demand for the technology traces back to the demand for the final good. (McAfee, Tr. 7182, 7198-99).

1011. Often in technology markets frequent trades have historically not taken place. Therefore there is little historical price and quantity data. (McAfee, Tr. 7321). In lieu of data pertaining to actual trades, serious consideration of a technology by JEDEC participants suggests that informed buyers of the technology view those technologies as significant substitutes and hence price-constraining substitutes. (McAfee, Tr. 7333-34).

1012. The relevant purchasers or buyers in this case include DRAM manufacturers. (McAfee, Tr. 7323-24; Rapp, Tr. 9969-72).

1013. There are four relevant technology markets in this case: (1) the latency technology market (McAfee, Tr. 7364); (2) the burst length technology market (McAfee, Tr. 7373); (3) the data acceleration technology market (McAfee, Tr. 7380); and (4) the clock synchronization technology market (McAfee, Tr. 7385-86).

1014. In addition, it can be analytically useful to consider a "cluster" market. (McAfee, Tr. 7390-92). A "cluster" market would consider each of the four relevant product markets as a collection, based on the logic that the products are used in the

same products, though strictly speaking they are not substitutes for one another. (McAfee, Tr. 7390-92). The "cluster" market utilized in this case is the synchronous DRAM technology market. (McAfee, Tr. 7390-91).

1015. Respondent does not challenge Complaint Counsel's product market definitions. Respondent's economic expert, Dr. Rapp, testified that "relevant market is not crucial to understanding competition and market power in this setting." (Rapp, Tr. 10036).

2. Geographic Market

1016. The relevant geographic market for each relevant product market is the world. (McAfee, Tr. 7393).

1017. The relevant geographic market for each relevant product market is the world because: buyers of technology typically do not care about the geographic source of technology; technologies tend to be licensed worldwide; technologies tend to flow across national borders; downstream products are produced and used worldwide; and transportation costs of both technology and DRAMs are negligible. (McAfee, Tr. 7393-95).

B. Monopoly Power

1018. Rambus possesses monopoly power in the relevant technology markets. (F. 1019-29; McAfee, Tr. 7420-21).

1019. Rambus's economic expert, Dr. Rapp, does not contest that Rambus possesses market power in the four technology markets. (Rapp, Tr. 10046). Dr. Rapp testified that his "opinion is that the market power that Rambus possesses in these four technologies arises solely out of the distance between the cost-performance qualities of the Rambus technologies and the next best alternative." (Rapp, Tr. 10260).

1. Market Share

1020. The percentage of total DRAM production in the world today that is subject to Rambus's patent claims is in the upper nineties. (McAfee, Tr. 7430).

1021. Rambus claims that approximately ninety percent of the entire DRAM market is covered by Rambus patents. (CX 1386 at 4 ("Today - We are on the cusp of achieving our original [goal] - SDRAM+DDR+RDRAM>>90% of the DRAM market - SDRAM/DDR: [approximately] 20% paying us royalties now; all by 01/E")); CX2067 at 171 (Davidow, Dep.) ("Q. So am I right, then, that it's Rambus's position [] that any SDRAM or RDRAM being used in main memory PCs today [January 31, 2001] are covered by their patents? . . . [A] I would say that it is highly likely that is true.")).

2. Assertion of Patents

1022. Rambus believed that certain of its patents cover SDRAM and DDR SDRAM products. (CX 1353 at 7 ("Intellectual Property . . . Strategic Patent Portfolio 1: SDRAM/DDR/Controllers all infringe"); CX 1382 at 33 ("Non-Compatible License Terms, All agreements cover SDRAM, DDR and logic ICs which control these memories"); CX 1364 at 1-2 (*in camera*)).

1023. Rambus has asserted that its innovations include "Programmable latency register on a SDRAM," "Programmable burst techniques implemented on a SDRAM," "DLL implemented on a SDRAM," and "Double data rate." (CX 1371 at 5; CX 1383 at 4; *see also* CX 1363 at 1).

1024. Rambus has asserted that "programmable latency on a DRAM" and "Programmable burst on a DRAM," as used in SDRAMs, and "DLL implemented on a DRAM" and "Double

data rate," as used in DDR SDRAMs, are Rambus innovations covered by its patents. (CX 1363 at 3).

1025. Rambus has asserted that its issued patents cover programmable CAS latency, as described and depicted in JEDEC SDRAM and DDR SDRAM data sheets and individual company data sheets. (CX 1371 at 46, 53 (asserting that the phrase "value which is representative of a time delay after which the memory device responds to a read request" in claim 44 of Rambus's '365 patent corresponds to the CAS latency portion of the mode register diagram in the JEDEC 64M DDR SDRAM Data Sheet); CX 1383 at 47, 51 (same); CX 1338 at 20, 23 (asserting that same language from claim 23 of Rambus's '195 patent corresponds to the CAS latency portion of the mode register in Micron's 16M SDRAM Datasheet); CX 1338 at 41, 44 (similar language from Rambus's '918 patent compared to the CAS latency portion of Micron's 16M SDRAM Datasheet)).

1026. Rambus has asserted that its issued patents cover programmable burst length, as described and depicted in JEDEC SDRAM and DDR SDRAM data sheets and individual company data sheets. (CX 1371 at 64, 68 (asserting that the phrase "a first amount of data to be output onto a bus in response to a read request" in claim 1 of its '214 patent corresponds to the burst length portion of the mode register diagram in the JEDEC 64M DDR SDRAM Data Sheet); CX 1383 at 60, 64 (same); CX 1371 at 31, 36 (asserting that similar language from Rambus's '918 patent corresponds to the burst length portion of the mode register in Micron's 16M SDRAM Datasheet)).

1027. Rambus has asserted that its issued patents cover on-chip DLL as depicted in JEDEC SDRAM and DDR SDRAM data sheets. (CX 1371 at 84-85 (asserting that the term "delay locked loop" in claim 11 of its '214 patent corresponded to the indication "DLL" in the functional block diagram of the JEDEC 64M DDR SDRAM Data Sheet)).

1028. Rambus has asserted that its patents cover use of programmable CAS latency, programmable burst length, on-chip DLL and dual edge clock in JEDEC-compliant SDRAMs and DDR SDRAMs. (Lee, Tr. 6776-77; Rhoden, Tr. 529-31).

1029. Rambus has also asserted that certain of its issued foreign patents cover use of programmable CAS latency, programmable burst length, on-chip DLL and dual edge clock in certain SDRAMs and DDR SDRAMs. (Bechtelsheim, Tr. 5884-85; CX 1268 at 1-8, 13-14).

3. JEDEC Standardization

a. Rambus's Market Power Is Not Attributable to the Inclusion of Its Technology In JEDEC Standards

1030. Regarding standardization and market power, Rambus offered the testimony of Dr. Rapp, who has expertise in the area of standard setting. As an example, he recently presented a paper on the economics of standard setting at a session of the Antitrust Section of the American Bar Association, which Dr. Rapp proposed and helped to organize. (Rapp, Tr. 9770-71).

1031. Last year, Dr. Rapp presented a paper and testified about the issue of standard setting and market power at the joint hearings of the Federal Trade Commission and the Department of Justice on intellectual property and the knowledge based economy. (Rapp, Tr. 9771).

1032. In contrast, Complaint Counsel's expert, Professor McAfee, has no expertise in the area of standard setting. (McAfee, Tr. 11345).

1033. According to the economic literature, a standard is a specification of a product design intended to achieve engineering compatibility, either between parts of a product or system or

between components of a network. (Rapp, Tr. 9783). Economists recognize that standards are necessary when compatibility requirements are high and when either products, systems, or networks will fail unless engineering compatibility is maintained. (Rapp, Tr. 9783). From an economist's point of view, standard setting does not entail specifying every detail of a product; rather, standard setting is economically efficient when it achieves compatibility but does not over-determine product characteristics. (Rapp, Tr. 9785).

1034. Economists refer to standards that are set through formal means, i.e., through a standard setting body or the government, as *de jure* standards. (Rapp, Tr. 9788-89). Standards that emerge through market forces are referred to as *de facto* standards. (Rapp, Tr. 9789).

1035. In a market where compatibility requirements are exceedingly high, the market might permit only a single standard. (Rapp, Tr. 9791). This may occur in a network industry, which require a special kind of complementarity where systems must be able to communicate. (Rapp, Tr. 9792). The typical example of this type of network effect is the facsimile machine. A facsimile machine is worthless if it cannot communicate with other facsimile machines; the more facsimile machines that it is able to communicate with, the more valuable it is. (Rapp, Tr. 9792-93).

1036. Where compatibility requirements are less than extreme, which is more common, multiple standards may coexist. (Rapp, Tr. 9791). For example, there are several standards for cellular telephones, but each type of cellular telephone can communicate with the other types. (Rapp, Tr. 9791).

1037. Compatibility requirements in the DRAM industry are not high. (Rapp, Tr. 9793). Although DRAM must be compatible with other components in a particular computer, a computer with one type of DRAM can communicate with a computer with another type of DRAM. (Rapp, Tr. 9793-94). This means that

network effects in the DRAM industry are weak. (Rapp, Tr. 9794).

1038. Because of the weakness of network effects, different DRAM standards can coexist in the market. (Rapp, Tr. 9794).

1039. Standardization by JEDEC is not necessary for marketplace success. For instance, the latest generation of Video RAM was not standardized by JEDEC yet gained market success. Samsung actually brought the technology to JEDEC for standardization, but JEDEC declined to adopt it. (Prince, Tr. 9021). Samsung produced the product anyway, and it became a high volume DRAM product. (Prince, Tr. 9021-22).

1040. Similarly, reduced latency DRAM ("RLDRAM") was developed and produced by Infineon and Micron with little or no involvement by JEDEC. (Bechtelsheim, Tr. 5965-66).

1041. Standardization by JEDEC is also sometimes insufficient for marketplace success. For example, JEDEC standardized Burst EDO, a technology brought to JEDEC by Micron (JX 23 at 68), yet it failed in the marketplace. (Williams, Tr. 873). Failure occurred despite the fact that Micron rigorously promoted the technology. (Williams, Tr. 822-24).

1042. JEDEC standardization is not always necessary nor sufficient to assure demand for a product. Standardization of SDRAM by JEDEC in 1993 did not assure that there would be demand for SDRAM devices (MacWilliams, Tr. 4809-10), and SDRAM might never have enjoyed demand from the market absent Intel's developemnt of the PC100.

1043. The publication of JEDEC's SDRAM standard was insufficient to ensure market success or even interoperability. The JEDEC SDRAM standard was not sufficiently comprehensive; because of this, SDRAM products made by one DRAM

manufacturer were not compatible with those produced by another. (MacWilliams, Tr. 4908).

1044. Prompted by these incompatibilities, Intel – not JEDEC – developed the "PC SDRAM" standard in 1996. (MacWilliams, Tr. 407-09). As stated in that standard, "The objective of this document is to define a new Synchronous DRAM specification ('PC SDRAM') which will remove extra functionality from the current JEDEC standard SDRAM specification, so that it will be a 'fully compatible' device among all vendor designed parts." (RX 2103-14 at 9).

1045. The Intel PC SDRAM specification set forth what would become the industry specification for PC100 SDRAM. (MacWilliams, Tr. 4908). For instance, Compaq used Intel PC100 SDRAM compliant parts for its products. (Gross, Tr. 2350-51). Similarly, AMD referred to the Intel PC SDRAM specification when designing its chipsets. (Polzin, Tr. 4010-11).

1046. The Intel PC SDRAM specification later set forth the industry standard for PC66 SDRAM. (MacWilliams, Tr. 4908; RX 2104-13 at 60-61). Compaq, for example, used Intel PC66 SDRAM compliant parts for its products. (Gross, Tr. 2348-49).

1047. The PC133 SDRAM standard was developed by yet another route. In that case, DRAM manufacturers and PC OEMs developed the specification. (MacWilliams, Tr. 4912-13; CX 2560 at 1). The PC133 SDRAM standard was later incorporated into the Intel PC SDRAM standard. (RX 2104-14 at 7 (document revision history shows addition of standards for 133MHz SDRAM); MacWilliams, Tr. 4908). Again, Compaq used the Intel PC133 SDRAM compliant DRAM for its products. (Gross, Tr. 2353).

1048. Intel's adding of the PC SDRAM standard specifications demonstrates that there are powerful forces in the DRAM industry that affect DRAM standards in a *de facto* rather

than *de jure* sense. From an economic perspective, Intel can, outside of a standard setting body, create specifications or specification addendums that become the industry standard. (Rapp, Tr. 9797). Formal standard setting is therefore not the only way in which an iteration of DRAM can become prominent. (Rapp, Tr. 9798).

1049. It is sometimes the case, but not always, that formal standard setting may create market power. (Rapp, Tr. 9798-99). Formal standard setting may create market power when (1) there are high compatibility requirements, (2) the standard setting body is faced with several technologies that are more or less equivalent in cost-performance terms, and (3) standard setting elevates one of those technologies above the others. (Rapp, Tr. 9799-00). Where compatibility requirements are not high and there may exist more than one standard, then little or no market power is gained through standard setting. (Rapp, Tr. 9800).

1050. Where one technology is superior to the alternatives then that technology would have been selected and become the *de facto* standard had the market been allowed to operate. Under these circumstances, formal standard setting does not add any market power. (Rapp, Tr. 9800-01). The market power of the technology is due to its superiority. (Rapp, Tr. 9801).

1051. Standardization of the Rambus technologies by JEDEC did not reduce the substitution possibilities of alternatives, and Rambus's market power was unchanged by formal standard setting by JEDEC. (Rapp, Tr. 9902).

b. Rational Manufacturers and a Rational Standard Setting Organization Would Have Still Adopted the Rambus Technologies Had Disclosure Occurred

1052. The evidence shows that the four Rambus technologies were the technologies of choice throughout the relevant time

period and that a rational manufacturer or a rational JEDEC would have selected the Rambus technologies. (Rapp, Tr. 9903). The additional disclosures that Complaint Counsel allege Rambus should have made would not have affected the outcome because there were no cost-performance equivalent technologies to the two Rambus technologies incorporated in SDRAM or to the four Rambus technologies incorporated in DDR. (Rapp, Tr. 9907-08). Had the allegedly required additional disclosures occurred, rational manufacturers and a rational standard setting organization would have adopted the Rambus technologies for both SDRAM and DDR. (Rapp, Tr. 9908-09).

1053. It therefore follows that competition has not been adversely affected by Rambus's alleged failure to disclose. (Rapp, Tr. 9908-09). It is worth noting on this issue that Complaint Counsel's economic expert testified that the alleged conduct of Rambus has had no impact on DRAM prices, no effect on consumers, and no effect on the final PC market as of the time of trial (over three and one-half years after Rambus began asserting its patents). (McAfee, Tr. 7565-66)).

1054. The conclusion that competition has not been adversely affected by Rambus's alleged failure to disclose is bolstered by the likelihood that JEDEC would have selected Rambus's four technologies had Rambus never joined JEDEC. This demonstrates that JEDEC members, acting as rational manufacturers, would have selected Ramubus's technologies, so that standardization by JEDEC did not increase Rambus's market power. (Rapp, Tr. 9863).

1055. Because the but-for world outcome is the same as the actual world outcome, Rambus's alleged conduct caused it to gain no additional market power. (Teece, Tr. 10312-13).

c. Intel's Choice of RDRAM Conferred Market Power, Not JEDEC Standardization

1056. In the 1995-1996 time period, Intel spent about a year exploring various alternatives for the next generation DRAM. (MacWilliams, Tr. 4800-01). Intel looked at EDO, SDRAM, DDR, SyncLink, and Rambus. (MacWilliams, Tr. 4800-01). Other than these alternatives, "the memory vendors didn't have any other good ideas." (MacWilliams, Tr. 4800-01).

1057. An internal Intel document written by Peter MacWilliams explained that the DRAM manufacturers were not focused on improving DRAM technology: "[u]p to this point in time, [(Q395)] memory vendors were strictly focus[]ing on lowering costs and increasing density – Intel felt the memory vendors needed to get more focused on increasing access speed." (RX 1532 at 1).

1058. Intel saw a growing performance gap in the mid-1990's between CPU performance and DRAM performance. (RX 868 at 3). After examining the alternatives for a year, Intel chose RDRAM to be its next generation DRAM technology. (MacWilliams, Tr. 4800-01).

1059. Intel chose RDRAM because of the need for higher bandwidth for use with faster CPUs and the need to satisfy memory needs driven by more I/O demands and new applications. (RX 904 at 5-6; *see also* RX 805 at 2 (December 1996 Intel document reciting need for increased bandwidth driven by memory intensive applications such as visual computing and noting that Intel was looking for technology beyond 100 MHz SDRAM)).

1060. Intel's choice of RDRAM was significant. As Richard Heye of AMD – Intel's competitor in the microprocessor market – explained, in the late 1990's AMD believed that RDRAM would become the next volume memory product (even though the

technology was "revolutionary") because it had been chosen by Intel:

> And given that, you know, Intel, who owns 80 percent of the market, really put his wood behind the arrow, so to speak, on Rambus, you know, they had talked about the customers, well our customers were saying, hey, you ought to use Rambus, and we talked to the memory vendors. And the memory vendors were saying, you know what, Rambus, it's a revolutionary change, not evolutionary, but, you know, that's the way the industry is going, that's the way we're going to go, and Rambus is it.

(Heye, Tr. 3685).

1061. Steve Polzin of AMD testified that it was important to AMD that Intel chose RDRAM because Intel's selection would make RDRAM a *de facto* standard: "[Intel] drove the volume, and if the volume DRAM was Rambus, that would become the commodity part, and we had to remain competitive in terms of both performance and cost, and if the indications were most of the DRAMs to be built in the world were going to be Rambus DRAMs, we better be compatible with them." (Polzin, Tr. 3941-42).

1062. Intel's selection of RDRAM was also significant to the PC OEMs. For example, Compaq, one of the largest producers of personal computers in the world stated in a November 1998 Compaq Memory Update that Compaq was planning to incorporate RDRAM into all Compaq products. (RX 1302 at 8). Jacquelyn Gross, the Director of Memory Procurement at Compaq (Gross, Tr. 2265), testified that Compaq was planning to transition all of its products – desktops, workstations, etc. – to RDRAM at rate higher than it had ever changed memory technologies before. (Gross, Tr. 2324-27). As described in

Compaq's documents, this was the "[m]ost aggressive, cross divisional memory technology shift ever planned at Compaq." (RX 1302 at 8). This was planned, even though Compaq considered RDRAM to be "revolutionary." (Gross, Tr. 2327).

1063. Similarly, an October 1998 internal presentation reflects Compaq's sentiment at the time that "Rambus is the clear next generation memory" technology. (RX 1287 at 4). As Gross explained, the reason for this belief was that Intel had told Compaq that it was going to produce chip sets for RDRAM. (Gross, Tr. 2317-18). This was important to Compaq because ninety percent of Compaq's PC applications used Intel chipsets. (Gross, Tr. 2317-18).

X. THE CHALLENGED CONDUCT WAS NOT EXCLUSIONARY

A. Rambus Had a Legitimate Business Justification For Not Disclosing its Proprietary Patent Information

1064. Crisp was advised by Vincent, Rambus's outside patent counsel, in the 1992 time frame, about the importance of keeping patent applications confidential. Crisp testified that Vincent "told us to not disclose our patent applications. They were confidential." Crisp understood that the consequences that might result from disclosure of applications included "that companies could potentially file interference actions on our patent applications in the patent office; that in certain countries where the rules are first to file, somebody could potentially file a claim before we actually did; and that we basically would be disclosing trade secrets that could work against us in terms of our competitive position in the marketplace." Crisp followed this advice. (Crisp, Tr. 3496).

1065. Crisp commented about Rambus's reasons not to disclose patent applications in a September 23, 1995 email:

> [W]e decided that we really could not be expected to talk about potential infringement for patents that had not issued both from the perspective of not knowing what would wind up being acceptable to the examiner, and from the perspective of not disclosing our trade secrets any earlier than we are forced to.

(CX 837 at 2).

1066. Respondent's economic expert, Dr. Rapp, received a bachelor's degree in economics from Brooklyn College in 1965, a master's degree in economic history from the University of Pennsylvania in 1966, and a Ph.D. in economic history from the University of Pennsylvania in 1970. (Rapp, Tr. 9766). He is the president of NERA, which is an economics consulting firm with five hundred employees that specializes in the economics of competition, including industrial economics, antitrust and intellectual property. (Rapp, Tr. 9764). He has been an economic consultant with NERA since 1977 and the president of NERA since 1988. (Rapp, Tr. 9764). Prior to his joining NERA, Dr. Rapp was a tenured professor at the State University of New York at Stony Brook. (Rapp, Tr. 9766).

1067. In addition, Dr. Rapp has published articles on predatory pricing, intellectual property economics, and innovation in high-technology markets. (Rapp, Tr. 9768-69). In the past fifteen years, a great deal of his consulting work has been in the area of high-technology antitrust and intellectual property, typically in the computer and semiconductor industries. (Rapp, Tr. 9769-70).

1068. Dr. Rapp has been qualified as an expert on numerous occasions. Since the early 1980's, Dr. Rapp has testified in hearings or trials as an antitrust economics expert, on average, about once per year. (Rapp, Tr. 9771). He has testified at least

five times as an expert on the economic aspects of intellectual property issues. (Rapp, Tr. 9771-72).

1069. Dr. Rapp testified that Rambus's alleged conduct was not exclusionary. (Rapp, Tr. 9921).

1070. Complaint Counsel's economic expert, Professor McAfee, did not criticize or rebut Dr. Rapp's opinion that Rambus's conduct was not exclusionary because of the presence of a legitimate business justification. To the contrary, McAfee admitted that concealing information, even if it discourages competitors from entering a market, is not exclusionary. (McAfee, Tr. 7525-27). McAfee also admitted that it is not exclusionary to conceal an invention from competitors in order to take advantage of the invention while others cannot. (McAfee, Tr. 7527-28).

1071. Professor McAfee admitted that the only "candidate purpose" he considered for Rambus's withholding information about its patent applications was monopolization, i.e., he did not consider other purposes that might have led Rambus to take the risk that he identified. (McAfee, Tr. 7539).

1072. The protection of trade secrets, including intentions about amending pending claims, is a valid business justification for not disclosing information regarding pending patent applications and intentions to file applications in the future. (Rapp, Tr. 9915-16).

1073. Disclosure of trade secrets, including pending patent applications or intentions to file or amend future applications, even after a parent patent application becomes public, may: (1) jeopardize the issuance of pending claims by enabling competitors to file patent interferences or to race to be first-to-file in certain foreign jurisdictions; and (2) result in a loss of competitive advantage by informing competitors of the firm's R&D focus or by inducing competitors to begin work around efforts earlier. (Rapp, Tr. 9916-18, 9926).

1074. Even after the ‘898 application had been disclosed (in the form of the PCT application), Rambus still had trade secrets (additional pending applications and intentions to file additional applications) that it could legitimately protect from disclosure. (Rapp, Tr. 9926).

1075. Prior to 1999, patent applications were kept strictly confidential by the PTO until patent issuance. (Fliesler, Tr. 8830).

1076. Patent applications are generally kept confidential by applicants for as long as possible. (Fliesler, Tr. 8829-30). Applicants have no enforceable rights until a patent issues and generally do not want to have their technology disclosed to competitors until such time as they do have enforceable patent rights. (Fliesler, Tr. 8829-30). In the 1990 to 1996 time frame, if a patent ultimately did not issue from an application, the application would remain secret and the applicant could retain trade secret protection over the material in the application. (Fliesler, Tr. 8836-37).

1077. As of October 31, 1991, Rambus had no trade secret protection over the written description, drawings, and original one hundred fifty claims of the ‘898 application. (Fliesler, Tr. 8894).

1078. Companies often are wary of disclosing patent applications because to do so would be to disclose to competitors the areas of technology that the company is developing and the areas of technology for which the company is seeking patent protection. (Fliesler, Tr. 8840).

1079. Even when a patent has issued from an original application – which results in disclosure of the drawings and written description – the applicant would still have reasons to keep confidential other applications claiming priority back to that original application. (Fliesler, Tr. 8837-38). It would be very valuable to a competitor to know what claims the applicant is

actually pursuing in those other applications from the entirety of inventions that could be claimed based on the written description. (Fliesler, Tr. 8838, 8900-02).

1080. Similarly, even if a corresponding international patent application is published, there remain business reasons for not disclosing a United States patent application, because information about the particular claims being pursued constitutes strategic business and technical information that a company would want to keep from its competitors. (Fliesler, Tr. 8840-41, 8894-96).

1081. In addition, if information about pending applications were disclosed by a company to a competitor, the competitor could potentially slow down or interfere with the prosecution of the application. (Fliesler, Tr. 8841). The competitor could disclose prior art to the company, for example. Even if it is not relevant prior art, it could cause a dilemma for the company about whether the information triggered a duty to disclose prior art to the PTO, potentially confusing or delaying the patent prosecution. (Fliesler, Tr. 8841-42).

1082. The competitor could also try to provoke an "interference" at the patent office – that is, a proceeding to determine which of two applicants claiming the same invention was actually the first to invent and entitled to a patent – by claiming the same invention in one of the competitor's applications. (Fliesler, Tr. 8834-35, 8842).

1083. In the United States, patents are generally awarded to the applicant who was the first to invent a given invention. (Fliesler, Tr. 8834-35). Most foreign jurisdictions, however, have a first to file rule: The first applicant to file an application that is otherwise entitled to a patent will be awarded the patent. (Fliesler, Tr. 8838-39). Through treaties to which the United States is a party, a patent applicant has up to one year following the filing date of his U.S. patent application to file a corresponding application in foreign countries. If he does so, the foreign country

accords the application a priority date, meaning a legally effective filing date in that foreign country, of the U.S. application. (Fliesler, Tr. 8839-40). Which applicant is the first to file an application in a foreign country will be judged according to the priority date. (Fliesler, Tr. 8839-40).

1084. Martin Fliesler, a patent attorney with over thirty years of experience prosecuting patent applications, advises his clients that they should not disclose patent applications, but instead should keep them confidential. (Fliesler, Tr. 8765-72, 8842-43).

1085. The need to keep patent applications confidential was well recognized in the semiconductor industry. JEDEC members were informed in 1992 of potential negative consequences flowing from premature disclosure of inventions. In October 1992, JC 42 Chairman Jim Townsend circulated an article entitled "Don't lose your patent rights" to members of the JC 42 committee. (CX 342 at 8). The article advises inventors to "keep it under your hat" because disclosure of an invention may waive any rights to obtain a patent. The article states that in the United States, a disclosure made one year before filing an application can bar a patent, while in some foreign jurisdictions, any disclosure before filing an application will bar a patent. (CX 342 at 8).

1086. Rambus's keeping information about its pending or future patent applications confidential did not impose on Rambus costs or risks that were compensable only by excluding rivals and thereby gaining market power. (Rapp, Tr. 9924).

1087. These conclusions apply in the standard setting context as in any other. A company that is the member of a standard setting body may benefit from not disclosing information regarding its pending patent applications or its intentions to file future patent applications regardless what standards are developed. (Rapp, Tr. 9919-20). The benefits to a company keeping control of its business and intellectual property strategies do not depend on which standard is chosen by the standard setting

body. (Rapp, Tr. 9919-20). These benefits have to do with maximizing the ability to operate competitively, not standardization. (Rapp, Tr. 9920).

B. Rambus's Conduct Did Not Impact Equal or Superior Alternatives

1088. The evidence shows that Rambus's conduct was not exclusionary even as that term was defined by Complaint Counsel's expert, Professor McAfee. The exclusion of inferior products from the market is not exclusionary in an economic sense. (McAfee, Tr. 7536).

1089. According to Professor McAfee, in order for conduct to be exclusionary, it must impact equal or superior alternatives. (McAfee, Tr. 7537). Professor McAfee defined the phrase equal or superior alternatives to include the commercially viable alternatives that could have been chosen had Rambus disclosed. (McAfee, Tr. 7762-63).

1090. Dr. Rapp testified that the cost differences that he quantified and the performance advantages of the Rambus technologies made the Rambus technologies superior to the alternatives in cost-performance terms. (Rapp, Tr. 9861-62).

1091. Professor McAfee admitted that he did not quantify any cost differences between Rambus's technologies and the alternative technologies. (McAfee, Tr. 11340).

1092. Although Professor McAfee admitted that JEDEC members would consider the performance of alternatives in deciding whether to pursue the alternatives (McAfee, Tr. 11340), he did not quantify the performance differences between Rambus's technologies and any of the alternatives he claimed were commercially viable. (McAfee, Tr. 7581-82, 11340).

1093. Professor McAfee also admitted that JEDEC members would consider the "headroom" or future flexibility of alternatives in deciding whether to pursue the alternatives. (McAfee, Tr. 11340). He did not, however, compare the headroom or future flexibility of Rambus's technologies with any of the alternatives he proposed as commercially viable. (McAfee, Tr. 11340-41).

1094. For example, Professor McAfee admitted that JEDEC behavior and JEDEC discussions show that JEDEC members valued multiple latencies and multiple burst lengths, yet he did not quantify that value. (McAfee, Tr. 11351).

1095. Professor McAfee also testified that, although he had made no effort to determine if any intellectual property covered any of the alternatives that he considered commercially viable other than Kentron's technology, the presence of intellectual property could render a technology not commercially viable in his opinion, because JEDEC attached a "penalty" to the presence of intellectual property. (McAfee, Tr. 7582-85).

C. The "Commercial Viability" Analysis of Complaint Counsel's Economic Expert

1096. Professor McAfee testified that he believed that equal or superior alternatives were excluded by Rambus's alleged conduct. His definition of "equal or superior," however, was flawed. To determine whether equal or superior alternatives were excluded, Professor McAfee developed a "commercial viability" test. (McAfee, Tr. 7330-31).

1097. Although he claimed that his methodology was "parallel" to standard economic tests, Professor McAfee admitted that he was aware of no economic literature that describes the use of a "commercial viability" test to determine market substitutability of alternatives. (McAfee, Tr. 7567).

1098. According to Professor McAfee, an alternative was "commercially viable" if it constrained the price of Rambus's technologies. (McAfee, Tr. 7330-31). But defined that way, the concept of "commercially viable" does not mean that the technology is "equal or superior." Even weak substitutes can constrain the price of a technology. (Rapp, Tr. 9860). An alternative can therefore be "commercially viable" in this sense without being equal or superior or even a viable alternative in any practical sense. (Teece, Tr. 10368, 10370-71).

1099. When determining whether an alternative was price constraining, Professor McAfee provided no analysis of price elasticity. In other words, he did not consider the price level required before the alternatives would actually constrain the price. Instead, he simply looked for evidence that the alternative was considered as a possible alternative by members of JEDEC and that knowledgeable engineers now claimed that the alternative was viable. (McAfee, Tr. 7333-34).

1100. Further, Professor McAfee tied his notion of commercial viability to subjective judgments of JEDEC members (McAfee, Tr. 7335) and considered the opinions of Professor Jacob, (*see, e.g.*, McAfee, Tr. 7360) and the cost information provided by Respondent's expert Michael Geilhufe. (McAfee, Tr. 11199, 11249-78).

1101. Professor McAfee judged patented technologies to be "hobbling" because the JEDEC rules put a "penalty" on technologies that were covered by intellectual property. (McAfee, Tr. 7337, 7582-83). He thus regarded patented technologies, such as Rambus's, as inferior based on the presence of intellectual property and without regard to the level of royalties sought for that technology.

1102. In a competitive market, if the best solution in cost-performance terms is patented and involves the payment of royalties, competition will dictate that the royalties be paid and

that the patented solution is adopted. (Rapp, Tr. 9939). While individual executives in an industry may dislike paying royalties, just as they may dislike paying health care costs for workers or a competitive wage, they will have no choice because competition will mandate that these costs be incurred. (Rapp, Tr. 9938-39).

1103. Professor McAfee also considered "a perception of the magnitude of those problems" associated with that technology as "relevant to the determination of which technologies should be selected." (McAfee, Tr. 7586). In other words, he based his determination of whether a technology was "equal or superior" on the subjective perceptions of JEDEC members at the time, regardless of whether these perceptions were ultimately correct. While this factor may go to whether JEDEC would have selected the technology, it does not go to whether the alternative is equal or superior in objective terms.

1104. Professor McAfee considered each company's strategic interests in which technology would be selected because of differences in technical ability. (McAfee, Tr. 7338-39). In determining whether a technology was commercially viable, he factored in whether some JEDEC members might prefer the technology because they were better equipped to produce it. Again, while this factor may go to whether JEDEC would have selected the technology, it does not go to whether the alternative is equal or superior in objective terms.

1105. Professor McAfee relied on his notion of "satisficing" to conclude, in effect, that a product that has lesser performance is nonetheless "equal" to one with better performance. (McAfee, Tr. 7335-36). Because he believed that JEDEC was "satisficing," Professor McAfee essentially defined "equal" to include technologies that were inferior to Rambus's technologies. Professor McAfee defined satisficing as referring to the process by which an organization like JEDEC will choose an adequate solution to a problem it faces rather than expending the effort to find the perfect solution. (McAfee, Tr. 7255-56).

1106. Rather than examining the actual cost differences between the Rambus technologies and the alternatives, Professor McAfee opined that he had considered an amalgam of factors and determined that certain alternatives were "commercially viable" based on the information he analyzed. (*See, e.g.*, McAfee, Tr. 7363). Professor McAfee did evaluate the alternatives using the cost information provided by Geilhufe and found that, using those cost estimates, there were a number of commercially viable alternatives to the technologies claimed by Rambus. (McAfee, Tr. 11249-78).

1107. While Professor McAfee testified that it was likely that at least one of the technologies he deemed commercially viable alternatives to Rambus's technology was equally efficient or superior to Rambus's technology, he admitted that he could not identify any particular technology as equal or superior to Rambus's technologies. (McAfee, Tr. 7578-79).

D. The Assumption by Complaint Counsel's Economic Expert that Rambus Knowingly Assumed the Risk Of Losing Its Ability To Enforce Its Patents

1108. In determining that Rambus's conduct was exclusionary, Professor McAfee assumed that Rambus knowingly took a risk that it might lose the ability to enforce its patents by not disclosing patent interests that it did not disclose. (McAfee, Tr. 7538-40).

1109. But Professor McAfee admitted that Rambus would have understood that if it withheld information about its patent applications that it should have disclosed, any effort to enforce its patents once they issued, would have triggered an inquiry into whether Rambus should have disclosed its patent interests. In addition, Professor McAfee admitted that if a JEDEC member failed to disclose patent interests that should have been disclosed and revealed knowledge of that patent interest, e.g., in a written

document, the risk of a challenge that would render the patents invalid would increase substantially. (McAfee, Tr. 7550).

E. The Assumption by Complaint Counsel's Economic Expert That Rambus Violated a JEDEC Rule or Made Misrepresentations to JEDEC

1110. Professor McAfee explained that Rambus's concealing of information about its patent applications would, in his opinion, be exclusionary only if it violated a rule or process. (McAfee, Tr. 7530-31, 7546). Professor McAfee assumed that Rambus's conduct included a violation of a JEDEC rule or process. (McAfee, Tr. 7530). An alternate assumption was that Rambus made misrepresentations to JEDEC. (McAfee, Tr. 7478).

1111. Professor McAfee assumed that Rambus "should have disclosed patents or patent applications with reference to all four of the technologies challenged in the case." (McAfee, Tr. 7546). But he admitted that, "[i]f they shouldn't have disclosed on one of the technologies, then my finding of exclusionary conduct on that technology is no longer – on that particular technology would no longer be reliable because I've assumed that they should have disclosed on that technology." (McAfee, Tr. 7546).

1112. Professor McAfee admitted that he did his analysis with no assumptions about the specific claims of any patent application that Rambus should have allegedly disclosed. (McAfee, Tr. 7669-70).

1113. Professor McAfee also admitted that he did his analysis with no assumptions about the specific date that Rambus allegedly should have made the disclosures that Complaint Counsel allege should have been made. (McAfee, Tr. 7671).

1114. Professor McAfee also admitted that he did his analysis with no assumed specific triggering event that would have caused

Rambus to be obligated to make disclosures to JEDEC. (McAfee, Tr. 7671).

1115. Professor McAfee admitted that if work on DDR had not begun by the time Rambus had left JEDEC and if there was no duty to disclose absent such work, the conclusions that he drew from assuming that Rambus failed to disclose with regard to DDR would fall away. (McAfee, Tr. 7575).

1116. Professor McAfee admitted that if Rambus had made the additional disclosures that Complaint Counsel allege should have been made, JEDEC ignored the disclosure, and JEDEC incorporated the Rambus technology nonetheless, Rambus would not have engaged in exclusionary conduct. (McAfee, Tr. 7682).

1117. Professor McAfee also admitted that there are situations in which JEDEC could become aware of Rambus's potential patents other than through Rambus's disclosure of that information to JEDEC, such that Rambus's failure to disclose would not, as a matter of economics, constitute exclusionary conduct. (McAfee, Tr. 7686).

1118. Professor McAfee further admitted that it is plausible with his assumptions that if Rambus never joined JEDEC, JEDEC would have selected the four Rambus technologies for inclusion in its standards. (McAfee, Tr. 7688).

F. The Economic Evidence Regarding "Hold Up" and Disclosure Costs

1119. Professor McAfee based his analysis that Rambus's conduct was exclusionary on several assumptions, one of which was the assumption that Rambus's conduct violated a JEDEC rule or process. (McAfee, Tr. 7530-31).

1120. Professor McAfee admitted that he had done no analysis to determine whether JEDEC's rules and processes advanced the interests of antitrust law. (McAfee, Tr. 7532-33).

1121. Nor did Professor McAfee perform any analysis of JEDEC's costs and benefits in order to determine the economically efficient disclosure rules for it to impose. (McAfee, Tr. 7727). In fact, he admitted that he has not investigated the economic efficiency of JEDEC's rules. (McAfee, Tr. 7727-28).

1122. As an economic matter it is disputed whether the optimal time for disclosure of information regarding patent interests is as early in the standardization process as possible. (Teece, Tr. 10385). As Professor Teece testified, disclosure involves costs, so the optimal time for disclosure must consider those costs. (Teece, Tr. 10385). Depending on the costs and benefits, later disclosure may be optimal. (Teece, Tr. 10402).

1123. The costs of disclosure include the cost to the patent applicant of losing trade secrets and confidentiality. (Teece, Tr. 10453). The costs to the standard setting organization are that it must try to evaluate and assess the highly preliminary information regarding the patent application. (Teece, Tr. 10453-54).

1124. Since patents are not going to change and are public, the costs associated with disclosing patents are less than those associated with disclosing patent applications. (Teece, Tr. 10454-55).

1125. The narrower the scope of disclosure regarding patent applications, the lower the costs and burdens of disclosure. (Teece, Tr. 10454, 10547-58). If intellectual property issues are put aside once a RAND assurance is given, there is less need for disclosure. (Teece, Tr. 10548).

1126. Professor McAfee admitted that JEDEC's disclosure rules do little to mitigate risk of hold up because the disclosure

obligation applies only to the knowledge of the representative at the meeting, rather than that of the member company (McAfee, Tr. 7724) and because, in large companies, the representative might not have a lot of knowledge about the company's patents. (McAfee, Tr. 7724-25).

1127. Professor McAfee also admitted that a JEDEC disclosure requirement would not mitigate the risk that the standard might involve technology covered by patents held by nonmembers. (McAfee, Tr. 7725).

XI. THE EVIDENCE DOES NOT SUPPORT COMPLAINT COUNSEL'S ARGUMENT THAT THERE WERE VIABLE ALTERNATIVES TO RAMBUS'S TECHNOLOGIES

A. The Testimony of Professor Jacob Regarding Allegedly Viable Alternatives Is Not Persuasive

1128. Complaint Counsel's expert witness regarding viable alternatives, Professor Jacob, has never done DRAM circuit design. (Jacob, Tr. 5588). Indeed, Professor Jacob had never designed any circuits for computer chips (even apart from DRAMs) that were to be fabricated prior to 2002. (Jacob, Tr. 5588). Aside from reviewing some DRAM data sheets, Professor Jacob, who was a student at the time, had no particular DRAM-related experience in the mid-1990's. (Jacob, Tr. 11148). Professor Jacob did not obtain his graduate degree and begin to teach electrical engineering until 1997. (Jacob, Tr. 5357).

1129. By contrast, Respondent's technical experts have a wealth of relevant experience in the DRAM and semiconductor industries. Dr. Soderman was employed in the semiconductor industry for over thirty years during which time he designed DRAMs as well as various other types of integrated circuits. (Soderman, Tr. 9329-36).

1130. Likewise, Michael Geilhufe worked in the semiconductor industry for over thirty years. (Geilhufe, Tr. 9543-52). Geilhufe holds four patents for DRAM design and managed Intel's international manufacturing operations which involved working closely with DRAM manufacturers such as Samsung. (Gelhufe, Tr. 9549-50, 9553).

1131. In Professor Jacob's publications comparing certain DRAM architectures, he tried to model their performance as precisely as possible using software simulation. In contrast, Professor Jacob did no such software simulation with respect to the alternatives that he proposed to Rambus's technology. (Jacob, Tr. 5589).

1132. With the exception of three of his alternatives (using a burst terminate command, increasing the number of pins on the DRAM, and increasing the number of pins on the module), Professor Jacob did no simulation or modeling of any kind to try to assess the alternatives' performance. (Jacob, Tr. 5590-91).

1133. Professor Jacob's proposed alternatives were not sufficiently detailed to enable an actual circuit design. (Geilhufe, Tr. 9673).

1134. Professor Jacob did not do any investigation to determine whether any of his proposed alternatives were covered by patents owned by Rambus or others. (Jacob, Tr. 5601).

B. Complaint Counsel Did Not Prove That There Were Viable Alternatives to the Rambus Technologies Adopted in the SDRAM

1. Programmable CAS Latency

1135. Complaint Counsel have suggested, through their technical expert, Professor Jacob, the following possible alternatives to programmable CAS latency in SDRAMs:

(1) Use fixed CAS latency parts;

(2) Program CAS latency by blowing fuses on the DRAM;

(3) Scale CAS latency with clock frequency;

(4) Use dedicated pins to transmit latency information from the controller to the DRAM;

(5) Explicitly identify CAS latency in the read command;

(6) Stay with an asynchronous-style DRAM.

(Jacob, Tr. 5370-96).

a. Complaint Counsel Did Not Prove That the Use of Fixed CAS Latency Parts Was a Viable Alternative

1136. One of the alternatives proposed by Professor Jacob for programmable CAS latency was to fix the CAS latency at the design stage, the manufacturing stage, or the packaging stage. (Jacob, Tr. 5371). Fixing CAS latency at the design stage would result in a single part with only one CAS latency. (Jacob, Tr. 5373). Fixing CAS latency at the processing stage would involve a "metal mask option" that would fix the CAS latency to one value or another. (Jacob, Tr. 5373-75). Fixing CAS latency during packaging would require a multiplexer that would be hardwired to either power or ground during the packaging process to select one of two latency values. (Jacob, Tr. 5375-76).

1137. Multiple CAS latency values are required for SDRAMs because users of DRAMs would prefer to buy parts that they can insert in a variety of systems with different bus speeds. (RX 1626

at 3-4; Soderman, Tr. 9346-47). The appropriate CAS latency for a part will depend on the bus speed and the access time of the DRAM. (Soderman, Tr. 9347-48). Therefore, using fixed latency parts would require multiple fixed latency parts, as opposed to a single, programmable latency part. (Soderman, Tr. 9347-48).

1138. Mark Kellogg of IBM testified that, in the 1992 time frame, "we weren't convinced that we knew the right latency and we did expect that the DRAM frequency would go up over time – that we knew the correct latency if we were to select one and we expected that the DRAM frequency would increase over time, which meant we might wish to change the CAS latency." (Kellogg, Tr. 5139).

1139. The mode register in SDRAMs and DDR SDRAMs reserves three bits for CAS latency, allowing for up to eight different CAS latency values. (CX 234 at 150).

1140. Release 4 of JEDEC Standard 21-C (November 1993), which contains the first published SDRAM standard, specified three required CAS latency values (1, 2, and 3) and one optional CAS latency value (4). (JX 56 at 114; Lee, Tr. 11003-04). Release 9 of JEDEC Standard 21-C (August 1999), which contains the first published DDR SDRAM standard, specified two required CAS latency values for SDRAMs (2 and 3) and one optional value (4); it also specified two required CAS latency values for DDR SDRAMs (2 and 2.5) and three optional values (1.5, 3, and 3.5). (CX 234 at 150; Lee, Tr. 11068-72).

1141. Although not all of the eight possible values of CAS latency are used in SDRAMs and DDR SDRAMs, the other possibilities were reserved to preserve flexibility for future additions. (Lee, Tr. 11072-73).

1142. Desi Rhoden gave a presentation on "Future SDRAM" at the March 1996 meeting of the JEDEC 42.3 subcommittee. (JX 31 at 64; Rhoden, Tr. 489-90). The presentation indicates that

CAS latencies of 2, 3, 4, 5 and 6 would be required for different generations of SDRAMs. (JX 31 at 64; Rhoden, Tr. 490-91).

1143. JEDEC's DDR2 SDRAM standard intends to expand the use of programmable latency. (Soderman, Tr. 9351-53). Preliminary DDR2 SDRAM data sheets from both Hynix and Samsung indicate that DDR2 SDRAMs will continue to have three bits in the mode register reserved for CAS latency, allowing for up to eight different CAS latency values. (RX 2099-14 at 21; RX 2099-39 at 20; Soderman, Tr. 9351). Hynix's part provides three different CAS latency values (3, 4, 5). (RX 2099-14 at 21; RX 2099-39 at 20; Soderman, Tr. 9351).

1144. DDR2 SDRAMs also reserve three bits in an "extended mode register" for "additive latency," allowing for up to eight different additive latency values. (RX 2099-14 at 24; RX 2099-39 at 22; Soderman, Tr. 9351-53; Lee, Tr. 11068). Hynix's part provides six different additive latency values (0, 1, 2, 3, 4, and 5), while Samsung's part provides five different additive latency values (0, 1, 2, 3 and 4). (RX 2099-14 at 24; RX 2099-39 at 22; Soderman, Tr. 9351-53; Lee, Tr. 11068). The "read latency" in DDR2 SDRAMs (that is, the number of clock cycles from receipt of a CAS command until data is output onto the bus) is the sum of the CAS latency and the additive latency. (RX 2099-14 at 32; RX 2099-39 at 37).

1145. In 1993, Micron's first SDRAM design allowed for four different CAS latencies (1, 2, 3, and 4). (Lee, Tr. 11063-64).

1146. Micron currently sells an SDRAM for the graphics market allowing for three different CAS latencies (1, 2, and 3). (Lee, Tr. 11064-67).

1147. The total unit cost for a mature product built by a first tier DRAM manufacturer in the mid-1990's was approximately two dollars. (Geilhufe, Tr. 9564). Multiple fixed latency parts

would have been an expensive alternative, for several reasons. (Soderman, Tr. 9348-49).

1148. First, manufacturing multiple fixed latency parts would decrease a DRAM manufacturer's yield due to speed distribution. (Soderman, Tr. 9348; Geilhufe, Tr. 9577). DRAMs cannot be accurately tested for speed until after packaging; fixing the CAS latency prior to that time would result in some parts that are not capable of performing at the CAS latency that has been fixed and, therefore, would not be usable. (Soderman, Tr. 9347-49; Geilhufe, Tr. 9577-78). If CAS latency were programmable, those slower parts would be usable at a higher CAS latency value. (Soderman, Tr. 9347-49; Geilhufe, Tr. 9577-78).

1149. Second, fixing CAS latency would result in DRAM manufacturers losing some of the price premium associated with their fastest (i.e., lowest CAS latency) parts which can sell for fifty percent or more over their standard parts. (Soderman, Tr. 9348-50; Lee, Tr. 11074-75). This, again, is because the latency would be fixed prior to accurate speed testing and, consequently, some parts that would be capable of faster performance (i.e., operating at a low CAS latency) will be set to a CAS latency higher than necessary. (Soderman, Tr. 9348-50; Lee, Tr. 11074-75).

1150. Steve Polzin of AMD testified that "Fixed CAS latency would have been pretty onerous for the DRAM manufacturers" and "would have a significant cost impact for the DRAM manufacturers." (Polzin, Tr. 3992).

1151. Joe Macri of ATI testified that [redacted] (Macri, Tr. 4762 (*in camera*)). [redacted] (Macri, Tr. 4762-63 (*in camera*)).

1152. Third, there would have been an increase in design, photo tooling, and qualification costs because multiple products would have had to be designed and manufactured, rather than just one product. (Geilhufe, Tr. 9679, 9682-83, 9690).

1153. Some design effort would have been required for each different CAS latency; one mask would have had to be changed for each different CAS latency; and each different CAS latency part would have had to be qualified before it could be sold. (Geilhufe, Tr. 9575-76, 9578-79).

1154. Fourth, multiple fixed latency parts in place of a single programmable latency part would result in substantial inventory costs. (Soderman, Tr. 9349-50).

1155. Gordon Kelley of IBM testified about the benefits of programmability as follows: "One of the advantages of that is that that drives low cost. The producer does not have to maintain multiple part numbers. One part number fits many applications. That's one of the drivers to low cost." (G. Kelley, Tr. 2550-51).

1156. When first developing the Rambus technology, Drs. Farmwald and Horowitz considered having a fixed latency. (Horowitz, Tr. 8532). Dr. Horowitz learned from an early visit to a DRAM manufacturer the importance of having a single, as opposed to multiple parts. At that time, there were two different packages for DRAMs, and the DRAM manufacturer was making a single die that could fit into either package even though this entailed ten percent additional die area. (Horowitz, Tr. 8532-33). Dr. Horowitz's understanding at the time was that the reason for making a single part despite the die size penalty was that inventory costs from having two different designs during the manufacturing process would be too expensive. (Horowitz, Tr. 8533-34).

1157. Multiple fixed latency parts would also be inferior from the user's standpoint. Because the part could no longer be programmed to operate in various systems, a user would have to pay attention to the part's detailed specifications to determine whether it would work in its system. (Soderman, Tr. 9350-51).

1158. In an April 11, 2000 email responding to a proposal to fix CAS latency in DDR2, Bill Hovis of IBM rejected the idea, both because of cost concerns and because of the benefits to DRAM users from programmable CAS latency. (RX 1626 at 3).

1159. Using fixed latency would not allow for the elimination of the mode register in SDRAMs and DDR SDRAMs because the mode register is used for purposes other than programming CAS latency. In the JEDEC SDRAM standard, the mode register is used for storing CAS latency, burst length and burst type. (CX 234 at 150). Certain SDRAMs being manufactured use the mode register for additional purposes as well, such as for programming operating mode and write burst mode. (RX 2100-13 at 3). The DDR SDRAM standard adds an extended mode register used to enable or disable a DLL. (CX 234 at 176). The DDR2 SDRAM standard expands the use of the mode register even further, with the mode register being used to program burst length, burst type, CAS latency, test mode, DLL reset, and tWR, and the extended mode register being used to program DLL enable, output driver impedance control, RTT, additive latency, OCD, /DQS enable and RDQS enable. (RX 2099-14 at 21, 24; RX 2099-39 at 20, 22).

1160. Although there would have been a decrease in testing costs because each part would have had to be tested for a single CAS latency, rather than for multiple CAS latencies (Geilhufe, Tr. 9576), this cost saving would have been far outweighed by the cost increases due to other factors.

1161. The fixed CAS latency alternative would have resulted in the following approximate net costs compared to the cost of SDRAM in the mid-1990's, assuming a first-tier DRAM manufacturer and a product that is already well down the learning curve with a volume of twenty million unit volume, that is, a product that has already realized its cost improvement: $100,000 increase in product design costs per latency; $50,000 increase in photo tooling costs per latency; one cent decrease per unit in testing costs at wafer sort; three cents per unit cost increase due to

reduced good die yield; two cents per unit increase in inventory costs; and $250,000 increase in qualification costs per latency. (Geilhufe, Tr. 9562-64, 9575-79).

1162. The net increase in variable costs for the fixed CAS latency alternative is, therefore, approximately four cents per unit. The total cost increase is approximately six cents per unit, calculated by converting the fixed costs to per unit costs through division by twenty million (the unit production run) and adding the resulting per unit fixed costs to the per unit variable costs. (Geilhufe, Tr. 9579).

1163. The additional inventory cost estimate is based on three different fixed latency parts being manufactured, the number of required CAS latencies in the original SDRAM standard, instead of a single programmable latency part. (Geilhufe, Tr. 9578; JX 56 at 114).

1164. The estimate for increased inventory costs is conservative, because inventory costs due to multiple products can be much larger. For example, in 1989, Apple Computer reported $27 million quarterly loss attributed entirely to purchasing a DRAM part that they could no longer use in their systems. (Geilhufe, Tr. 9587). This amounted to a loss of about five to six dollars per unit. (Geilhufe, Tr. 9588).

b. Complaint Counsel Did Not Prove That Programming CAS Latency with Fuses Was a Viable Alternative

1165. Professor Jacob's proposed alternative of programming CAS latency with fuses is similar to his fixed CAS latency alternative because, once the fuse is blown, the part has a fixed CAS latency. (Jacob, Tr. 5378-79).

1166. Fuses can be blown by lasers or electrically. (Jacob, Tr. 5380).

1167. Laser-blown fuses are more reliable than electrically-blown fuses. (Soderman, Tr. 9356-57; Geilhufe, Tr. 9581-82 (Certain products using electrically blown fuses were discontinued at Intel for reliability reasons.)).

1168. In the 1995 time frame, the dominant fuse technology used by major DRAM manufacturers was laser fuse technology. (Geilhufe, Tr. 9581-82). There are DRAM manufacturers who do not have the technology to blow fuses electrically and did not have such technology in the 1995-2000 time frame. (Jacob, Tr. 5596; Geilhufe, Tr. 9740-41).

1169. Fixing the CAS latency with laser-blown fuses prior to packaging would lead to the same logistical difficulties as Professor Jacob's fixed CAS latency alternative. (Soderman, Tr. 9354).

1170. Another disadvantage of using fuses is that the manufacturer would have to blow the fuses after receiving orders for parts, leading to a "time lag from request to delivery of parts." (Kellogg, Tr. 5131).

1171. Laser blown fuses could not be blown by OEMs (original equipment manufacturers) because they cannot be blown after packaging. (Jacob, Tr. 5378-80; Soderman, Tr. 9354-56). Electrically-blown fuses can be blown after packaging, but they still could not be blown by OEMs because the part must be tested after the fuse is blown to make sure it is operating correctly. (Soderman, Tr. 9517). OEMs do not have the capability to perform such testing. (Soderman, Tr. 9354-56).

1172. There would have been an increase in design costs due to the design effort to provide the fuses required. (Geilhufe, Tr. 9575, 9584-85).

1173. There would have been an increase in testing costs due to the time required to blow a fuse and perform certain additional steps. (Geilhufe, Tr. 9585).

1174. There would have been reduced good die yield, inventory, and qualification costs of the same magnitude as the corresponding increases for the fixed CAS latency alternative because, once the fuse is blown, the part is a fixed latency part. (Geilhufe, Tr. 9585-89).

1175. Programming CAS latency by blowing fuses would have resulted in the following approximate net costs compared to SDRAM in the mid-1990's, assuming a first-tier DRAM manufacturer using existing laser fuse technology and a product that is already well down the learning curve with a volume of twenty million unit volume, that is, a product that has already realized its cost improvement: $100,000 increase in product design costs per latency; one cent increase per unit in testing costs at wafer sort; three cents per unit cost increase due to reduced good die yield; two cents per unit increase in inventory costs; and $250,000 increase in qualification costs per latency. (Geilhufe, Tr. 9562-64, 9584-86, 9589).

1176. The net increase in variable costs for the alternative of programming CAS latency by blowing fuses is, therefore, approximately six cents per unit. The total cost increase is approximately seven cents per unit, calculated by converting the fixed costs to per unit costs through division by twenty million (the unit production run) and adding the resulting per unit fixed costs to the per unit variable costs. (Geilhufe, Tr. 9589).

1177. If the DRAM manufacturer did not have antifuse or electrically blown fuse technology available and wished to use that technology, adding it to the manufacturing process would entail several million dollars in additional development costs. (Geilhufe, Tr. 9583-84).

c. Complaint Counsel Did Not Prove That Scaling CAS Latency With Clock Frequency Was a Viable Alternative

1178. Professor Jacob's proposed alternative of scaling CAS latency with clock frequency involves having the DRAM either being informed of the frequency by the memory controller or using some sort of internal circuitry to sense the frequency. The DRAM would then calculate the appropriate CAS latency to use based upon its own inherent latency. (Jacob, Tr. 5383).

1179. Professor McAfee did not testify that this alternative was commercially viable. (McAfee, Tr. 7363).

1180. Having the controller send the bus speed information to the DRAM would require extra pins and circuitry on the controller and, potentially, extra pins on the DRAM, adding manufacturing expense. (Soderman, Tr. 9359-60).

1181. Having the DRAM sense the bus speed would require complex and costly circuitry on the DRAM. (Soderman, Tr. 9358).

1182. Scaling CAS latency with clock frequency is not an alternative to using a register to store a latency value because the latency value would still have to be stored in a register, potentially violating Rambus's patents. (RX 1626 at 2; Soderman, Tr. 9359).

1183. For example, upon a formal infringement analysis, this alternative might be determined to be covered by claim 1 of U.S. Patent No. 5,953,263, assigned to Rambus. (CX 1517 at 29).

1184. Scaling CAS latency with clock frequency was actually proposed by Micron as an alternative to programmable CAS latency for DDR2. At the March 2000 meeting of the JEDEC JC 42.3 subcommittee, Micron made a first showing entitled "Simplifying Read Latency for DDRII." (CX 154A at 9, 25-32).

In its presentation, Micron noted that one approach would be to "offer devices with a fixed read latency." (CX 154A at 26). Under this approach, "[v]endors can offer different speed devices, each with a different fixed latency," but there would be the "[d]isadvantage" that "[u]sers may need to order different parts to cover different applications." (CX 154A at 26).

1185. Micron went on to present a second approach, proposing to scale CAS latency with clock frequency: "offer devices with programmable operating frequency; each operating frequency range has a fixed read latency associated with it." (CX 154A at 27).

1186. In an email dated April 13, 2000 from Mark Kellogg of IBM to Art Kilmer of IBM, Kellogg discussed the proposals made by Micron at the March 2000 JEDEC meeting in the context of the Rambus patents. (RX 1626 at 2). Kellogg noted that "[i]n the last JEDEC meeting, the option of a single latency device was pooh-poohed." (RX 1626 at 2). Kellogg went on to discuss Micron's alternative proposal of scaling CAS latency with clock frequency. Kellogg stated:

> [T]he alternate proposal from Micron (programming the frequency range instead of CAS Latency) was better-received. The problem with the latter proposal (in my mind), was that nothing changed except the name assigned to the command register bits (originally defined as CAS Latency, now to be defined as frequency range or something similar). As such, I felt they were walking a fine line and that this change would not hold up in court as being anything other than an attempt to circumvent possible patent infringement via a term redefinition.

(RX 1626 at 2).

d. Complaint Counsel Did Not Prove That Using Dedicated Pins to Identify the Latency Was a Viable Alternative

1187. Professor Jacob's proposed alternative of using an existing or dedicated pin to identify the latency involves a pin on the DRAM that would select one CAS latency if it received a high voltage and a different CAS latency if it received a low voltage. (Jacob, Tr. 5386-87).

1188. This alternative would require additional wiring in the DIMM and from the DIMM to the memory controller. These additional wires can have a "noise glitch" – that is, the signals could be perturbed by adjacent signals – that would upset the CAS latency value and lead to improper operation of the DRAM. (Soderman, Tr. 9361-62).

1189. Certain configurations of SDRAMs had no "no-connect" pins. (CX 234 at 84; Geilhufe, Tr. 9741-42). Certain others had only a single "no-connect" pin. (RX 2100-13 at 1; Polzin, Tr. 4026-28).

1190. Moreover, pins designated as "no connect" are not necessarily available for other uses because they may be used in testing. (Soderman, Tr. 9463-65).

1191. Pins designated as "no connect" also may be unavailable because they are reserved for uses in other configurations. For example, if a manufacturer used the same mask for x4, x8 and x16 configurations, and if a pin designated "no connect" in the x4 and x8 configurations was used as a data pin in the x16 configuration, that pin could not be used for other purposes in the x4 and x8 configurations; in other words, the pin would need to remain a "no connect" pin in the x4 and x8 configurations. (Lee, Tr. 11084-87).

1192. Pins designated as "no connect" may also be valuable for use in future, higher density generations of the product. As Gordon Kelley of IBM testified, using up a pin is not something that was done "easily, because once you use that pin up for a function, you don't have it available to you in the future for generation advance. As the memory densities increase, we need pins for more addressing of more address locations and those pins are very valuable for that feature, so this would have limited the number of generations of DRAM design that we could have used if we were to use up this pin." (J. Kelly, Tr. 2552-53).

1193. To achieve the same level of flexibility as SDRAMs and DDR SDRAMs which have three bits in the mode register for storing a CAS latency value, a manufacturer would have to add three pins to a DRAM with no pins available. (Soderman, Tr. 9362; Geilhufe, Tr. 9589-90). Moreover, since the packages in use in the 1990's were all rectangular and required pins to be added in multiples of two, four pins would have to be added. (Soderman, Tr. 9362-63; Geilhufe, Tr. 9590).

1194. In its license negotiations with Rambus in 1994, Samsung was motivated to seek a non-assertion provision for non-Rambus-compatible uses of Rambus's inventions because of the on-chip DLL shown in Rambus's PCT application. (CX 2078 at 107-08 (Karp, Micron Dep.)).

1195. The number of pins required could not be reduced by having more than two voltage levels per pin. Although Professor Jacob has suggested that this could be done, he has never designed a circuit that would detect more than two voltage levels at high frequency. (Jacob, Tr. 11126). No SDRAM or DDR SDRAM parts support more than two voltage levels per pin in normal operation. (Jacob, Tr. 11125-26). Having more than two voltage levels on a pin would require sophisticated circuitry that would be easily perturbed by noise. (Soderman, Tr. 9363-64).

1196. The first Rambus DRAM, the 4.5 megabit part built by Toshiba in the early 1990's, had a pin with three voltage levels. (Horowitz, Tr. 8549). Rambus did not want to use an extra pin for entering test mode and, instead, created an extra voltage level on one of the existing pins for that purpose. (Horowitz, Tr. 8549). Although Rambus believed that the part had been built and designed with enough separation between the voltage levels to prevent confusion, in fact the part sometimes failed because it entered test mode accidentally. (Horowitz, Tr. 8550-51). Rambus never used a pin with more than two voltage levels on subsequent Rambus DRAMs. (Horowitz, Tr. 8551).

1197. Assuming a first-tier DRAM manufacturer and a product that is already well down the learning curve with a volume of twenty million unit volume, that is, a product that has already realized its cost improvement, programming CAS latency by using dedicated pins would have resulted in approximately four cents in increased packaging costs per unit, compared to the cost of SDRAMs in the mid-1990's, because of the need for additional four pins. (Geilhufe, Tr. 9562-64, 9589-91).

1198. The four cent increase cost estimate for this alternative is very conservative. First, standard packages generally add more than four pins – for example, the JEDEC SDRAM standards move from a 44-pin package to a 54-pin package, adding ten pins, and then to a 66-pin package, adding twelve pins. (Geilhufe, Tr. 9590; CX 234 at 99-106). Thus, if there were not enough pins available on a certain standard package, one might have to move up to the next standard package, adding many more than the bare minimum of four pins.

1199. Second, in addition to the four pins on the DRAM, more pins would also be required on the memory controller; however, every pin on controllers is fully utilized, so pins would have to be added there. (Soderman, Tr. 9363; Geilhufe, Tr. 9591).

1200. Third, both a new, more expensive connector may be required to connect the DIMM to the motherboard, and more lines on the bus. (Geilhufe, Tr. 9590-91).

e. Complaint Counsel Did Not Prove That Identifying CAS Latency in the Read Command Was a Viable Alternative

1201. Professor Jacob's proposed alternative of identifying CAS latency in the read command would involve a different command sent from the controller to the DRAM for each desired CAS latency. (Jacob, Tr. 5389).

1202. However, this alternative, upon a formal infringement analysis, might be determined to be covered by claim 1 of U.S. Patent No. 5,953,263, assigned to Rambus. (CX 1517 at 29).

1203. Professor Jacob testified that this alternative would not require a register because a "latch" could be used to store the latency information instead. (Jacob, Tr. 5393). This distinction is of no consequence because a register is a generic class of storage (Soderman, Tr. 9450-51), and one type of register is a latch. (Soderman, Tr. 9450-51; Horowitz, Tr. 8508-09).

1204. Professor Jacob concedes that "a register might be built out of latches." (Jacob, Tr. 5393). He testified that: "A latch is a specific implementation. A register implies how a piece of storage is being used." (Jacob, Tr. 5393).

1205. Identifying CAS latency in the command would have the negative side effect of limiting the simultaneous issuing of independent commands that is possible with the current command set. (Jacob, Tr. 5599).

1206. This alternative might also be covered by U.S. Patent No. 5,835,956, which is assigned to Samsung and was not considered by Professor Jacob. (RX 1308; Jacob, Tr. 5599-601). Claim 1 of that patent claims a synchronous memory device that

is capable of receiving latency mode information and selecting one of a plurality of latency modes in response to the information. (RX 1308 at 90).

f. Complaint Counsel Did Not Prove That Staying with Asynchronous Technology Was a Viable Alternative

1207. SDRAM, SLDRAM and RDRAM are all synchronous designs. (Jacob, Tr. 5601-02).

1208. Despite the success of SDRAM, a substantial amount of work on asynchronous technology has continued during the last decade at both the academic and commercial levels. (Jacob, Tr. 5602; Horowitz, Tr. 8560-61).

1209. When Dr. Horowitz began working on what was to become RDRAM, he had substantial experience in asynchronous designs. Some of Dr. Horowitz's Ph.D. students had done their dissertations in asynchronous design, and Dr. Horowitz had himself done studies comparing asynchronous to synchronous designs. (Horowitz, Tr. 8559).

1210. Dr. Horowitz decided that a synchronous design would be necessary for RDRAM because he did not believe that one could build a very high-performance asynchronous interface. (Horowitz, Tr. 8498). As a circuit designer, Dr. Horowitz realized that when a signal passes through a block of circuitry, the amount by which it is delayed is subject to some uncertainty because of fluctuations in certain parameters such as temperature and voltage. (Horowitz, Tr. 8499-00). In the absence of a timing reference, like the clock in a synchronous system, as the signal continues to travel through more and more blocks, the amount of uncertainty will grow so that it will not be possible to predict with any accuracy when data will arrive. (Horowitz, Tr. 9499-00). For high performance, the amount of uncertainty must be kept to a

small, predictable amount; this requires a synchronous system. (Horowitz, Tr. 8501-02).

1211. Asynchronous memories are very dependent on loading on the bus – that is, how many other chips are on the bus. In a general purpose environment, the loading of the bus can vary; consequently, asynchronous memories do not perform well in a bus environment at high frequencies. (Soderman, Tr. 9366).

1212. It was generally understood in the 1990's that asynchronous memories were not capable of reaching the speeds that would be required for future DRAMs. For example, an article by a Fujitsu engineer published in 1996 states that "[a]synchronous DRAMs, be that EDO or Burst EDO, can not keep up with bus speeds of over 66 MHz." (RX 2099-4 at 4). Jacquelyn Gross of Hewlett-Packard, formerly of Compaq, testified that it was Compaq's view in the 1996-1997 time frame that asynchronous technology was limited in the bandwidth it could achieve and that synchronous technology "provided higher benefits." (Gross, Tr. 2347). Steve Polzin of AMD testified that in the 1996-1997 time frame it was his opinion that, due to inherent limitations, asynchronous technology had less "headroom," that is less of an ability to offer improved performance over time, than synchronous technology. (Polzin, Tr. 4033-35).

1213. Burst EDO was an asynchronous type of DRAM that Micron was strongly pushing in the mid-1990's. (Williams, Tr. 822-23, 879). A 1995 Micron publication entitled "The Burst EDO DRAM Advantage" raises a question about the viability of Burst EDO ("BEDO") at bus speeds greater than 75 MHz and states that "BEDO will probably reach its limit somewhere around 100 MHz." (CX 2632 at 5).

1214. Burst EDO was standardized by JEDEC in March 1995. (Williams, Tr. 873, 879-80; RX 585 at 1). However, Burst EDO failed in the marketplace in competition with SDRAM. (Williams, Tr. 829).

2. Programmable Burst Length

1215. Complaint Counsel, through Professor Jacob, have suggested the following possible alternatives to programmable burst length in SDRAMs:

(1) Use fixed burst length parts;

(2) Program burst length by blowing fuses on the DRAM;

(3) Use dedicated pins to transmit burst length information from the controller to the DRAM;

(4) Explicitly identify burst length in the read command;

(5) Use a burst terminate command;

(6) Use a CAS pulse to control data output.

(Jacob, Tr. 5397-12).

a. Complaint Counsel Did Not Prove That the Use of Fixed Burst Length Parts Was a Viable Alternative

1216. Professor Jacob's proposed alternative of using fixed burst length parts, similar to his fixed CAS latency alternative, involves fixing the burst length of the DRAM during the design phase, manufacturing phase, or packaging phase. (*See* Jacob, Tr. 5373, 5397-98)

1217. Different burst lengths are required for different applications, so multiple fixed burst length parts would be required for this alternative. (Soderman, Tr. 9368-69). As Gordon

Kelley of IBM testified with respect to programmable burst length:

> The programmable feature allowing you to make that selection when the PC or the computer powered up was a nice feature because it allowed you to use devices that were common from multiple suppliers, put them into many different types of machines. Some of them would be a burst length of one, some would be a burst length of four, with the same part that was programmed at power-up. One of the advantages of that is that that drives low cost. The producer does not have to maintain multiple part numbers. One part number fits many applications. That's one of the drives to low cost.

(G. Kelley, Tr. 2550-51).

1218. The mode register in SDRAMs and DDR SDRAMs reserves three bits for burst length, allowing for up to eight different burst length values. (CX 234 at 150).

1219. Release 4 of JEDEC Standard 21-C (November 1993), which contains the first published SDRAM standard, provided specified two required burst length values (4 and 8) and three optional burst length values (1, 2, and full page). (JX 56 at 114). Release 9 of JEDEC Standard 21-C (August 1999), which contains the first published DDR SDRAM standard, specified three required burst length values for SDRAMs (2, 4, and 8) and two optional values (1 and full page); it also specified three required burst length values for DDR SDRAMs (2, 4, and 8). (CX 234 at 150).

1220. Burst lengths of one are used in graphics applications. (Lee, Tr. 11076).

1221. Micron sells SDRAMs that allow for five different burst lengths (1, 2, 4, 8 and full page). (RX 2100-13 at 1; Lee, Tr. 11078-80).

1222. Mark Kellogg of IBM noted that a disadvantage of fixing burst length in the manufacturing process would be that if a manufacturer did not have enough parts of the right burst length in stock, there could be a time lag of two weeks to one month before parts could be delivered. (Kellogg, Tr. 5119). Kellogg recommended to his company in 1992 that they support the programmable burst length feature because "[i]t offered us the greatest flexibility. We had a lot of applications." (Kellogg, Tr. 5132).

1223. A fixed burst length would have been "very, very bad for AMD." (Polzin, Tr. 3994). AMD designed processors to use a burst length of eight "for performance reasons," but because Intel processors use a burst length of four, fixing burst length would have meant that manufacturers would most likely produce burst length of four parts. (Polzin, Tr. 3994).

1224. JEDEC originally intended to fix the burst length at four in the DDR2 SDRAM standard. (Soderman, Tr. 9369; Macri, Tr. 4673-74). After further review by the DRAM manufacturers and the user community, it was determined that programmable burst length needed to be retained. (Soderman, Tr. 9369). DDR2 SDRAMs continue to have three bits in the mode register reserved for burst length, allowing for up to eight different burst length values. (RX 2099-14 at 21; Soderman, Tr. 9370). DDR2 SDRAMs currently require burst lengths of four and eight. (RX 2099-14 at 21; Soderman, Tr. 9369). This may change in the future; thus, the flexibility provided by the mode register is very important. (Soderman, Tr. 9370).

1225. There would have been an increase in design, photo tooling, and qualification costs because multiple products would

have had to be designed and manufactured rather than just one product. (Geilhufe, Tr. 9679, 9682-83, 9690).

1226. There would have been a decrease in testing costs due to the fact that each part would have had to be tested for a single burst length rather than multiple burst lengths. (Geilhufe, Tr. 9594).

1227. There would have been additional inventory cost due to four different burst lengths parts being manufactured, one less than the number of required and optional burst lengths in the original SDRAM standard, instead of a single programmable burst length part. (Geilhufe, Tr. 9595; JX 56 at 114). There would be an "economic disadvantage" from having multiple part numbers corresponding to different burst lengths. (Kellogg, Tr. 5119).

1228. The fixed burst length alternative would have resulted in the following approximate net costs compared to SDRAM in the mid-1990's, assuming a first-tier DRAM manufacturer and a product that is already well down the learning curve with a volume of twenty million unit volume, that is, a product that has already realized its cost improvement: $100,000 increase in product design costs per latency; $50,000 increase in photo tooling costs per latency; one cent decrease per unit in testing costs at wafer sort; three cents per unit increase in inventory costs; and $250,000 increase in qualification costs per latency. (Geilhufe, Tr. 9562-64, 9594-95).

1229. The net increase in variable costs for the fixed burst length alternative is, therefore, approximately two cents per unit. The total cost increase is approximately four cents per unit, calculated by converting the fixed costs to per unit costs through division by twenty million (the unit production run) and adding the resulting per unit fixed costs to the per unit variable costs. (Geilhufe, Tr. 9595-96).

1230. If both CAS latency and burst length were fixed, one would need to multiply the number of latencies by the number of burst lengths to calculate the total number of parts required. For example, if there were three latencies and four burst lengths, twelve parts would be required. (Geilhufe, Tr. 9601). Fixing both CAS latency and burst length would thus increase inventory costs by far more than the increase that would result from fixing CAS latency or burst length, but not both. (Geilhufe, Tr. 9601).

b. Complaint Counsel Did Not Prove That Programming Burst Length With Fuses Was a Viable Alternative

1231. Professor Jacob's proposed alternative of setting burst length with fuses is similar to his corresponding proposed alternative for programming CAS latency with fuses. (Jacob, Tr. 5403).

1232. Professor McAfee did not testify that this alternative was commercially viable. (McAfee, Tr. 7372).

1233. Once the fuse is blown, the DRAM becomes a fixed burst length part under this alternative. (Jacob, Tr. 5404; Soderman, Tr. 9370). As with fixing the CAS latency, having multiple fixed burst length parts would lead to logistical difficulties exacerbated by the fact that the fuse could not be blown by OEMs. (Soderman, Tr. 9370-71; Kellogg, Tr. 5142).

1234. There would have been an increase in design costs due to the design effort to provide the fuses required. (Geilhufe, Tr. 9575, 9584-85).

1235. There would have been increased inventory and qualification costs of the same magnitude as the corresponding costs for the fixed burst length alternative because, once the fuse is blown, the part would be a fixed burst length part. (Geilhufe, Tr. 9585-89).

1236. Setting burst length by blowing fuses would have resulted in the following approximate net costs compared to SDRAM in the mid-1990's, assuming a first-tier DRAM manufacturer using existing laser fuse technology and a product that is already well down the learning curve with a volume of twenty million unit volume, that is, a product that has already realized its cost improvement: $100,000 increase in product design costs per latency; three cents per unit increase in inventory costs; and $250,000 increase in qualification costs per latency. (Geilhufe, Tr. 9562-64, 9596-98).

1237. The net increase in variable costs for the alternative of setting burst length by blowing fuses is, therefore, approximately three cents per unit. The total cost increase is approximately five cents per unit calculated by converting the fixed costs to per unit costs through division by twenty million (the unit production run) and adding the resulting per unit fixed costs to the per unit variable costs. (Geilhufe, Tr. 9598).

1238. If the DRAM manufacturer did not have antifuse or electrically blown fuse technology available and wished to use that technology, adding it to the manufacturing process would entail several million dollars in development costs in addition to the costs above. (Geilhufe, Tr. 9583-84).

c. Complaint Counsel Did Not Prove That Using Dedicated Pins To Identify Burst Length Was a Viable Alternative

1239. Professor Jacob's proposed alternative of using an existing or a new dedicated pin to identify burst length is similar to his corresponding proposed alternative for using pins to identify CAS latency. (Jacob, Tr. 5405).

1240. As with the use of pins to set CAS latency, this alternative would lead to additional costs associated with adding

pins to the DRAM, wiring to the module and the motherboard, and adding pins to the controller. (Soderman, Tr. 9371).

1241. When asked about the advantages of using pins to set burst length, Gordon Kelley of IBM responded:

> I can't think of a lot of advantages compared to the programmable feature, which did not require a pin. I can think of the disadvantage that having a pin or using up a pin to do burst length selection was not a thing that we did easily, because once you use that pin up for a function, you don't have it available to you in the future for generation advance. As the memory densities increase, we need pins for more addressing of more address locations and those pins are very valuable for that feature, so this would have limited the number of generations of DRAM design that we could have used if we were to use up this pin.

(G. Kelley, Tr. 2552-53).

1242. Moreover, this alternative, upon a formal infringement analysis, might be determined to be covered by claim 1 of U.S. Patent No. 6,324,120, assigned to Rambus. (RX 2099-52 at 31-32; Soderman, Tr. 9371-72).

1243. Programming burst length by using dedicated pins would have resulted in the following approximate net costs compared to SDRAM in the mid-1990s, assuming a first-tier DRAM manufacturer and a product that is already well down the learning curve with a volume of twenty million unit volume, that is, a product that has already realized its cost improvement: 2 cents in increased packaging costs per unit due to an additional two pins. (Geilhufe, Tr. 9562-64, 9599).

1244. Although SDRAMs use three bits to program burst length, the cost calculation above involves the addition of only two pins based on the assumption that if pins were being used to set burst length, they would also be used to set CAS latency. (Geilhufe, Tr. 9599). Because pins have to be added in even increments, four pins were added to program CAS latency although only three were required. That extra pin, plus two additional pins, are sufficient to set burst length. (Geilhufe, Tr. 9599). If burst length were being set using pins, but not CAS latency, then an additional four pins would be required to achieve the same degree of flexibility as provided in the SDRAM standard. (Geilhufe, Tr. 9599-9600).

1245. As in the case of using dedicated pins for CAS latency, the estimated two cent increase cost for this alternative is very conservative. (Geilhufe, Tr. 9599).

d. Complaint Counsel Did Not Prove That Explicitly Identifying Burst Length in the Read Command Was a Viable Alternative

1246. Professor Jacob's proposed alternative of identifying burst length in the read command is similar to his corresponding proposed alternative for identify CAS latency in the read command. (Jacob, Tr. 5407).

1247. However, claim 1 of the '120 patent, reproduced above, upon a formal infringement analysis, might be determined to cover "receiving block size information" including when the block size (equivalently, burst length) information is embedded in a read command. (RX 2099-52 at 31-32; Soderman, Tr. 9373-74).

e. Complaint Counsel Did Not Prove That Using a Burst Terminate Command Was a Viable Alternative

1248. Professor Jacob's proposed alternative of using a burst terminate command rather than programming burst length through the mode register would involve defining all parts to have a fixed, long burst length and then sending a command to terminate the burst if a shorter burst length were desired. (Jacob, Tr. 5409).

1249. A burst terminate command is an optional feature in SDRAMs. (CX 234 at 161). The burst terminate command is required in DDR SDRAMs, but can be used only to terminate "read" bursts, not "write" bursts. (CX 234 at 174). Although DDR SDRAMs have this burst terminate command available, DDR SDRAMs program burst length in the mode register. (CX 234 at 150).

1250. A burst length of one would not have been possible with a burst terminate command because when a read command is issued it takes one cycle to execute before a burst terminate command could be encountered and, at that point, there are already two bits of data coming out. (Geilhufe, Tr. 9598-99).

1251. Professor Jacob's proposed alternative of using a burst terminate command would lead to inefficiencies on the bus. (Jacob, Tr. 5411). For example, terminating a read burst when the next command is a write leads to inefficient bus utilization because data already in the pipeline to be read out must be cleared before data can be written to the DRAM. (Soderman, Tr. 9374-76). Moreover, when the burst terminate command was on the bus, the controller would not be able to send a command to another bank. (Jacob, Tr. 11126).

1252. In fact, according to a study performed by Professor Jacob and a graduate student, this alternative could lead to a ten to

fifteen percent decrease in the efficiency of the system. (Jacob, Tr. 5604-06).

1253. JEDEC participants considered burst terminate an "internal device timing nightmare." (CX 415 at 10).

1254. Steve Polzin of AMD testified that use of a burst terminate command would interfere with pipelining and make the system less efficient overall. (Polzin, Tr. 4038-40).

1255. The JEDEC Future DRAM Task Group considered eliminating the burst terminate command, also known as burst interrupt, from DDR2 because at "high data rates burst interrupt commands are of less value, and are more difficult to engineer." (CX 392 at 5). The Task Group also noted that elimination of burst terminate would reduce test costs and increase yield due to elimination of speed critical path. (RX 2234 at 10).

1256. Although JEDEC retained some form of burst terminate in DDR2 SDRAM, the timing difficulties led JEDEC to limit its use. (Soderman, Tr. 9376-77). As Joe Macri, chairman of the JEDEC Future DRAM Task Group focusing on DDR2, testified:

> Well, SDRAM and DDR had a very general purpose interrupt. Essentially you could interrupt the DRAM anywhere. And that's difficult, you know, it's like in the middle of a sentence, getting interrupted, and it's just difficult to figure out where to stop. If you can only be interrupted at a particular place, in a very precise place and under precise conditions, then it makes it much easier to do the – the burst interrupt.

(Macri, Tr. at 4774 (*in camera*)). Thus, in the DDR2 standard, burst terminate can be used only to truncate a burst of eight to four, and it can be used only when reads are followed by reads or writes are followed by writes, not when a read is followed by a

write or a write is followed by a read. (RX 2099-39 at 63; Soderman, Tr. 9376-77). Despite including this limited form of a burst terminate command in the DDR2 standard, JEDEC also included the programmable burst length feature. (RX 2099-39 at 20).

f. Complaint Counsel Did Not Prove That Using CAS Pulse To Control Data Output Was a Viable Alternative

1257. Professor Jacob's proposed alternative of using a CAS pulse to control data output involves toggling the CAS line to the DRAM once for each bit of data desired – thus, if a burst of four were required, the CAS line would be toggled four times. (Jacob, Tr. 5411-12).

1258. This alternative would not work as Professor Jacob described it because it is not clear how the DRAM would be able to determine whether a signal on the CAS line were intended to be a "toggle" that was part of a burst of data or a new command. (Soderman, Tr. 9378-79). Sophisticated additional circuitry would have to be added to allow the DRAM to recognize the toggling of the CAS line, and that would add cost and create testing problems. (Soderman, Tr. 9379).

1259. In addition, this alternative would not allow efficient interleaving between banks without adding more CAS lines. (Soderman, Tr. 9379-80). Currently, while one bank of an SDRAM is reading out data, the CAS line can be used to send a command to a second bank, a process known as interleaving. Under the proposed CAS pulse alternative, the CAS line would be toggling in connection with the burst and additional CAS lines would have to be added to the other banks to enable this sort of operation. (Soderman, Tr. 9379-80). Because there are four banks on each DRAM, three CAS lines would have to be added requiring additional pins on the DRAM and the controller, as well

as additional circuitry on the DIMMs and the motherboard. (Soderman, Tr. 9380).

3. Given the Cost-Performance Differences, an Economically Rational DRAM Manufacturer Would Have Adopted and Licensed the Rambus Technologies Incorporated In SDRAM If It Had Known Of Rambus's Royalty Rates In Advance

1260. JEDEC-compliant SDRAM parts use two of the four Rambus technologies at issue: programmable CAS latency and programmable burst length. In order to determine whether the use of alternatives to the Rambus technologies used in SDRAM is more costly than paying the Rambus royalties, one can determine the additional variable costs associated with the alternatives and compare them to the Rambus royalties that would be paid under a license from Rambus. (Rapp, Tr. 9830-33). Costs for alternatives to different features are additive; that is, to calculate the costs associated with implementing alternatives to more than one feature simultaneously, one would simply add the costs associated with the individual alternatives. (Geilhufe, Tr. 9614).

1261. To make this comparison, the total additional cost of each alternative is divided by the weighted average of the selling price ("ASP") of SDRAM for the period 1996 to 2006. (Rapp, Tr. 9816-17, 9830-33). For SDRAM, the ASP is $4.87. (Rapp, Tr. 9816-17). This calculation shows the additional cost of the alternative as a percentage of selling price.

1262. The Rambus royalty rate for the use of its technologies in SDRAM is 0.75%. (Rapp, Tr. 9832).

1263. The alternatives for programmable CAS latency identified as "commercially viable" by Complaint Counsel's economic expert were: fixed CAS latency, explicitly identify latency in the read command, programming latency with fuses,

and using multiple pins to set a latency value. (Rapp, Tr. 9810-11; McAfee, Tr. 7354-63).

1264. The total additional incremental costs associated with the use of the fixed latency alternative is four cents per part. (Rapp, Tr. 9814). This total consists of the following additional incremental costs per part: a one cent wafer sort cost savings, a three cent good die yield cost increase, and a two cents inventory cost increase. (Rapp, Tr. 9814). As a percentage of ASP, this total additional incremental cost is 0.82%. (Rapp, Tr. 9817).

1265. The total additional incremental costs associated with the use of the alternative of explicitly identifying latency in the read command is one cent per part, which is the additional incremental costs associated with packaging. (Rapp, Tr. 9814-15). As a percentage of ASP, this total additional incremental cost is 0.21%. (Rapp, Tr. 9817).

1266. The total additional incremental cost associated with the use of the alternative of programming latency with fuses is six cents per part. (Rapp, Tr. 9815). This total consists of the following additional incremental costs per part: a one cent wafer sort cost increase, a three cents good die yield cost increase, and a two cents inventory cost increase. (Rapp, Tr. 9815). As a percentage of ASP, this total additional incremental cost is 1.23%. (Rapp, Tr. 9817-18).

1267. The total additional incremental costs associated with the use of the alternative of using multiple pins to set latency is four cents per part, which is the additional incremental costs associated with packaging. (Rapp, Tr. 9815). As a percentage of ASP, this total additional incremental cost is .82%. (Rapp, Tr. 9818).

1268. In addition to the additional incremental costs, each of the alternatives for programmable CAS latency either has performance disadvantages when compared to Rambus’s

technology or is potentially covered by Rambus's patents. (Rapp, Tr. 9819-23).

1269. The alternatives for programmable burst length identified as "commercially viable" by Complaint Counsel's economic expert were: fixed burst length, explicitly identify burst length in the read command, using a burst terminate command, and using multiple pins to set the burst length. (Rapp, Tr. 9810-11; McAfee, Tr. 7366-72).

1270. The total additional incremental costs associated with the use of the fixed burst length alternative is two cents per part. (Rapp, Tr. 9824-25). This total consists of the following additional incremental costs per part: a one cent wafer sort cost savings and a three cents inventory cost increase. (Rapp, Tr. 9825). As a percentage of ASP, this total additional incremental cost is 0.41%. (Rapp, Tr. 9825).

1271. The total additional incremental costs associated with the use of the alternative of explicitly identifying burst length in the read command is one cent per part, which is the additional incremental costs associated with packaging. (Rapp, Tr. 9825-26). As a percentage of ASP, this total additional incremental cost is 0.21%. (Rapp, Tr. 9826).

1272. There is no additional incremental cost associated with the use of the alternative of using a burst terminate command to set burst length. (Rapp, Tr. 9826). As discussed above, this alternative suffers from performance drawbacks.

1273. The total additional incremental costs associated with the use of the alternative of using multiple pins to set latency is two cents per part, which is the additional incremental costs associated with packaging. (Rapp, Tr. 9826). As a percentage of ASP, this total additional incremental cost is .41%. (Rapp, Tr. 9826).

1274. In addition to the additional incremental costs, each of the alternatives for programmable burst length either has performance disadvantages when compared to Rambus's technology or is potentially covered by Rambus's patents. (Rapp, Tr. 9828-30).

1275. The most costly alternatives to the two identified Rambus technologies that are used in JEDEC-compliant SDRAM that are not covered by Rambus's patents are the use of fuses to set latency and the use of fixed burst length. (Rapp, Tr. 9832). The total additional incremental cost of using these two alternatives is eight cents per part. (Rapp, Tr. 9832). As a percentage of ASP, this additional incremental cost is 1.64%, which exceeds the 0.75% Rambus royalty rate. (Rapp, Tr. 9832).

1276. The least costly alternatives to the two Rambus technologies that are used in JEDEC-compliant SDRAM that are not covered by Rambus's patents are the use of fixed CAS latency and the use of a burst terminate command to set burst length. (Rapp, Tr. 9831). The total additional cost of using these two alternatives is four cents per part. (Rapp, Tr. 9831-32). As a percentage of ASP, this additional incremental cost is 0.82%, which exceeds the 0.75% Rambus royalty rate. (Rapp, Tr. 9832).

1277. In order to determine what royalty a rational decision-maker would have expected Rambus to charge (in the absence of direct knowledge), the standard assumption and methodology in economics is to assume that the royalty rate actually charged is the best estimate of the royalty rate a decision-maker would have expected at an earlier time. (Rapp, Tr. 10207-09). Similarly, the standard assumption and methodology in economics is to assume that the actual weighted average selling price over the product life cycle is the best estimate of an ASP that a decision-maker would have predicted in advance. (Rapp, Tr. 10212-13). Using the standard assumptions and methodology in economics, a rational DRAM manufacturer or group of manufacturers would have

expected the additional costs of any alternatives to outweigh the costs of Rambus's royalties.

1278. Even without any reference to performance penalties, a rational manufacturer or group of manufacturers in JEDEC would have chosen to take a license from Rambus at 0.75% for SDRAM rather than use any combination of the alternatives identified by Complaint Counsel's economic expert as "commercially viable" that are not covered by Rambus's patents because all of those alternatives are more costly than licensing the Rambus technologies for SDRAM. (Rapp, Tr. 9833). Taking performance issues into account would have reinforced the decision to license rather than to substitute any of these alternatives because most of the alternatives have performance problems as well. (Rapp, Tr. 9833).

1279. Accordingly, a rational standard setting organization that knew that Rambus had patent interests on those two technologies but did not know precisely what Rambus's royalty rates would be to license the technologies would have selected the Rambus technologies. (Rapp, Tr. 9838-39). That is true even if the standard setting body were acting in a satisficing manner. (Rapp, Tr. 9839-40). If satisficing means that small cost differences are overlooked, then a satisficing standard setting body would be indifferent to the prospect of paying royalties; therefore, the theory of satisficing does not contribute to the analysis. (Rapp, Tr. 9839-40).

C. Complaint Counsel Did Not Prove That There Were Viable Alternatives To the Specified Rambus Technologies Adopted In DDR SDRAM

1. Dual-Edge Clocking

1280. Complaint Counsel, through Professor Jacob, have suggested the following possible alternatives to dual-edge clocking in DDR SDRAMs:

(1) Interleave on-chip banks;

(2) Interleave on-module ranks;

(3) Increase the number of pins on the DRAM;

(4) Increase the number of pins on the module;

(5) Double the clock frequency;

(6) Use simultaneous bidirectional input/output;

(7) Use toggle mode.

(Jacob, Tr. 5415-38).

a. Complaint Counsel Did Not Prove That Interleaving On-Chip Banks Was a Viable Alternative

1281. Professor Jacob's alternative of interleaving on-chip banks involves sending a clock signal to one bank on the DRAM and a second clock signal, a delayed version of the first, to another bank. (Jacob, Tr. 5419-20, 5614). Data would then be output or input on only a single edge of each clock signal, alternating between the two banks. (Jacob, Tr. 5419-20, 5614).

1282. Professor McAfee did not testify that interleaving on-chip banks was a commercially viable alternative. (McAfee, Tr. 7376-81).

1283. Efficient implementation of interleaving on-chip banks would still require dual-edge clocking and, therefore, is not an alternative. (Soderman, Tr. 9366). That is because the successive data signals from each bank should be given equal amounts of time on the bus. If one bank were given a shorter time window for

detection of data signals than the other, the data given the shorter time window might not be detected accurately; if, the data could be detected accurately in such a short time window, then it would be more efficient to restrict both banks to such a time window and run the bus at a faster speed. (Soderman, Tr. 9384-85). Also, a multiplexer would be used to select which bank is outputting data onto the bus at a given time. (Soderman, Tr. 9384). But the multiplexer must have a timing reference to tell it when to switch from one bank to the other. If one of the two clocks required by Professor Jacob's alternative is used for this reference, then data will be output onto the bus on both the rising and falling edge of this clock (since the falling edge of one of these clocks corresponds to the rising edge of the other); if, on the other hand, a third clock (not specified by Professor Jacob) is used to time the multiplexer, data would have to be output on the rising and falling edges of that clock. (Soderman, Tr. 9384-86).

1284. Even if interleaving on-chip banks did not require dual-edge clocking, it might still not be an alternative to Rambus's technology, because, upon a formal infringement analysis, it might be determined to be covered by U.S. Patent No. 5,915,105 (the '105 patent), assigned to Rambus. (RX 1472).

1285. Professor Jacob did not consider the '105 patent when he proposed interleaving on-chip banks as an alternative. (Jacob, Tr. 5615-16).

1286. Performance disadvantages of interleaving on-chip banks include significant increased power dissipation because of the power consumed by the additional clocks and the fact that two banks are being accessed alternately. Keeping both banks active doubles the number of precharge cycles, and the precharge operation may be the most power consuming part of the whole DRAM operation. (Soderman, Tr. 9387).

1287. There would have had to be a significant design effort for this alternative. (Geilhufe, Tr. 9602-03).

1288. There would have been a reduction in good die yield due to additional critical die area. (Geilhufe, Tr. 9603-04). So-called "redundancy technology" can be used to replace a defective part of the memory array on a DRAM, but the peripheral circuitry is "critical" in the sense that a defect in that circuitry will cause the unit to fail. (Geilhufe, Tr. 9603). The additional peripheral circuitry that would have been required to implement this alternative – such as multiplexing circuitry and timing circuitry – is critical in nature and defects in this circuitry would have reduced the good die yield. (Geilhufe, Tr. 9603-04).

1289. This alternative would have also complicated final testing and led to a slightly higher fall-out at that stage due to the necessity to activate two banks and to test the additional clocking circuitry. (Geilhufe, Tr. 9604).

1290. The alternative of interleaving on-chip banks would have resulted in the following approximate net costs compared to DDR SDRAM in the late 1990's, assuming a first-tier DRAM manufacturer and a product that is already well down the learning curve with a volume of twenty million unit volume, that is, a product that has already realized its cost improvement: $250,000 increase in product design costs; three cents per unit cost increase due to reduced good die yield; two cents per unit increase in final testing and good unit yield costs. (Geilhufe, Tr. 9562-64, 9602-04).

1291. The net increase in variable costs for the alternative of interleaving on-chip banks is, therefore, approximately five cents per unit. The total costs increase is approximately six cents per unit, calculated by converting the fixed costs to per unit costs through division by twenty million (the unit production run) and adding the resulting per unit fixed costs to the per unit variable costs. (Geilhufe, Tr. 9604-05).

b. Complaint Counsel Did Not Prove That Interleaving On-Module Ranks Was a Viable Alternative

1292. Professor Jacob's proposed alternative of interleaving banks on the DIMM or memory module is similar to his proposed alternative of interleaving on-chip banks except that data from different chips in a module, rather than data from different banks on the same chip, would be interleaved. (Jacob, Tr. 5426).

1293. Implementing this technology would require high speed bidirectional switches or multiplexers. (Soderman, Tr. 9389). Such bidirectional switches would require sophisticated engineering and would add appreciable cost. (Soderman, Tr. 9389). Moreover, additional hardware would be required to drive the switches. (Soderman, Tr. 9389).

1294. Professor Jacob testified that this alternative would have significant advantages and that the only disadvantage would be a slight complication of the memory module because of an extra clock line. (Jacob, Tr. 5427-28). Professor Jacob did not testify about any need for expensive high speed switches. (Jacob, Tr. 5427-28).

1295. Unlike most of Professor Jacob's proposed alternatives, his opinion about this alternative can be tested because a company, Kentron Technologies, Inc. ("Kentron"), has actually tried to implement the alternative of interleaving on module ranks. (Soderman, Tr. 9388).

1296. Kentron's "QBM" technology involves interleaving between chips on the module. (Goodman, Tr. 5997, 6002-03). Robert Goodman, Kentron's Chief Executive Officer, testified that the QBM technology requires the use of advanced switches. (Goodman, Tr. 6082).

1297. Each module would require eight switches at a dollar a piece in high-volume production, for a total of eight dollars per module. (Goodman, Tr. 6046-47, 6083). Additional circuitry, such as a PLL on the module is also required. (Goodman, Tr. 6048).

1298. Although Kentron now uses DDR SDRAM chips in its QBM technology, it initially called the technology "DBR" for "double bus rate" and used SDRAM chips. (CX 409 at 2). Kentron asserted that it could achieve the "same performance as 'DDR' using standard SDRAM single data rate." (CX 409 at 2).

1299. [redacted] (RX 1976 at 49 (*in camera*)).

1300. AMD's preliminary evaluation of the Kentron QBM technology concluded that it would have signal integrity problems. (Polzin, Tr. 4035-36).

1301. Kentron had no customers for its QBM technology. (Goodman, Tr. 6008).

1302. Interleaving on-module ranks suffers from additional disadvantages. First, it would lead to a less flexible memory increment: "[b]ecause high bandwidth is achieved by interleaving between DRAMs, twice as many DRAMs would be required on the DIMM to achieve the same bandwidth as is available using dual-edge clocking." (Soderman, Tr. 9389-90).

1303. Moreover, this alternative would not be available in all applications since many applications do not use modules at all but, rather, have the DRAM soldered directly onto the motherboard. (Soderman, Tr. 9390-91; Wagner, Tr. 3871-72).

1304. The alternative of interleaving on-module ranks would have resulted in the following approximate net costs compared to DDR SDRAM in the late 1990's, assuming a first-tier DRAM manufacturer and a product that is already well down the learning curve with a volume of twenty million unit volume, that is, a

product that has already realized its cost improvement: four dollars per module for multiplex and driver circuitry. (Geilhufe, Tr. 9562-64, 9605-06).

1305. This four dollar per module cost translates into a twenty-five cent per DRAM cost for DIMMs, which are memory modules containing 16 DRAMs each. (Geilhufe, Tr. 9606). This twenty-five cent increase is a variable cost.

c. Complaint Counsel Did Not Prove That Increasing the Number of Pins on the DRAM Was a Viable Alternative [*415]

1306. Professor Jacob's proposed alternative of increasing the number of pins per DRAM involves achieving high bandwidth by using only a single edge of a clock but doubling the number of data pins. (Jacob, Tr. 5429).

1307. Professor McAfee did not testify that increasing the number of pins on the DRAM is commercially viable. (McAfee, Tr. 7376-81).

1308. In addition to doubling the number of data pins, this alternative would require increasing the number of power and ground pins in order to support the added data pins. (Jacob, Tr. 5429-30). The number of pads and receivers on the DRAM would also have to be increased, leading to an increase in the size of the DRAM die and the size of the package. (Jacob, Tr. 5430-31).

1309. The additional data signals would toggle very fast and cause noise that could perturb the DRAM or other circuitry on the board. (Jacob, Tr. 5430-31).

1310. Tom Landgraf of Hewlett-Packard testified that his company was in favor of including dual-edged clocking in the DDR standard because of cost concerns. (Landgraf, Tr. 1709). Landgraf explained:

> In DDR, double data rate memory, you need – you're essentially transitioning data twice as fast as at a single data rate, and since memory systems tend to be very cost-competitive, one of our goals was to minimize the number of new pins we had to add to the next generation of memory. So, by using the double edged clock to transfer data, we were using the package and the pins more efficiently.

(Landgraf, Tr. 1709-10).

1311. The alternative of increasing the number of pins on the DRAM would be very expensive because of the number of additional pins required. (Soderman, Tr. 9391-92). For example, DRAMs with 16 data pins would have to have 16 additional data pins, plus additional power and ground pins. (Soderman, Tr. 9391-92). Moreover, the pins would need to be interconnected through the DIMM to the motherboard, increasing the cost of the whole system. (Soderman, Tr. 9392).

1312. There would have been additional product design costs because of the significant design effort associated with adding 16 input/output drivers and related multiplexing circuitry. (Geilhufe, Tr. 9607).

1313. There would have been a reduction in good die yield because of the considerable amount of critical die area added by the additional input/output circuitry. (Geilhufe, Tr. 9607).

1314. There would have been additional packaging costs associated with a more sophisticated and packaging technology known as a "ball grid array," which would have been required by the addition of 16 input/outputs. (Geilhufe, Tr. 9607-08).

1315. The alternative of increasing the number of pins on the DRAM, assuming that the data width would be doubled from 16 to 32, would have resulted in the following approximate net costs

compared to DDR SDRAM in the late 1990's, assuming a first-tier DRAM manufacturer and a product that is already well down the learning curve with a volume of twenty million unit volume, that is, a product that has already realized its cost improvement: $250,000 increase in product design costs; five cent per unit cost increase due to reduced good die yield; twenty-five cent per unit increase in packaging costs. (Geilhufe, Tr. 9562-64, 9607-08).

1316. The net increase in variable costs for the alternative of increasing the number of pins on the DRAM is, therefore, approximately thirty cents per unit. The total cost increase is approximately thirty-one cents per unit, calculated by converting the fixed costs to per unit costs through division by twenty million (the unit production run) and adding the resulting per unit fixed costs to the per unit variable costs. (Geilhufe, Tr. 9579).

d. Complaint Counsel Did Not Prove That Increasing the Number of Pins on the Module Was a Viable Alternative

1317. Professor Jacob's proposed alternative of increasing the number of pins per module would not change the single data rate DRAM at all but would achieve the desired bandwidth by adding data pins to the module. (Jacob, Tr. 5431).

1318. Professor McAfee testified that increasing the number of pins on the module is *not* commercially viable. (McAfee, Tr. 7378).

1319. This alternative would require 128 wires on the motherboard and 128 pins on the memory controller. (Jacob, Tr. 5432-33).

1320. This alternative would be expensive because of the extra pins and wires required. (Soderman, Tr. 9392-93).

1321. This alternative would not be available in all applications because many applications do not use modules at all but, rather, have the DRAM soldered directly onto the motherboard. (Soderman, Tr. 9390-91; Wagner, Tr 3871-72).

e. Complaint Counsel Did Not Prove That Doubling the Clock Frequency Was a Viable Alternative

1322. In Professor Jacob's proposed alternative of doubling the clock frequency, rather than using both the rising and falling edges of a clock, only a single edge of a clock running at twice the frequency would be used to achieve the same bandwidth. (Jacob, Tr. 5433-34).

1323. This alternative would require a clock signal that transitions at twice the rate of present systems and would, therefore, burn twice as much power as present systems. (Jacob, Tr. 5434-35).

1324. This alternative would cause clock distribution problems, because routing the clock signal through the DIMM to the various DRAMs is a critical task that becomes much more difficult at higher frequencies. (Soderman, Tr. 9393-94).

1325. This alternative would also lead to increased electromagnetic radiation from the higher frequency clock. (Soderman, Tr. 9395). Both DRAM manufacturers and systems companies are very careful about the amount of electromagnetic radiation generated because it can interfere with other circuitry and because there are strict FCC guidelines as to how much such radiation is permissible. (Soderman, Tr. 9395).

1326. At the time that JEDEC was considering using dual-edged clocking in DDR SDRAMs, the "predominant disadvantage" of using a higher frequency clock was "electromagnetic interference, radiation, the fact that fast pulses

tend to radiate. And we've constantly been concerned, and at that time was no different, about our ability to distribute very high-speed signals throughout a system." (Kellogg, Tr. 5182).

1327. In July 1997, Texas Instruments made a proposal involving a high speed single-edge clock. (CX 371 at 2-3; Lee, Tr. 6710-12). Terry Lee of Micron wrote the following in an email about the Texas Instruments proposal: "[a] single frequency clock is not practical. There is no real support yet for the higher frequency clock idea yet." (Lee, Tr. 11039, 11087-89).

1328. In September 2000, Micron proposed using a double frequency, single-edge clock in DDR2. (CX 2769 at 13; Lee, Tr. 6795-98).

1329. As late as November 2000, JEDEC was considering using a single data rate clock in DDR2. In an email dated November 29, 2000, Terry Lee of Micron circulated a summary of a conference call regarding "clocking issues" in DDR2. (CX 426). The conference call included representatives of ATI, Micron, Hewlett-Packard, IBM, Intel, Mitsubishi, AMD, Texas Instruments, and others. (CX 426 at 2-4). The summary of the conference call includes the following statement:

> Discussion on single data rate clock vs. doble [sic] data rate clock Fundamentally question is that is single data rate clock possible? Micron believes that SDR has some advantages as it gets ride [sic] of duty cycle issue, it has old prior art, and the inherent bandwidth is better with write than read . . . . In general, everyone agreed that SDR clock is ok provided that it works.

(CX 426 at 4).

1330. DDR2 SDRAMs use dual edge clocking. (RX 2099-14 at 3; RX 2099-39 at 5-6).

1331. There would have been additional design costs associated with additional circuitry required for the faster clock. (Geilhufe, Tr. 9608-9).

1332. There would have been additional final testing costs associated with testing involving a clock that is running at the speed of current technology. This would have been a significant step up in testing that would have required changes in the test equipment and would have lowered yield. (Geilhufe, Tr. 9609).

1333. To distribute a double frequency clock on the DIMM would have required an on-DIMM clock. (Geilhufe, Tr. 9609). At the required frequency, that clock would have cost approximately $3.80. Because the cost of a clock is a function of frequency, such a clock could cost as much as seven to eight dollars for the highest frequency parts and much less for lower frequencies. (Geilhufe, Tr. 9609-10).

1334. The alternative of doubling the clock frequency would have resulted in the following approximate net costs compared to DDR SDRAM in the late 1990's, assuming a first-tier DRAM manufacturer and a product that is already well down the learning curve with a volume of twenty million unit volume, that is, a product that has already realized its cost improvement: $100,000 increase in product design costs; four cent per unit cost increase due to higher speed final testing; $3.80 per module for an on-module clock. (Geilhufe, Tr. 9562-64, 9608-10).

1335. The net increase in variable costs for the alternative of doubling the clock frequency is approximately twenty-eight cents per unit, obtained by dividing the "per module" costs by sixteen corresponding to the number of DRAMs on a DIMM and adding this to the other variable costs. (Geilhufe, Tr. 9610). Since the increase in fixed costs is relatively small, the total cost increase, calculated by converting the fixed costs to per unit costs through division by twenty million (the unit production run) and adding

the resulting per unit fixed costs to the per unit variable costs, is also approximately twenty-eight cents per unit.

f. Complaint Counsel Did Not Prove That Using Simultaneous Bi-directional I/O Drivers Was a Viable Alternative

1336. Professor Jacob's proposed alternative of using simultaneous bi-directional input/output drivers involves a signaling scheme that allows read data and write data to exist on the bus simultaneously, potentially increasing bandwidth. (Jacob, Tr. 5435-36).

1337. Professor McAfee did not testify that simultaneous bi-directional I/O drivers was a commercially viable alternative. (McAfee, Tr. 7376-81).

1338. Simultaneous bi-directional input/output drivers involve a more complex driver design. (Jacob, Tr. 5437).

1339. This complex technology has been used in point-to-point systems in which there is only a single transmitter and receiver sending data back and forth and the time it takes to get from one to the other is known and built into the design parameters of the system. (Soderman, Tr. 9396-97). It would not work in a high-speed, bus-based system, such as used in general purpose computers, where there might be differing numbers of DRAMs connected to the bus and the components do not know precisely when signals being sent will arrive at other components. (Soderman, Tr. 9396-97).

1340. Even if this alternative could be made to work, the amount of additional bandwidth that would result from the ability to read from and write to the DRAM simultaneously would depend on the application and on whether the read and write operations are balanced. (Jacob, Tr. 5437). For most systems, which require a burst of data to be read from the DRAM prior to

writing to the DRAM and for which the read and write operations are thus not balanced, this alternative would not achieve the same high bandwidth as DDR SDRAMs. (Soderman, Tr. 9397-98). In the extreme case of an application that only read data from the DRAM but never wrote data to the DRAM, no benefit whatsoever would be obtained. (Soderman, Tr. 9397-98).

1341. Rambus has considered using simultaneous bi-directional input/output for high speed signaling. (Horowitz, Tr. 8563). Rambus did not use it, however, because Rambus could not implement it in a way that was not likely to cause errors. (Horowitz, Tr. 8563-64).

g. Complaint Counsel Did Not Prove That Using Toggle Mode Was a Viable Alternative

1342. By his proposed "toggle mode" alternative, Professor Jacob meant a DRAM like IBM's toggle mode DRAM. (Jacob, Tr. 5417).

1343. IBM's toggle mode DRAM was an asynchronous design. (Jacob, Tr. 5608; Soderman, Tr. 9398; Sussman, Tr. 1472). Asynchronous technology could not achieve the same performance in a general purpose, bus type architecture as could synchronous technology. (Soderman, Tr. 9398-99).

1344. An IBM researcher described IBM's toggle mode DRAM as "very big, very hot, and very nonstandard." (RX 2099-97 at 16; Soderman, Tr. 9399-00). The researcher went on to conclude that "in the commodity market, these attributes are disastrous." (RX 2099-97 at 16; Soderman, Tr. 9399-400).

1345. The toggle mode alternative would have required significant additional design costs. (Geilhufe, Tr. 9611).

1346. The good die yield would have been reduced due to additional critical die area. (Geilhufe, Tr. 9611).

1347. The toggle mode alternative would also have required an additional pin for the data toggle signal. Because pins must be added in pairs, two additional pins would have to be added. (Geilhufe, Tr. 9611).

1348. The toggle mode alternative would have resulted in the following approximate net costs compared to DDR SDRAM in the late 1990's, assuming a first-tier DRAM manufacturer and a product that is already well down the learning curve with a volume of twenty million units, that is, a product that has already realized its cost improvement: $250,000 increase in product design costs; ten cents cost increase per unit due to reduced good die yield; one cent cost increase per unit for an additional pin. (Geilhufe, Tr. 9562-64, 9610-11).

1349. The net increase in variable costs for the toggle mode alternative is, therefore, approximately twelve cents per unit. The total cost increase is approximately thirteen cents per unit, calculated by converting the fixed costs to per unit costs through division by twenty million (the unit production run) and adding the resulting per unit fixed costs to the per unit variable costs. (Geilhufe, Tr. 9611-12).

2. On-Chip DLL

1350. Complaint Counsel has suggested, through Professor Jacob, the following possible alternatives to on-chip DLL in DDR SDRAMs:

(1) Put a DLL on the memory controller;

(2) Put a DLL on the module;

(3) Use a vernier method;

(4) Increase the number of pins on the DRAM;

(5) Rely on the DQS data strobe for timing;

(6) Read clocks to avoid replicating DLL circuits on DRAM chips.

(Jacob, Tr. 5443-58).

1351. The purpose of the on-chip DLL in DDR SDRAMs is to compensate for internal delays on the DRAM and thereby to remove uncertainty in the timing of the system. (Jacob, Tr. 5442-43; Soderman, Tr. 9404).

1352. This timing uncertainty varies from DRAM to DRAM because of differences in process, temperature and voltage. (Soderman, Tr. 9402-03).

1353. The timing uncertainty compensated for by the DLL is more of a problem at high speeds because, as speeds increase, the window of time in which data is valid becomes smaller and the timing uncertainty reduces the size of the window even more. (Soderman, Tr. 9404-05).

1354. At high enough bus speeds, a DLL or PLL on the DRAM to compensate for individual timing uncertainties is required for correct operation. (Soderman, Tr. 9401-05).

1355. In the mid-1990s, DRAM engineers believed that a DLL or PLL on the DRAM would be necessary at future bus speeds. (RX 2099-29 at 1-4; RX 2099-13 at 1-7; Soderman, Tr. 9408-10).

1356. In a presentation on “Future SDRAM” at the March 1996 meeting of the JEDEC 42.3 subcommittee, Desi Rhoden presented a chart with columns representing clock speeds and rows representing certain features. (JX 31 at 64; Rhoden, Tr. 542-43). The chart indicates that “on-chip PLL/DLL” would be a “no”

at 100 MHz, "maybe" at 150 MHz, and "yes" at 200 MHz and above. (JX 31 at 64; Rhoden, Tr. 542-43). Indeed, Rhoden testified that: "We discussed [on-chip PLL/DLL] at length inside of JEDEC, and I don't think we ever had any question whether we would use the technology. It was just a question of when." (Rhoden, Tr. 546).

1357. In an email dated November 18, 1997, Bill Gervais of Transmeta wrote that "a DLL must be onchip and enabled for the Intel spec." (RX 1060 at 1). In other words, an on-chip DLL was required to meet Intel's timing requirements.

a. Complaint Counsel Did Not Prove That Putting a DLL On the Memory Controller Was a Viable Alternative

1358. Professor Jacob's proposed alternative of putting the DLL on the memory controller involves putting a DLL circuit on the memory controller rather than on each individual DRAM. (Jacob, Tr. 5445).

1359. This alternative is not sufficient for high speed performance because a DLL on the controller will broadcast the same delayed clock to all of the DRAMs and, therefore, cannot compensate for timing differences between DRAMs. (Soderman, Tr. 9405-06).

1360. Dr. Horowitz and other Rambus engineers have considered moving the DLLs off of the DRAMs and onto the memory controller on a number of occasions. (Horowitz, Tr. 8561-62). However, they determined that they were unable to meet the necessary timing requirements without a DLL on the DRAM. (Horowitz, Tr. 8561-62).

b. Complaint Counsel Did Not Prove That Putting a DLL On the Module Was a Viable Alternative

1361. Professor Jacob's proposed alternative of putting the DLL on the module involves putting an additional chip on the module containing either one or more DLL circuits rather than having a DLL on each individual DRAM. (Jacob, Tr. 5448-49).

1362. At high speeds, a single DLL would be insufficient and a separate DLL would be required for each DRAM on the module. (Jacob, Tr. 5449; Soderman, Tr. 9406-07).

1363. Professor Jacob's suggestion that multiple DLLs be put on a single chip would not solve the problem. A DLL on the DRAM could sense the DRAM's performance in order 430] circuitry on the DRAM to communicate with the DLL chip about the DRAMs performance. (Soderman, Tr. 9407). Such circuitry would be difficult and expensive to implement and would require extra traces on the module which would further increase the cost of the system. (Soderman, Tr. 9407-08).

1364. Tom Landgraf of Cisco, formerly at Hewlett-Packard, testified that Hewlett-Packard was in favor of including an on-chip PLL or DLL in the DDR SDRAM standard because putting a PLL on the motherboard or module instead would have led to lower performance at higher cost. Landgraf explained:

> One way to implement PLL is to put it on a – on the system, on the motherboard or on the memory module, and what we were suggesting, what we were in favor of doing was any time you can take a function which is on the motherboard that is common to a memory system, if you can incorporate that in the memory system itself, it reduces the overall cost of the system and also improves the performance of the system.

(Landgraf, Tr. 1709).

1365. The test time at wafer sort would have been decreased because the DLL on the DRAM would no longer have had to be tested. (Geilhufe, Tr. 9612-13).

1366. There would have been an increase in good die yield due to the decrease in critical die area resulting from removal of the DLL from the DRAM. (Geilhufe, Tr. 9613).

1367. The cost of an on-DIMM DLL is a function of the frequencies supported. For the DLL required for DDR SDRAMs, it would have cost approximately $3.80. (Geilhufe, Tr. 9613).

1368. The alternative of putting the DLL on the module would have resulted in the following approximate net costs compared to DDR SDRAM in the late 1990's, assuming a first-tier DRAM manufacturer and a product that is already well down the learning curve with a volume of twenty million units, that is, a product that has already realized its cost improvement: two cent cost decrease due to decreased test time at wafer sort; one cent cost decrease due to increased good die yield; $3.80 per module for an on-DIMM DLL. (Geilhufe, Tr. 9562-64, 9612-14).

1369. These costs would lead to an approximate twenty-one cent increase in the cost per unit, calculated by converting the fixed costs to per unit costs through division by twenty million (the unit production run), dividing the "per module" costs by sixteen corresponding to the number of DRAMs on a DIMM, and adding the resulting per unit fixed costs and per unit variable costs to the other variable costs. (Geilhufe, Tr. 9614). This twenty-one cent cost increase is a variable cost.

c. Complaint Counsel Did Not Prove That Using a Vernier Method To Account For Skew Was a Viable Alternative

1370. Professor Jacob proposed using a "vernier method" to "account for skew," that is timing uncertainties. (Jacob, Tr. 5444).

A "vernier" is a circuit that provides a static delay, that is, it is a variable delay circuit that does not contain a feedback loop like a DLL for changing the size of the delay. (Jacob, Tr. 5450; Soderman, Tr. 9411).

1371. Unlike a DLL, Professor Jacob's proposed alternative of using a vernier method to account for skew would not account for dynamic changes in skew caused by, for example, fluctuations in temperature or voltage without recalibration, that is adjustment of the amount of the delay, by the memory controller. (Jacob, Tr. 5452-53).

1372. These temperature and voltage changes can occur on the order of milliseconds and microseconds, respectively, and without the DLL's feedback loop the vernier will not be able to take these fluctuations into account and minimize the timing uncertainty. (Soderman, Tr. 9411-12).

1373. Moreover, the recalibration necessary to make the vernier more precise would consume bus bandwidth, because the recalibration information would have to be transmitted over the bus from the controller to the DRAM, and would make the system less efficient. (Soderman, Tr. 9412).

1374. The SyncLink consortium tried to design a chip, called an "SLDRAM," using verniers alone without PLLs or DLLs on the DRAM. (RX 2099-43 at 158; Soderman, Tr. 9412-14).

1375. Ultimately, however, SyncLink's SLDRAM chip did use a DLL in each DRAM, in addition to the vernier, in order "to make that timing a little bit more accurate." (Jacob, Tr. 5620-21; RX 2099-11; Soderman, Tr. 9414-15).

1376. In addition, the use of verniers, upon a formal infringement analysis, might be determined to be covered by U.S. Patent No. 6,115,318, "Clock Vernier Adjustment" assigned to Micron Technology (RX 1701), and as used in SLDRAM by U.S.

Patent No. 5,917,760, "Deskewing Data Signals in a Memory System," assigned to SLDRAM, Inc. (RX 1479).

1377. Professor Jacob did not consider these patents when he proposed the use of verniers as an alternative. (Jacob, Tr. 5622-23).

d. Complaint Counsel Did Not Prove That Increasing the Number of Pins on the DRAM Was a Viable Alternative

1378. Professor Jacob's proposed alternative of achieving high bandwidth using more DRAM pins and not clock frequency is the same as the alternative he proposed of using more pins per DRAM rather than using dual-edge clocking. (Jacob, Tr. 5453-54).

1379. This alternative suffers from the same infirmities and the same additional costs as the same alternative when it was proposed as an alternative for dual-edge clocking. (Geilhufe, Tr. 9612).

1380. Professor McAfee did not testify that increasing the number of pins on DRAM was a commercially viable alternative. (McAfee, Tr. 7385).

e. Complaint Counsel Did Not Prove That Relying on the DQS Data Strobe Was a Viable Alternative

1381. Professor Jacob's proposed alternative of relying on the DQS data strobe involves using the DQS signal that already exists in DDR SDRAMs to time the data which would no longer necessarily be aligned with the system clock. (Jacob, Tr. 5456-57).

1382. Using the DQS signal without the DLL is not sufficient for high speed performance. (Soderman, Tr. 9415-16).

1383. DDR SDRAMs already have the DQS signal available, but DDR SDRAMs also contain a DLL for accurate operation, even though DRAM manufacturers incur a cost to put the DLL on the DRAM. (Soderman, Tr. 9416-17).

1384. DDR2 SDRAMs have DQS data strobe signals as well as on-chip DLLs, even though DRAM manufacturers incur a cost to put the DLL on the DRAM. (*See* RX 2099-14 at 3; RX 2099-39 at 5, 7).

f. Complaint Counsel Did Not Prove That Read Clocks Were a Viable Alternative

1385. In the 1995-1998 time frame, JEDEC considered read clocks as an alternative to using DLL circuits in every DRAM. (Kellogg, Tr. 5159-60; Lee, Tr. 6663-65; JX 29 at 18-19).

1386. A read clock is less accurate than a strobe. (Kellogg, Tr. 5161). Since JEDEC could not rely on a strobe absent a DLL, it could not have relied on a read clock.

1387. Even Professor Jacob did not testify that a read clock was a viable alternative to on-chip DLL. (Jacob, Tr. 5444-45).

3. Given the Cost-Performance Differences, Economically Rational DRAM Manufacturers Would Have Adopted and Licensed the Rambus Technologies Incorporated in DDR and SDRAM

1388. JEDEC-compliant DDR parts use all four of the Rambus technologies at issue: programmable CAS latency, programmable burst length, dual-edge clocking, and on-chip PLL/DLL. In order to determine whether the use of alternatives to these Rambus technologies used in DDR is more costly than

paying the Rambus royalties, one can determine the additional incremental costs associated with the alternatives and compare those to the Rambus royalties that would be paid to Rambus under a license from Rambus. (Rapp, Tr. 9850-54). Costs for alternatives to different features are additive; that is, to calculate the costs associated with implementing alternatives to more than one feature simultaneously, one would simply add the costs associated with the individual alternatives. (Geilhufe, Tr. 9614).

1389. To make this comparison, the total additional incremental costs of alternatives are summed and divided by the weighted average of the actual and forecast average selling price ("ASP") of DDR for the period 2000 to 2006. (Rapp, Tr. 9844-45, 9850-54). For DDR, the ASP is $5.13. (Rapp, Tr. 9844-45).

1390. The Rambus royalty rate for the use of its technologies in DDR is 3.5%. (Rapp, Tr. 9853).

1391. The same additional incremental costs and performance disadvantages that apply to the alternatives to programmable CAS latency and programmable burst length as used in SDRAM also apply to the use of those alternatives in DDR. (Rapp, Tr. 9842-43).

1392. The alternatives for dual-edge clocking identified as "commercially viable" by Complaint Counsel's economic expert were: interleaving banks on the module, doubling the clock frequency, and the use of toggle mode. (Rapp, Tr. 9841; McAfee, Tr. 7380-81).

1393. The total additional incremental cost associated with the use of the alternative of interleaving banks on a module is twenty-five cents per part, which is the additional incremental cost associated with board complexity. (Rapp, Tr. 9844). As a percentage of ASP, this total additional incremental cost is 4.88%; which exceeds the 3.5% Rambus royalty rate. (Rapp, Tr. 9844-45).

1394. The total additional incremental cost associated with the use of the alternative of doubling the clock frequency is twenty-eight cents per part. (Rapp, Tr. 9845-46). This total consists of the following additional incremental costs per part: a four cents final test and good yield cost increase and a twenty-four cent circuit board area cost increase. (Rapp, Tr. 9845-46). As a percentage of ASP, this total additional incremental cost is 5.46%. (Rapp, Tr. 9846).

1395. These two technologies also have performance disadvantages when compared to Rambus's dual-edge clocking technology. (Rapp, Tr. 9846-48).

1396. The final alternative, toggle mode, is an asynchronous technology that is not technically viable. (Rapp, Tr. 9841, 9856-57).

1397. The alternatives for on-chip PLL/DLL identified as "commercially viable" by Complaint Counsel's economic expert are: the use of a vernier mechanism, placing the DLL on the module, and relying on the DQS data strobe. (Rapp, Tr. 9841-42). Each of these alternative has performance disadvantages when compared to Rambus's on-chip PLL/DLL technology. (Rapp, Tr. 9848-50).

1398. The most costly alternatives to the four specified Rambus technologies that are used in JEDEC-compliant DDR that are not covered by Rambus's patents are the use of fuses to set latency, the use of fixed burst length, any on-chip PLL/DLL alternative, and doubling the clock frequency. (Rapp, Tr. 9850-52). The total additional cost of using these four alternatives is thirty-six cents per part. (Rapp, Tr. 9852). As a percentage of ASP, this additional cost is 7.02%, which exceeds the 3.5% Rambus royalty rate by a substantial margin. (Rapp, Tr. 9853).

1399. The least costly alternatives to the four specified Rambus technologies that are used in JEDEC-compliant DDR that are not covered by Rambus's patents are the use of fixed latency, the use of a burst terminate command, any on-chip PLL/DLL alternative, and interleaving banks on a module. (Rapp, Tr. 9850-52). The total additional cost of using these four alternatives is twenty-nine cents per part. (Rapp, Tr. 9852). As a percentage of ASP, this additional cost is 5.65%, which exceeds the 3.5% Rambus royalty rate by a substantial margin. (Rapp, Tr. 9853).

1400. In order to determine what royalty a rational decision-maker would have expected Rambus to charge (in the absence of direct knowledge), the standard assumption and methodology in economics is to assume that the royalty rate actually charged is the best estimate of the royalty rate a decision-maker would have expected at an earlier time. (Rapp, Tr. 10207-09). Similarly, the standard assumption and methodology in economics is to assume that the actual weighted average selling price over the product life cycle is the best estimate of an ASP that a decision-maker would have predicted in advance. (Rapp, Tr. 10212-13). Using the standard assumptions and methodology in economics, a rational DRAM manufacturer or group of manufacturers would have expected the additional costs of any alternatives to outweigh the costs of Rambus's royalties.

1401. Based on these cost calculations and in consideration of the performance advantages of the four Rambus technologies incorporated in DDR, it is clear that Rambus's technologies were superior in cost-performance terms. (Rapp, Tr. 9857-58). A rational manufacturer or group of manufacturers in JEDEC would have chosen to take a license from Rambus at 3.5% for DDR rather than use any combination of the alternatives identified by Complaint Counsel's economic expert as "commercially viable." (Rapp, Tr. 9857-59).

1402. Although DRAM manufacturing costs decline over time, this does not affect the additional incremental costs used for

purposes of the calculations with regard to alternative technologies for either SDRAM or DDR because these costs were estimated for a mature product. (Rapp, Tr. 9854). Moreover, some of the estimated costs, such as inventory costs, are not subject to a decline over time because the decline in costs in the DRAM industry come from improvements in manufacturing technology and increased yields. (Rapp, Tr. 9854-55).

XII. EVEN ASSUMING THAT ALTERNATIVES DID EXIST, JEDEC WOULD NOT HAVE REJECTED THE RAMBUS TECHNOLOGIES

A. Whether JEDEC Would Have Adopted Alternatives To Rambus's SDRAM and DDR Technologies Had Rambus Made Additional Disclosures

1403. Rambus offered the testimony of Professor David Teece. Professor Teece has a Master's degree in economics from the University of Canterbury, a Master's degree in economics from the University of Pennsylvania, and a Ph.D. in economics from the University of Pennsylvania. (Teece, Tr. 10297). The subject of his Ph.D. Thesis was the resource costs of transferring technology between nations and amongst firms. (Teece, Tr. 10297). The thesis was published as a book, and two peer-reviewed articles came from it. (Teece, Tr. 10297). Professor Teece has written over one hundred fifty publications and over a dozen books. (Teece, Tr. 10298).

1404. Professor Teece is a chaired professor in the School of Business at the University of California at Berkeley. (Teece, Tr. 10295). He is also the Director of the Institute for Management, Innovation, and Organization at the University of California at Berkeley. (Teece, Tr. 10295). The Institute conducts research into questions of innovation, technology policy, and technology strategy. (Teece, Tr. 10295). The Institute has conducted a lengthy multi-country study of the global semiconductor industry. (Teece, Tr. 10295-96).

1405. Professor Teece has taught a number of courses over the years, including a Master's level course on management innovation and a Ph.D. seminar on technology strategy and related public policy issues. (Teece, Tr. 10296-97). In addition to teaching at Berkeley, Professor Teece has taught at the University of Pennsylvania, Stanford University, and Oxford University. (Teece, Tr. 10296).

1406. Professor Teece has received the first international prize in technology strategy and he has been named one of the fifty most important business thinkers of our time. (Teece, Tr. 10298-99).

1407. Professor Teece co-founded a journal entitled Industrial and Corporate Change, published by Oxford University Press, which focuses on technology management, technology policy, and the economics of innovation. (Teece, Tr. 10299). He has also referred several peer-reviewed journals. (Teece, Tr. 10299-300).

1408. Professor Teece's specialization within the field of industrial organization is in technology policy and particularly antitrust policy as it relates to high technology industries. (Teece, Tr. 10300). In the last fifteen to twenty years, he has written numerous articles on technology strategy and on the interface of technology policy and antitrust policy. (Teece, Tr. 10300).

1409. Professor Teece also has substantial expertise in the area of the economics of standard setting. He began to study the economics of standard setting organizations about a decade ago. (Teece, Tr. 10300-01). He was invited to speak twice at the joint FTC/DOJ hearings on the subject of standard setting and antitrust. (Teece, Tr. 10301).

1410. In contrast, Complaint Counsel's economic expert, Professor McAfee has not published a single paper on the issue of standard setting. (McAfee, Tr. 11345). He was not invited to

speak at the joint FTC/DOJ hearings. (McAfee, Tr. 11345). He has never been invited to speak on the issue of standard setting. (McAfee, Tr. 11345).

1411. The "but-for" world may be analyzed by the use of a decision tree, which is a device commonly used in economics to understand the different possible scenarios and outcomes in a "but-for" world. (Teece, Tr. 10315-16).

1412. In this case, the decision tree starts with the but-for world assumption that Rambus made the additional disclosures that Complaint Counsel allege Rambus should have made. (Teece, Tr. 10316).

1413. The decision tree may be described as follows. Had Rambus made these additional disclosures, JEDEC would have a choice; it could either proceed without seeking a RAND letter from Rambus, or it could ask Rambus to provide a RAND letter. (Teece, Tr. 10316). Had JEDEC proceeded without asking for a RAND letter, the same outcome would have occurred in the but-for world as in the actual world – JEDEC would have adopted standards incorporating Rambus's technologies. (Teece, Tr. 10329-30). If JEDEC had asked for a RAND letter, Rambus would have to decide whether to give a RAND letter. (Teece, Tr. 10317). If Rambus agreed to give a RAND letter, JEDEC members would (as a theoretical matter) have sought to negotiate licenses from Rambus before the standard was adopted and before any relevant patents issued (*ex ante*) or it could have proceeded without such negotiations. (Teece, Tr. 10317-18). If there were no *ex ante* negotiations, JEDEC could have adopted the standards incorporating Rambus's technologies or it could have adopted different standards. (Teece, Tr. 10319). Had JEDEC adopted the same standards as it actually adopted, the same outcome would have occurred in the but-for world as in the actual world. (Teece, Tr. 10319).

B. JEDEC Might Not Have Sought a RAND Assurance From Rambus Even if Rambus Had Made Disclosures

1414. As a matter of economic analysis, there are a number of considerations that suggest JEDEC might not have asked Rambus for a RAND letter, even if Rambus had made all of the disclosures described by Complaint Counsel.

1415. First, JEDEC might have perceived that Rambus was trying to derail the standard setting process by gaming the system. (Teece, Tr. 10320-22). That is, JEDEC might have believed that Rambus was asserting that it had patent rights in order to provoke JEDEC into seeking a RAND letter so that Rambus could refuse to give the letter and thereby stopping or slowing the standardization process. (Teece, Tr. 10320-22).

1416. Second, JEDEC might not have asked for a RAND letter because members might have believed that Rambus would not obtain patents that would cover products complying with the JEDEC standard. (Teece, Tr. 10323). For example, JEDEC members might have believed that Rambus's patent applications would not result in issued patents or that, if they did, the patents might not be valid because of prior art. (Teece, Tr. 10323).

1417. Third, JEDEC might not have asked for a RAND letter from Rambus because, in the real world, JEDEC did not seek, and to this day has not sought, a RAND assurance from Rambus regarding SDRAM, DDR or DDR2, despite JEDEC's knowledge of and concerns about Rambus's patent coverage. (Teece, Tr. 10323-27).

1418. JEDEC's failure to seek a RAND letter from Rambus is not explained by speculation that JEDEC *may* have chosen not to ask for a RAND letter – after Rambus began asserting its issued patents against DRAM manufacturers – because of litigation between Rambus and the DRAM manufacturers. (Teece, Tr. 10328-29). In the real world however, JEDEC sought a RAND

letter from Texas Instruments regarding the Quad-CAS technology even though TI was in litigation with Micron at the time. (Teece, Tr. 10329; CX 348 at 2, 4).

1419. Had Rambus made the additional disclosures that Complaint Counsel contend it should have made and had JEDEC not sought a RAND letter, economic analysis shows that JEDEC would have adopted the same standards that it did in the real world – the standards incorporating Rambus's technology. (Teece, Tr. 10329-30). Professor McAfee conceded this to be true; he testified that had JEDEC not sought a RAND letter, "it would lead to the same outcome as the actual world." (McAfee, Tr. 11308). In that event, the alleged failure to disclose had no anticompetitive effect. (Teece, Tr. 10320).

1420. Professor McAfee also admitted that if JEDEC was aware of patents that applied to SDRAM and not to previous generations of DRAM, and if JEDEC went forward with SDRAM without requesting a RAND letter, that would impact his assumption that JEDEC requires a RAND letter and therefore impact his opinions that rely on that assumption. (McAfee, Tr. 7708).

1421. There was, in addition, an example in the 1995-1996 time frame where a RAND letter was *not* requested by an EIA standards body, despite an assertion by an EIA member that it possessed a patent relating to the standard. In that case, an EIA member called Echelon gave notice to an EIA standards body, the Consumer Electronics Association ("CEA") that it had an issued patent that might cover a technology included in a CEA standards proposal. The EIA body chose not to ask for RAND assurances. (J. Kelly, Tr. 2122-23).

1422. Echelon was a participant in the standards setting process that had voted against the proposed standard. Echelon was promoting its own technology in competition with certain technology included in the standard. (J. Kelly, Tr. 2122).

1423. EIA General Counsel John Kelly was personally involved in the Echelon situation. He testified that RAND assurances were not sought from Echelon because "it appeared to us at the time . . . That Echelon was deliberately trying to impede the process, to stall it out for its own purposes . . . ." (J. Kelly, Tr. 2135).

1424. J. Kelly testified that after Echelon asserted that it had a patent related to the standard, it tried to insist that the EIA request a RAND assurance from it under the EIA Patent Policy. (J. Kelly, Tr. 2166-67).

1425. J. Kelly believed that Echelon was asserting its intellectual property claims, and insisting upon receiving a request for RAND assurances, in a bad faith effort to block the process of standardization. (J. Kelly, Tr. 2167). J. Kelly also believed that it was "reasonably clear" that "we weren't going to get those licensing assurances" from Echelon. (J. Kelly, Tr. 2166-67). J. Kelly believed that if a request for RAND assurances was made to Echelon, Echelon would refuse to give those assurances, and the standardization process would necessarily come to a stop. (J. Kelly, Tr. 2165-67).

1426. Dr. Gustavson expressed concern that standards could be blocked by a company asserting patent rights. (Gustavson, Tr. 9296; RX 675 at 1).

1427. Keith Weinstock, an Intel account representative from Micron, sent an email to Ryan, Lee and Walther stating that "Rambus plans legal action to request royalties on all DDR memory efforts." (RX 920 at 2).

1428. It appears that neither Ryan, Lee nor Walther, each of whom attended JEDEC meetings on behalf of Micron, ever notified JEDEC about the information they had learned regarding Rambus's plans. (Lee, Tr. 6972-73).

1429. Walther responded to the information in part by saying that he thought that "changing data on both edges of the clock" was "old technology." (RX 920 at 1).

1430. Lee testified that he ignored the information about Rambus's plans to request royalties on all DDR memory efforts because he did not "believe this was true." (Lee, Tr. 6981). Instead, he believed that Rambus was trying to spread "misinformation." (Lee, Tr. 6983). As Lee explained, his "thought process was that they were trying to get Intel locked into designing Rambus in on everything, direct RDRAM, and to try to tell [Intel] they had no other alternative, that they've eliminated all of their competition. . . ." (Lee, Tr. 6982-83).

1431. Lee testified that "it was consistent with [Rambus's] prior behavior that they might tell Intel, Oh, we have patents on that, so you can't use DDR there either," referring to a specific graphics memory application. (Lee, Tr. 6982-83).

1432. Professor McAfee testified that if JEDEC determines that the technology is not patented, JEDEC may proceed without requesting a RAND letter or RAND assurance even if someone asserts that the technology is covered by a valid patent as they did with Echelon. (McAfee, Tr. 7676-77).

1433. Professor McAfee further conceded that if, in the but for world in which Rambus made the additional disclosures that Complaint Counsel allege should have been made, JEDEC had determined that the Rambus technology it sought to include into a standard would not be patented, JEDEC might not have requested a RAND letter. (McAfee, Tr. 7678).

1434. Professor McAfee also admitted that he did not consider the possibility that had Rambus made the additional disclosures that Complaint Counsel allege should have been made, JEDEC might have proceeded to incorporate the technology without

requiring a RAND letter. (McAfee, Tr. 7680-81). Although Professor McAfee said in his rebuttal testimony that he did not think that there was a significant possibility that JEDEC would not have asked for a RAND letter (McAfee, Tr. 11308), he also testified that if JEDEC thought that it was being "gamed" by Rambus, and if JEDEC thought that Rambus was unlikely to obtain patent coverage, it was a "logical possibility" that JEDEC would not ask for a RAND letter and would proceed to incorporate in its standards the technologies at issue. (McAfee, Tr. 11331).

C. If JEDEC Had Sought a RAND Assurance, It Would Still Have Adopted Rambus's Technologies

1. Rambus Would Have Given a RAND Assurance

1435. A RAND letter must state that the patent holder will license its patent either royalty free or on reasonable terms and conditions that are demonstrably free of any unfair competition; in the latter case, the royalty rate is not specified in the letter. (Teece, Tr. 10331-32; JX 54 at 9-10). In this case, given Rambus's business model, an economist would not expect Rambus to agree to license its technology royalty free. (Teece, Tr. 10314, 10331-32; McAfee, Tr. 7492-93).

1436. A RAND assurance has three key provisions, each of which has economic implications for the patent holder. (Teece, Tr. 10333).

1437. The first provision is that the patent holder must make licenses available to all interested parties. (Teece, Tr. 10333). This provision means that the patent holder gives up the right to pick and choose to whom it will license. (Teece, Tr. 10334). There is a substantial economic motivation for a patent holder to agree to this provision. Agreeing to the provision makes it likely that firms will be willing to incorporate the patented technology because they are assured of not being frozen out. (Teece, Tr. 10334). The

patent holder is therefore likely to receive royalties that it otherwise would not receive. (Teece, Tr. 10334-35). Economic literature indicates that patent holders may be willing to agree to this type of restriction because doing so gives confidence to the licensees that they can use the patent holder's technology and be competitive in the marketplace. (Teece, Tr. 10335).

1438. The second provision of a RAND assurance is that the licensor agrees to license on reasonable terms and conditions. (Teece, Tr. 10336). This provision prevents the patent holder from charging unreasonable terms. (Teece, Tr. 10336). This commitment assures the licensees that royalties will not be unreasonable, again making them more likely to adopt the patentee's technology. (Teece, Tr. 10336). A patentee therefore has an economic incentive to agree to this provision. (Teece, Tr. 10337-38).

1439. In economic terms, reasonable terms and conditions means that the royalty rates are not so high as to negate the offer to license. (Teece, Tr. 10336-37). For example, if the rate is so high that it would put the licensee out of business, the rate is not reasonable. (Teece, Tr. 10337).

1440. The third provision of a RAND assurance is that the license be demonstrably free of any unfair discrimination. (Teece, Tr. 10338). This provision prevents arbitrary pricing differences among different licensees; it is designed to create a level playing field. (Teece, Tr. 10338). Again, this commitment is often attractive for a patent holder because it makes it more likely that licensees will adopt the patented technology, leading to royalties for the patentee. (Teece, Tr. 10338).

1441. From an economic perspective, licensees would be most concerned about the third provision - that licenses be demonstrably free of any unfair discrimination. (Teece, Tr. 10339). A level playing field is more important to firms than the

level of royalties because nondiscriminatory licenses mean that the firm is not competitively disadvantaged. (Teece, Tr. 10320).

1442. Economic analysis leads to the conclusion that if JEDEC had asked Rambus to provide a RAND letter, Rambus would have provided such a commitment. (Teece, Tr. 10340-41). First, in the but-for world in which Rambus makes the additional disclosures Complaint Counsel contends should have been made, Rambus would have already lost any benefits of keeping that information confidential. (Teece, Tr. 10344). Agreeing to give a RAND assurance at that point therefore involves less of a sacrifice. (Teece, Tr. 10344).

1443. Second, in Complaint Counsel's "but-for" world, where commercially feasible alternatives to Rambus's technologies exist, Rambus would have been confronted with the choice of giving a RAND letter and obtaining royalties or potentially seeing its technologies excluded from the standard and not receiving royalties. (Teece, Tr. 10344-45). Rambus never had to make that choice in the real world. Rambus is a pure-play licensing company. That is, Rambus does not manufacture DRAM, but rather uses research and development to invent new DRAM technologies and makes its money by licensing its technology to others. (Teece, Tr. 10350-51). If Rambus does not license, it goes out of business. (Teece, Tr. 10341). Rambus therefore has an economic incentive to agree to terms that make it possible for it to license its technology. (Teece, Tr. 10341). If it does not give a RAND assurance, it forces JEDEC to look at alternative technologies. (Teece, Tr. 10345). But given Rambus's business model, it does not want JEDEC to look at alternatives; it wants JEDEC to adopt its technologies so that it can obtain royalties. (Teece, Tr. 10345).

1444. This incentive is especially great if there are in fact alternatives to Rambus's technologies. (Teece, Tr. 10341-42). If there were good alternatives to Rambus's technologies, Rambus would clearly have given a RAND assurance because refusing to

do so would have cost it the opportunity to get significant revenue from licensing. (Teece, Tr. 10343). In that situation, it would have been economically irrational for Rambus to refuse to give a RAND letter. (Teece, Tr. 10345).

1445. This conclusion is consistent with the views of Professor McAfee. First, McAfee admitted that his starting point would be that whatever information was known to JEDEC about alternative would be known to Rambus. (McAfee, Tr. 7729). Second, he admitted that one of the risks that Rambus would face if it chose not to give a RAND letter in the but-for world would have been that JEDEC would adopt a non-infringing alternative. (McAfee, Tr. 7729).

1446. The conclusion that Rambus would have given a RAND letter is not affected by speculation that Rambus might have gained some marketplace benefit for RDRAM by refusing to give a RAND assurance. (Teece, Tr. 10345-46). Especially if there were alternatives to Rambus's technologies, any benefit to Rambus's goal of increasing the acceptance and sales of RDRAM that might flow from a refusal to give a RAND assurance for SDRAM and/or DDR would be minimal or nonexistent. (Teece, Tr. 10346). Moreover, giving a RAND assurance would lead to royalties in hand for Rambus rather than a mere potential benefit to RDRAM. (Teece, Tr. 10739-40).

1447. Finally, the conclusion that Rambus would have issued a RAND letter if asked is bolstered by the fact that the DRAM industry exhibits fairly rapid technological change. (Teece, Tr. 10346-47). Rambus is a "repeat player"; that is, its business model is such that it will often be engaging in licensing in the DRAM industry as it develops new technologies. (Teece, Tr. 10346-47). Rambus therefore has an incentive to behave in a reasonable and cooperative manner because it is building an ongoing technology company (Teece, Tr. 10347), and it therefore has incentive to give a RAND letter because it wants to build

relationships with the licensees for the future. (Teece, Tr. 10740-41).

1448. Evidence that Rambus was concerned about agreeing to a RAND policy does not change this conclusion. First, in the but-for world, unlike the real world, Rambus has already disclosed its trade secrets. (Teece, Tr. 10716).

1449. Second, evidence that Rambus might have been reluctant in the actual world to give a RAND letter is affected by the fact that Rambus had apparently misunderstood what a JEDEC RAND assurance required. Had Rambus been confronted with a request from JEDEC to provide a RAND letter, it would have had an incentive to seek to determine what that commitment entailed. (Teece, Tr. 10716-17).

1450. This fact is supported by Rambus's conduct in December 1995 – just before Rambus left JEDEC – when Rambus was considering proposing the R-Module technology for standardization at JEDEC. Because Rambus realized that proposing a technology at JEDEC might require it to agree to license on RAND terms, Richard Crisp made inquiries about what RAND entailed. (Crisp, Tr. 3479-82). When he did so, Crisp learned from Sussman that "reasonable" terms and conditions meant "almost anything we wanted it to mean." (Crisp, Tr. 3480-81; CX 711 at 188). After learning this, Crisp wrote an email to others at Rambus explaining, "So the conclusion I reach here is that we can abide by the patent policy on a case-by-case basis, are free to set the terms of our license arrangements to what we like (as long as we agree to license all-comers to build our modules), and we give up nothing else in the process." (CX 711 at 188; Crisp, Tr. 3483). He then concluded that with regard to RAND, the JEDEC policy was not "nearly as onerous as some of us had earlier believed." (CX 711 at 188; Crisp, Tr. 3483).

1451. In contrast to this analysis, Complaint Counsel's economic expert admitted that he was unable to determine

whether or not Rambus would have given a RAND letter in the but-for world (McAfee, Tr. 7730, 11333), and he admitted that he could not say "one way or the other" if it would have been in Rambus's economic interest to issue a RAND letter in the but-for world. (McAfee, Tr. 7733).

2. It is Unlikely There Would Have Been Any Ex Ante Negotiations

1452. Professor McAfee testified that once Rambus issued a RAND letter, JEDEC members would have an "incentive" to engage in ex ante negotiations, i.e., to negotiate with Rambus prior to the adoption of Rambus's technologies into the SDRAM and DDR standards. (McAfee, Tr. 7493-94). Professor McAfee testified that if one firm engaged in *ex ante* negotiations with Rambus, that firm would "report" the royalty rates back to other JEDEC members. (McAfee, Tr. 7494). This analysis, however, is flawed. Firms have incentives to do lots of things that they do not actually do; a proper analysis must take into account all the pertinent factors, including those that would have prevented JEDEC members from asking for any incentive to negotiate *ex ante*. (Teece, Tr. 10353-54). Moreover, any such licensing negotiations would be done under confidentiality agreements (Teece, Tr. 10352-53), and companies would, or should, avoid such an exchange of pricing information because of antitrust concerns.

1453. There is also no evidence of *ex ante* negotiations for naked licenses for patent applications outside of the DRAM industry. (Teece, Tr. 10354). Professor Teece, who has studied licensing for over twenty years, did not know of a single example of a negotiation of a naked license for a patent application. (Teece, Tr. 10356, 10360).

1454. There are several economic reasons for the absence of negotiations before patents issue. First, because patent applications are a bundle of rights that has not matured, the parties

do not know for what they are bargaining. (Teece, Tr. 10357). Patent applications often change during the course of prosecution – claims get amended, claims get withdrawn, claims are abandoned – and it is not clear what claims will ultimately issue. (Teece, Tr. 10357-59). There is therefore great uncertainty about the rights that would be negotiated before a patent issues. (Teece, Tr. 10357).

1455. Because of the uncertainty about what, if any, claims in an application will issue, negotiations before patents issue are extraordinarily complex and costly, and in the real world, firms do not engage in this type of negotiations with any frequency. (Teece, Tr. 10357).

1456. Moreover, *ex ante* negotiations for a license regarding patent applications involve confidentiality concerns – the negotiations may be an avenue for the parties to discover each other's intellectual property strategies or information about future inventions. (Teece, Tr. 10359). This might provide a disincentive to *ex ante* negotiations of this sort. (Teece, Tr. 10358-59).

1457. Finally, *ex ante* negotiations for a naked license involving patent applications may require claim contingent licensing – agreements on different royalty rates depending on which claims in the application issue – which adds to the complexity and costs. (Teece, Tr. 10359).

1458. The fact that Rambus entered into licenses for RDRAM does not undermine this conclusion. The licenses for RDRAM were not naked patent licenses (licenses that do not include rights other than a right to use the intellectual property). (*See, e.g.*, CX 1592 at 19-21; Teece, Tr. 10355-56).

1459. Because of these costs and disincentives, *ex ante* negotiations for a naked license involving patent applications usually do not take place either inside or outside the DRAM industry. (Teece, Tr. 10354-60).

1460. Professor McAfee agreed that *ex ante* negotiations are less likely with respect to a patent application than an issued patent. (McAfee, Tr. 11335). He also agreed that the less certainty there is about the exact scope of a claim and whether or not it would issue, the lower the probability of *ex ante* negotiations. (McAfee, Tr. 11336).

1461. Professor McAfee also admitted that if the potential licensee believed that the pending claims would be invalid or would not issue, it would be less likely to engage in *ex ante* negotiations. (McAfee, Tr. 11336).

1462. Moreover, according to Professor McAfee, the likelihood of *ex ante* negotiations would be less if Rambus did not have pending claims that actually covered the relevant technologies at the time it gave the RAND letter because, "[i]f nothing else, it makes it harder to describe precisely what is being negotiated about." (McAfee, Tr. 11334-35).

1463. In the but-for world, JEDEC members and Rambus would most likely have recognized the costs of negotiating a license regarding patent applications as opposed to issued patents. (Teece, Tr. 10396). Complaint Counsel's economic expert agreed in part, that JEDEC members might rationally conclude that the costs of *ex ante* negotiations exceed the costs of waiting to negotiate *ex post*. (McAfee, Tr. 11337).

3. JEDEC Would Have Adopted Rambus's Technologies with Rambus's RAND Assurance

1464. Assuming that Rambus would have given a RAND assurance if asked, there are a number of reasons why JEDEC would have adopted the Rambus technologies. First, the alternatives were inferior, even when taking into account Rambus's royalties. (Teece, Tr. 10363, 10365; *see* F. 1128-1402, *supra*).

1465. Second, the theory of revealed preference shows that JEDEC preferred Rambus's technologies. (Teece, Tr. 10365-66; *infra* F. 1486-1518). These two points are sufficient to show that JEDEC would have adopted Rambus's technologies for both SDRAM and DDR. (Teece, Tr. 10366).

1466. Third, JEDEC has demonstrated a willingness to adopt patented technologies, and it would likely do the same thing with Rambus's technologies. (Teece, Tr. 10371-72).

1467. JEDEC has previously adopted patented technologies where it received a RAND letter. Gordon Kelley, a long time chair of JC 42.3 testified that he could not recall any instance in which JEDEC pursued alternatives after receiving a RAND commitment on what the committee thought was the best alternative. (G. Kelley, Tr. 2707-09). By contrast, he did recall some instances in which all consideration of alternatives was dropped as soon as a RAND assurance was received. (G. Kelley, Tr. 2707-09).

1468. During the period when Rambus attended JEDEC, Desi Rhoden could not recall any example of a JEDEC committee trying to find an alternative technology after a JEDEC member disclosed a patent application that in someway related to the technology being standardized and stated that it would license on RAND terms. (Rhoden, Tr. 628-29).

1469. At the May 1990 meeting, JC 42.3 sent a ballot to Council to standardize the 256K x4 MPDRAM technology (JC-42.3-89-48) after receiving a RAND assurance from Digital Equipment Corporation. The minutes state, "This ballot passed but was on hold concerning the patent issue. A patent release letter . . . was circulated during the meeting resolving that issue. The ballot will now go to Council." (JX 1 at 6). The "patent release letter" indicated that Digital Equipment Corporation was

willing to license the relevant patent for a one percent royalty on sales. (JX 1 at 24).

1470. At the December 1991 JC 42.3 meeting, Siemens disclosed at the time of balloting that it had an issued patent that may cover Extended Data Out for MPDRAM (JC-42.3-91-157). (JX 10 at 9). The committee responded that it was aware of prior art on this patent and unanimously moved to send the ballot to Council assuming the patent issue could be resolved. (JX 10 at 9).

1471. At the July 1992 JC 42.3 meeting, the committee considered a ballot for 2M x8/x9 Sync DRAM in TSOP II (JC 42.3-92-83). (JX 13 at 9). At the meeting, Motorola disclosed an issued patent and provided a letter assuring that Motorola would license the patent on a nondiscriminatory basis for a reasonable fee. (JX 13 at 9, 136). The committee agreed that the letter met the EIA requirements, and the committee voted to pass the ballot. (JX 13 at 9-10). The item was given Council ballot number 93-13. (JX 16 at 38). At the May 1993 JEDEC Council meeting, the Council passed the ballot and standardized the technology. (CX 54 at 8).

1472. At the March 1993 JC 42.3 meeting, the committee voted to pass a ballot on Mode Register Timing (JC-42.3-92-129-1A) for the SDRAM draft specification even though Hitachi commented "patent alert." (JX 15 at 5). At that meeting, the committee voted unanimously to send all SDRAM ballots to JEDEC Council for standardization. (JX 15 at 14). The item was given Council ballot number 93-19. (JX 16 at 39). At the May 1993 JEDEC Council meeting, the Council passed the ballot to standardize this technology. (CX 54 at 9).

1473. At the March 1993 JC 42.3 meeting, the committee considered a ballot for Write Latency (JC-42.3-92-130A) for the SDRAM draft specification. With regard to this ballot, the minutes state that Mosaid raised a patent issue. (JX 15 at 5-6). The committee voted unanimously to pass this ballot. (JX 15 at 6).

At that meeting, the committee voted unanimously to send all SDRAM ballots to JEDEC Council for standardization. (JX 15 at 14). The item was given Council ballot number 93-20. (JX 16 at 38). At the May 1993 JEDEC Council meeting, the Council passed the ballot to standardize this technology. (CX 54 at 9).

1474. At the March 1993 JC 42.3 meeting, the committee considered a ballot for Self-Refresh Entry/Exit (JC-42.3-92-133A) for the SDRAM draft specification. (JX 15 at 8). The minutes state that both Hitachi and Mosaid raised a "patent alert." (JX 15 at 8). The committee voted unanimously to pass this ballot. (JX 15 at 8). At that meeting, the committee voted unanimously to send all SDRAM ballots to JEDEC Council for standardization. (JX 15 at 14). At the May 1993 JEDEC Council meeting, the Council passed the ballot to standardize this technology. (CX 54 at 10).

1475. At the March 1993 JC 42.3 meeting, the committee considered a ballot for Auto-Refresh (JC-42.3-92-134A) for the SDRAM draft specification. (JX 15 at 8). The minutes state that both Hitachi and Mosaid raised a patent issue. (JX 15 at 8). The committee voted unanimously to pass this ballot. (JX 15 at 9). At that meeting, the committee voted unanimously to send all SDRAM ballots to JEDEC Council for standardization. (JX 15 at 14). The item was given Council ballot number 93-24. (JX 16 at 38). At the May 1993 JEDEC Council meeting, the Council passed the ballot to standardize this technology. (CX 54 at 10).

1476. At the March 1993 JC 42.3 meeting, the committee considered a ballot for DQM Latency Reads/Writes (JC-42.3-92-136A) for the SDRAM draft specification. (JX 15 at 9). The minutes state that both Hitachi and Mosaid raised a "patent concern." (JX 15 at 9). The committee voted unanimously to pass this ballot. (JX 15 at 9). At that meeting, the committee voted unanimously to send all SDRAM ballots to JEDEC Council for standardization. (JX 15 at 14). This item was given Council ballot number 93-26. (JX 16 at 38). At the May 1993 JEDEC Council

meeting, the Council passed the ballot to standardize this technology. (CX 54 at 10).

1477. At the March 1994 JC 42.3 meeting, the committee considered a ballot for SGRAM and SVRAM Special Mode (JC-42.3-94-15). (JX 19 at 12). Micron voted against the ballot, citing three issued patents held by Texas Instruments that could cover the technology. (JX 19 at 12). Texas Instruments said they saw "no need to comment." (JX 19 at 12). The committee passed the ballot unanimously on the motion by Hitachi to "send it [to] Council providing TI gives some assurance on the patent. (JX 19 at 12).

1478. At the March 1995 JC 42.3 meeting, the committee considered ballot JC-42.3-95-14 Item 637. (JX 25 at 2). TI raised patent concerns. (JX 25 at 2). The committee nonetheless passed a motion to send the ballot to JEDEC Council. (JX 25 at 2).

1479. At the September 1995 JC 42.3 meeting, the committee considered a ballot for 4M/8M x8 DRAM in 32-pin SOP Item 660 (JC-42.3-65-109). (JX 27 at 7). The minutes state, "The Stacktek patent was discussed. Motion by HP to pass to Council the ballot conditionally on resolution of Stacktek's patent position. . . . Unanimous." (JX 27 at 8). The Council later passed this ballot. (JX 34 at 18).

1480. JEDEC's behavior, as exhibited in the JEDEC 42.3 meeting minutes, shows that JEDEC repeatedly adopted technologies despite patent issues, especially after receiving a RAND letter. In accordance with this behavior, had Rambus provided a RAND assurance, JEDEC most likely would have adopted the Rambus technologies. (Teece, Tr. 10379-80, 10382-84).

1481. EIA General Counsel, John Kelly, agreed that there is no objection to having features and standards that are protected by

valid patents as long as they are available to all comers on reasonable and nondiscriminatory terms. (J. Kelly, Tr. 2072).

1482. The chair of JC 42.3 admitted that if Rambus had agreed to give a RAND assurance, "I would have had to consider accepting their intellectual property." (G. Kelley, Tr. 2564-66).

1483. Even if alternatives were "price constraining" with respect to Rambus's technologies, they could not have been chosen by JEDEC. (Teece, Tr. 10366-67). A technology that is price constraining is not the same as an economic substitute. (Teece, Tr. 10370-71). An economic substitute must be equivalent in terms of cost-performance features. (Teece, Tr. 10371).

1484. Technologies that are not equivalent may still be price constraining, but that does not make them a viable alternative for JEDEC. (Teece, Tr. 10371). What is important to compare is the overall attractiveness of the alternatives on a quality/cost-adjusted basis. (Teece, Tr. 10976-97).

1485. The conclusion that JEDEC would have adopted Rambus's technologies in SDRAM and DDR once it received a RAND assurance from Rambus is not undermined by the possibility that JEDEC might have been "satisficing." (Teece, Tr. 10414-15). If JEDEC had avoided patented technologies in favor of alternative technologies without a lot of analysis, it would not have been satisficing; such conduct is merely biased behavior. (Teece, Tr. 10414). If JEDEC were satisficing, it would be willing to go forward with patented technology upon the receipt of a RAND letter. (Teece, Tr. 10414-15).

XIII. ANALYSIS OF THE BUT/FOR WORLD HYPOTHESIS

A. The Revealed Preference Theory – JEDEC Continued To Select Rambus Technologies Even While Rambus Was Asserting Its Patent Rights

1486. The economic theory of revealed preference posits that one should not look to what people say but, at what they actually do. (Teece, Tr. 10366).

1487. In simple terms, the theory of revealed preference is that one draws inferences about people's preferences by observing their choices. (Rapp, Tr. 9804).

1488. According to the theory of revealed preference, the choices of JEDEC and DRAM manufacturers to use the Rambus technologies when there were opportunities to use other technologies, shows that the Rambus technologies were superior to any alternatives in cost-performance terms. (Rapp, Tr. 9803-05).

1489. For SDRAM, JEDEC selected two Rambus technologies – programmable CAS latency and programmable burst length – over all available alternatives. As Gordon Kelley testified, JEDEC considered the available technologies and selected what was considered to be the best. (G. Kelley, Tr. 2707-09).

1490. Instead of Rambus's programmable CAS latency technology, JEDEC considered for the SDRAM standard, the alternatives of fixed latency and the use of fuses to set the latency. (Kellogg, Tr. 5136). With regard to Rambus's programmable burst length technology, JEDEC considered the alternatives of fixed burst length, the use of pins to set the burst length, and the use of fuses to set the burst length. (Kellogg, Tr. 5111-12).

1491. In the place of Rambus's dual-edge clocking technology, for the DDR standard, JEDEC considered increasing the speed of the clock and interleaving banks on a module. (Kellogg, Tr. 5178). Instead of Rambus's on-chip PLL/DLL technology, JEDEC considered using verniers and relying only on data strobes. (Kellogg, Tr. 5156).

1492. The development of the DDR2 standard began in April 1998. (Macri, Tr. 4598). From that date through June 2000, JEDEC specified many of the architectural attributes for DDR2. (Macri, Tr. 4598-99).

1493. The April 1998 meeting minutes of the Future DRAM Task Group (the JEDEC subcommittee that developed DDR2) reveal that JEDEC considered entirely different architectures for the next generation DRAM, including architectures based on SLDRAM, Rambus and DDR, as well as packetized and non-packetized architectures. (CX 379A at 9). About one-third of the Task Group voted to base the next generation DRAM on the SLDRAM architecture and one-third voted to use a packetized architecture. (CX 379A at 9).

1494. Similarly, a few months later, in September and October of 1998, Joe Macri, the Task Group Chair, presented four possible choices on how to proceed with DDR2 definition, from simply tightening the DDR specifications to a complete change of the logic interface, I/O, and core architecture. (RX 1306 at 9; Macri, Tr. 4621-22).

1495. In late 1999, well prior to the close of the DDR2 specification period, Rambus began asserting its patents against JEDEC-compliant SDRAM and DDR products that incorporated the technologies at issue in this case. (F. 1022-29). This assertion of patent rights was widely publicized and well-known in the industry. (CX 1864 at 1; Macri, Tr. 4667-68). JEDEC's development of the DDR2 standard continued in the face of this knowledge.

1496. From June 2000 to June 2001, even as more companies announced licenses for Rambus's technologies in SDRAM and DDR, JEDEC continued to flesh out the DDR2 specification. According to Macri, "Well, once you have kind of a – you know, a list of attributes, major attributes, to create a, you know, a real standard which is in the end a specification, you must add an infinite amount of detail to those attributes. So, this was – during June of 2000 to June of 2001, we were adding the meat, you know, the real description that an engineer would need to truly understand these – these concepts." (Macri, Tr. 4598-99).

1497. All of this JEDEC work from June 2000 to June 2001 was done in full view of Rambus's patents and in full view of Rambus's assertion – accepted by the over one-half of the industry that had licensed the technologies – that SDRAM and DDR SDRAM devices infringed certain claims of those patents. [redacted] (Macri, Tr. 4753-56 (*in camera*)).

1498. From June 2001 through September 2001, JEDEC made further architectural changes to the DDR2 standard. (Macri, Tr. 4599). These changes were made with knowledge of Rambus's patents and demands for royalties.

1499. As of May 2003, the DDR2 specification had not been finalized. (Rhoden, Tr. 411-12).

1. Proposed Alternatives Not Adopted By JEDEC

1500. Steve Polzin of AMD testified that he had discussions with DRAM manufacturers in 2000 about alternatives for programmable CAS latency, programmable burst length, and dual-edge clocking. (Polzin, Tr. 3988, 3996, 4044). At the time, the DDR2 standard was still winding its way through JEDEC. (Polzin, Tr. 4044-45). Polzin understood at the time of these discussions that Rambus patents cover these technologies. (Polzin, Tr. 4047-48). The DDR2 standard, however, still specifies

programmable CAS latency, programmable burst length, and dual-edge clocking. (Polzin, Tr. 4046-48).

1501. Complaint Counsel's economic expert conceded that it is unlikely that JEDEC would discuss alternatives in the year 2000 unless at least some significant number of JEDEC members thought that the adoption of the alternatives was feasible at that point in time. (McAfee, Tr. 7571).

a. Alternative To On-Chip PLL in DDR2

1502. JEDEC explored alternatives to the use of Rambus technologies in DDR2. In late 1998, the Future DRAM Task Group wanted to explore eliminating both on-chip DLL and programmable burst length. (RX 1306 at 10; Macri, Tr. 4705).

1503. The December 1998 Future DRAM Task Group Minutes record that HP proposed to eliminate the on-chip PLL in DDR2. (CX 137 at 3, 27). Those minutes also show that IBM proposed to use a vernier mechanism in place of on-chip PLL. (CX 137 at 4).

1504. Despite this investigation, and despite Rambus's assertion of its patents in 1999, no alternative to on-chip PLL/DLL was adopted. (RX 1854 at 12-14 (preliminary DDR2 specification showing mode register and extended mode register using DLL Reset, and DLL Enable/Disable, "passed committee ballots and went to council at June 2001 meeting")).

b. JEDEC Selection of Programmable CAS Latency

1505. In March and April 2000, JEDEC considered alternatives for programmable CAS latency in SDRAM, DDR, and DDR2, including fixed latency, scaling latency with clock frequency, and using pins or additional commands in DDR2. (RX 1626 at 5-6). At the March 2000 meeting of JC 42.3, Micron

made a proposal entitled, "Simplifying Read Latency for DDRII." (CX 154A at 25; Lee, Tr. 6779-80). The proposal included a section on "Avoiding Programmable Latency in SDR/DDR SDRAMs." (CX 154A at 27-29). The presentation also included a proposed alternative for programmable CAS latency in DDR2. (CX 154A at 30-31; Lee, Tr. 6779-80).

1506. In response to these proposals, Bob Fusco at Hitachi wrote, "For DDR-2, we have no legacy to live with, so I like the Micron proposal. For DDR-1 it's not too late for minor, carefully considered changes, so I'm open to either proposal." (RX 1626 at 4). This response demonstrates that JEDEC could have adopted alternatives if doing so were preferable.

1507. Bill Hovis of IBM rejected the proposals regarding alternatives to programmable CAS latency because of cost concerns. (RX 1626 at 3). For DDR, Hovis still supported programmable CAS latency because "ultimately the flexibility of supporting multiple CAS latencies in one device can result in benefits to the customers that end up buying the memory." (RX 1626 at 3). Hovis similarly insisted that DDR2 retain programmable CAS latency, even though he was "not currently locked in." (RX 1626 at 3-4).

1508. In July 2000, Micron made a presentation entitled, "Pin Selectable Posted CAS for DDR II." (CX 2766 at 1). The proposal included using multiple pins "to select specific latency values," which had the trade off of "higher overhead for pins/traces, lower overhead associated with mode register." (CX 2766 at 3). The proposal also stated, "Latency select pin(s) on DRAMs can be: hardwired, . . . brought out to pins on the module, [or] . . . driven by a modified SPD device." (CX 2766 at 4).

1509. JEDEC ultimately opted to use Rambus's programmable CAS latency technology in DDR2. (Polzin, Tr. 4046; RX 1854 at 12-14).

c. JEDEC Selection of Programmable Burst Length

1510. The preliminary DDR2 specification, published in July 2001, specified a fixed burst length of 4. (RX 1854 at 20; Macri, Tr. 4733-34; Krashinsky, Tr. 2834).

1511. After that specification was published, both AMD and Intel proposed to change the DDR2 specification to add programmable burst length. (Macri, Tr. 4675). At the September 2001 JC42.3 meeting, Intel proposed that DDR2 have burst length of 8 in addition to 4. (CX 174 at 7-8). At that same meeting, AMD also proposed the addition of a burst length of 8. (CX 174 at 8). According to Intel, adding a burst length of 8 would result in a potential improvement of four to ten percent on high-bandwidth applications. (CX 174 at 37). The vote to ballot this proposal was unanimous. (CX 174 at 7-8).

1512. Joe Macri, the Future DRAM Task Group chairman, admitted that he was aware when adding programmable burst length to DDR2 that Rambus would believe it infringes its patents. (Macri, Tr. 4679-83).

1513. JEDEC adopted Rambus's programmable burst length technology in DDR2 despite complete awareness of Rambus's issued patents and demands for royalties. (Polzin, Tr. 4046-47).

d. JEDEC Selection of Dual-Edge Clocking

1514. JEDEC was looking at alternative clocking schemes to avoid Rambus patents. (Krashinsky, Tr. 2828). JEDEC failed to find an acceptable alternative and adopted Rambus's dual-edge clocking technology. (Polzin, Tr. 4047).

1515. At the September 2000 JEDEC meeting, Micron made a proposal that DDR2 incorporate single data rate technology instead of dual-edge clocking. (CX 2769 at 13). Micron made this

proposal to convince the committee that they had a better clocking scheme. (Macri, Tr. 4719-20).

1516. In a November 2000 conference call, committee members discussed going to a single data rate ("SDR") technology. (Macri, Tr. 4639-42). The minutes of that meeting reflect a consensus to try to adopt SDR if it would work. Those minutes state, "HP . . . prefers SDR" and indicate that for IBM, "Single data rate clocks are acceptable provided that it works." (CX 426 at 2). The minutes also indicate that IBM agreed "with the need to avoid I.P. issues." (CX 426 at 3). The minutes state: "Majority of companies prefers [sic] single data rate clocks but not all of them." (CX 426 at 3). "Discussion on single data rate clock vs. doble [sic] data rate clock . . . . Fundamentally question is that is single data rate clock possible? . . . . In general, everyone agreed that SDR clock is ok provided that it works." (CX 426 at 4).

1517. Macri, the chair of the Task Group, believed that everyone knew about Rambus IP at this time; therefore, there was no need to discuss the issue and the JEDEC rules were satisfied even though he did not disclose his knowledge of Rambus patents. (Macri, Tr. 4639-42).

1518. Despite the consensus to use SDR in place of dual-edge clocking "provided we can make it work," JEDEC incorporated dual-edge clocking into DDR2. (Polzin, Tr. 4047).

2. JEDEC Continued to View Rambus Patents As A Collection Of Prior Art

1519. Many JEDEC members were aware of Rambus's patent claims but considered Rambus's patents a collection of prior art when considering the four technologies at issue. (F. 869-70).

1520. Furthermore, JEDEC members continued to believe that Rambus's patents were a collection of prior art when JEDEC

subsequently considered alternatives to Rambus's technologies. (F. 1521-35).

1521. Mark Kellogg of IBM testified that he examined Rambus's patents in 2001. (Kellogg, Tr. 5301). With respect to the technologies in SDRAM and DDR, Kellogg testified that he believed that there was prior art to Rambus's patents, and he said that he had conveyed his opinion to other DRAM manufacturers. (Kellogg, Tr. 5301-02).

1522. According to Kellogg, the DRAM manufacturers "were considering the fact that some of the Rambus patents might be overturned" when making decisions about whether to try to design around Rambus patents. (Kellogg, Tr. 5303-04).

1523. At the May 1992 JEDEC meeting, NEC representative Howard Sussman stated that he had reviewed the claims in Rambus's PCT application and that, in his opinion, many of the 150 claims were barred by prior art. (RX 290 at 3).

1524. Notes taken at the May 1992 JC 42.3 meeting by IBM representative Mark Kellogg state: "NEC: Rambus International Patent 150 pages, Motorola patents/Rambus patent – suspect claims won't hold." (RX 290 at 3; Kellogg, Tr. 5319).

1525. In an email recounting the meeting, Richard Crisp wrote, "Siemens expressed concern over potential Rambus Patents covering 2 bank designs. . . . In response to the patent issue, Sussman stated that our patent application is available from foreign patent offices, that he has a copy, and has noted many, many claims that we make that are anticipated by prior art. He also stated the Motorola patent predated ours (not the filing date!) and it too was anticipated by prior art." (RX 673 at 1). Crisp understood the gist of Sussman's statement to be that "everything that he thought Rambus had invented, somebody else had invented first." (Crisp, Tr. 3492-93).

1526. Siemens's JEDEC representative Willi Meyer prepared a trip report from the May 1992 JC 42.3 meeting that states, "Siemens and Philips concerned about patent situation with regard to Rambus and Motorola. No comments given. Motorola patents have priority over Rambus'. Rambus patents filed but pending." (RX 297 at 5).

1527. Meyer also testified that sixteen months later, at the September 1993 JC 42 meeting, there was an additional discussion of Rambus's patent applications in which someone said that the applications were "stuck in the patent office" and "not proceeding right now." (CX 2057 at 300 (Meyer, Dep.). The speaker then referred to Rambus's patent applications as "a collection of prior art." (CX 2057 at 300 (Meyer, Dep.).

1528. In 1994, during a presentation to Samsung, Dr. Betty Prince stated that "many of the large systems houses believe that Rambus patents are challengeable by previous internal work and/or patents." (RX 153 at 10). This was public information that Dr. Prince had gathered for Samsung. (Prince, Tr. 9003). The presentation went on to state that the early concern about the impact of the Rambus patents on the major systems houses and vendors seems to have diminished considerably. (RX 2153 at 10).

1529. As Dr. Prince explained at trial: "When Rambus first started talking about their product, they were very secretive and nobody really knew what they had. After it was clear what they had, then many of the big companies reviewed the patents that they had already – prior work that they had already had and there was discussion various places in the industry that much of this seemed to have prior art." (Prince, Tr. 9004). Dr. Prince testified that this information was from public sources. (Prince, Tr. 9004).

1530. A November 6, 1995 Mitsubishi memorandum regarding "Request for Cray Patent Investigation as a Countermeasure for the Rambus Patent" states: "In response to the directive from the U Memory Department, we did a prior art

search regarding the patents owned by Rambus, emphasizing the patents by Cray Corporation, and have found at least three issues that are potentially prior art for the Rambus patent." (RX 660A at 3).

1531. Mitsubishi followed up with Cray Corporation and received some additional reassurance. In a November 28, 1995 email, Alan Grossmeier of Cray wrote to Kazutami Ariomoto in Mitsubishi's Memory Devices Department that, based on Cray work, "[w]e have not been concerned about infringing on Rambus patent since if dispute would occur we believe we have sufficient *prior art* to show." (RX 660 at 1).

1532. A 1996 Micron email states: "We have also been [i]nvestigating the prior art related to the area of high-speed DRAMs. From our research, we think many RAMBUS patents read on prior art or other patents." (RX 829 at 2).

1533. As Howard Sussman, who represented NEC and then Sanyo at JEDEC meetings, explained, although the engineers who attended JEDEC meetings were "not really the experts" on construing patent claims, "[f]or prior art, we most likely have knowledge." (Sussman, Tr. 1344).

1534. Although there was no assurance that Ramlink did not infringe Rambus's patents, the Ramlink standard was issued by the IEEE. (Gustavson, Tr. 9300-01). As Wiggers explained at trial, "the SyncLink work went forward, yes, based on the fact that we still felt we were in the public domain, that everything we had done was, you know, based on things that had been done in the public domain. . ." (Wiggers, Tr. 10604). Wiggers testified that he did not take Rambus's patent position very seriously. (Wiggers, Tr. 10604).

1535. In 1997, Craig Hampel of Rambus was informed that Desi Rhoden, currently JEDEC's Chairman of the Board, "was commenting that it looked like there was going to be prior art on

Rambus, that would make [Rambus's] patents difficult to defend." (RX 908 at 1).

XIV. RAMBUS'S ROYALTY RATES ARE IN FACT REASONABLE AND NONDISCRIMINATORY

1536. Professor Teece has studied the semiconductor industry for many years; he has consulted in the industry; and he has focused on understanding patents, licensing and cross-licensing in the semiconductor industry. (Teece, Tr. 10301-02).

1537. Professor Teece is frequently called to advise companies on their licensing policies and the design of licensing arrangements and agreements. (Teece, Tr. 10303). He is also frequently asked to testify on antitrust and patent damages issues. (Teece, Tr. 10303). Much of his consulting work involves the semiconductor industry. (Teece, Tr. 10303). Over the last twenty years, he has advised at least a dozen companies on licensing and licensing strategy. (Teece, Tr. 10417). In addition, as the member of the board of directors of several companies, he has approved licensing agreements and on some occasions actually negotiated them. (Teece, Tr. 10419).

1538. Professor Teece published a paper on licensing and cross-licensing in the semiconductor industry that was published in the California Management Review. (Teece, Tr. 10302). He has written a number of times on the issue of licensing, including one of the first studies on technology transfer and technology licensing (for which he interviewed over one hundred licensing executives). (Teece, Tr. 10418). In the mid-1990's, Professor Teece did a study on cross-licensing, though not specific to the semi-conductor industry, during which he interviewed more licensing executives. (Teece, Tr. 10418).

1539. Professor Teece has been a member of the Licensing Executives Society for about twenty years. (Teece, Tr. 10417). He has addressed licensing executives at the annual meeting of the

Licensing Executives Society and he has published two papers in the journal of that society. (Teece, Tr. 10418).

1540. Professor Teece has been qualified as an expert in a number of courts to testify on the issue of reasonable royalties. (Teece, Tr. 10419).

1541. Complaint Counsel's economic expert, on the other hand, admitted that he had little expertise determining a reasonable royalty rate. (McAfee, Tr. 7737). Nor does he have any expertise in the areas of licensing or technology transfer. (*See* McAfee, Tr. 7144, 11246).

A. Rambus's Royalty Rates Are Reasonable

1. The JEDEC Rules Defined "Reasonable" as the Rate Determined By the Market

1542. J. Kelly, the EIA General Counsel, testified that EIA does not get involved in the determination of whether terms are reasonable and nondiscriminatory; rather, EIA leaves this determination to the "marketplace," i.e., a willing licensee and licensor engaged in arms-length negotiation. (J. Kelly, Tr. 1882-83). As he explained, "We don't get into the definition, the further definition of reasonable and nondiscriminatory at all. We leave that to the parties to work out or the courts." (J. Kelly, Tr. 2073-74).

1543. J. Kelly also admitted that it is not one of the goals of EIA or JEDEC to get the lowest possible royalty rate if there is intellectual property in the standards. (J. Kelly, Tr. 2073).

1544. Robert Goodman of Kentron testified that he understood a reasonable rate to be what the market will agree to pay. (Goodman, Tr. 6088).

1545. Similarly, according to Desi Rhoden, whether licensing terms for patents covering JEDEC compliant products were "fair and reasonable" is to be determined by the courts. (Rhoden, Tr. 658, 663; RX 1461 at 1).

2. Rambus's Royalties Are Comparable To Other Licensing Rates in the Industry and Are "Reasonable" Under the JEDEC Rules

1546. Rambus's royalty rate for its SDRAM licenses for most companies is .75%. (Rapp, Tr. 9832; CX 1680 at 4 (*in camera*); CX 1683 at 13 (*in camera*); CX 1685 at 19 (*in camera*); CX 1686 at 17 (*in camera*); CX 1687 at 16 (*in camera*); CX 1689 at 20, (*in camera*)). Its royalty rate for its DDR licenses (with the exception of its license to Hitachi) is 3.5%. (Rapp, Tr. 9853).

1547. These rates are low compared to other licensing rates in the semiconductor industry. (Teece, Tr. 10429-51).

1548. The IBM Worldwide Licensing Policy sets forth royalty rates from 1-5% of selling price: "The royalty for use of IBM's patents may be based on the licensee's selling price of each product covered by one or more licensed patents or on the royalty portion selling price of such product, the choice being left to the licensee. . . . The royalty rates are 1% of the selling price if the product is covered by one Category I patent and 2% of the selling price if the product is covered by two or more Category I patents . . . . If the product is covered by one, two or three or more Category II patents, the royalty will be, respectively, 1%, 2% or 3% of the selling price added to any royalty incurred for Category I patents." (JX 9 at 24).

1549. Mark Kellogg presented this IBM Worldwide Licensing policy to JEDEC at a meeting of JC 42.5 on December 2, 1991. (JX 9 at 24; Kellogg, Tr. 5236). No one, to his memory, suggested that IBM's license rates were unreasonable. (Kellogg, Tr. 5238-39). Kellogg was not authorized by IBM to discuss royalty rates;

he therefore could not tell anyone at JEDEC that IBM would license on other than IBM's standard rates. (Kellogg, Tr. 5236-37).

1550. Gordon Kelley agreed that the IBM Worldwide Licensing Policy shown at the December 1991 JEDEC meeting shows royalty rates of one to five percent, and he too did not recall anyone saying that these rates were unreasonable. (G. Kelley, Tr. 2620).

1551. The IBM Standards Practice Manual that was in effect in 1996 states, "The normal royalty rate for a license to IBM patents ranges from one percent to five percent of the selling price for the apparatus that practices the patents. This is a very reasonable rate in our industry and generally meets the requirement of standards organizations that licenses be made available on reasonable and nondiscriminatory terms and conditions." (RX 653 at IBM/2 128124).

1552. Similarly, the IBM Standards Program, which superseded the IBM Standards Practice Manual, states, "The normal royalty rate for a license to IBM patents ranges from one percent to five percent of the selling price for the apparatus that practices the patents. This is a very reasonable rate in our industry and generally meets the requirement of standards organizations that licenses be made available on reasonable and nondiscriminatory terms and conditions." (RX 653 at IBM/2 153802).

1553. The IBM website contains IBM's Standards Practices and states that IBM's royalty rates for patent licenses granted to members of standard setting organizations is one to five percent. (RX 2105-07 at 1).

1554. AMD [redacted] (Heye, Tr. 3919-20 (*in camera*); CX 1420 at 8 (*in camera*)).

1555. In February 1990, Digital Equipment Corporation wrote to JEDEC to inform its members that Digital would agree to license its U.S. Patent No. 4,851,834 and corresponding foreign patents for a royalty rate of one percent of sales. (JX 1 at 24).

1556. After DRAM manufacturers complained of administrative burdens associated with royalty agreements, Kentron changed from charging five percent royalties for Kentron's FEMMA technology to pricing its patented flex tabs, which are a necessary input for the FEMMA technology, so as to receive the equivalent of the five percent royalty. (Goodman, Tr. 6020-22, 6078-80). Kentron has also set the price of its patented switches, used in its QBM technology, such that for a QBM product priced around $200, the purchaser would pay an additional eighteen dollars included within that price for the Kentron patented QBM technology (approximately nine percent). (Goodman, Tr. 6087). As a matter of economics, a higher price built into a product that is a necessary input is the equivalent of the same amount charged as a royalty. (Teece, Tr. 10432).

1557. In Rambus's 1992 business plan, Rambus recognized that its royalty rates were in line with semiconductor "traditional royalty levels of 1-5%." (CX 543A at 14).

1558. Based on these cited industry rates, as Professor Teece concluded, Rambus's royalty rates are reasonable. (Teece, Tr. 10429-51). The industry royalty rates cluster around four to five percent. The Rambus SDRAM royalty rate of 0.75% is at the low end of what comparable technologies command. (Teece, Tr. 10451). Rambus's DDR royalty rate of 3.5% is near the low end of the middle of comparable rates. (Teece, Tr. 10451).

1559. The industry rates used in this comparison underestimated actual rates because the semiconductor industry rates tend to reflect balancing payments on cross-licenses rather than rates for a straight license like Rambus's. (Teece, Tr. 10423-24). A royalty rate that is paid as a balancing payment (e.g., where

two companies cross-license, the company with the smaller or weaker patents must pay the other party a balancing payment) reflects a much higher implied royalty rate for the underlying intellectual property rights. (Teece, Tr. 10424).

1560. Complaint Counsel's economic expert recognized this when he admitted that companies can get economic value from internally developed patented technology because this gives the company a benefit in cross-licensing negotiations. (McAfee, Tr. 7698). Appleton testified that Micron decreased the amount of revenue it pays in royalty rates by devoting more resources to its own research and development projects. (Appleton, Tr. 6299-300).

1561. Rambus's royalty rates for SDRAM and DDR SDRAM were agreed to in armslength negotiations with major industry players. (Teece, Tr. 10425).

1562. The conclusion that the Rambus's royalty rates for SDRAM and DDR are reasonable is not undermined by the fact that Rambus's RDRAM royalty rates are lower than its rates for DDR because those licenses are not comparable. (Teece, Tr. 10534 (*in camera*)).

1563. [redacted] (Teece, Tr. 10534-35 (*in camera*); MacWilliams, Tr. 4824-25).

1564. Also with RDRAM, Rambus had an economic incentive to accept lower royalty rates because it was trying to build a new technology and would get the benefit of co-development from its licensees. (Teece, Tr. 10535-36 (*in camera*)). Rambus was able to "participate in future design improvements," obtain information about the partner's customers, and be "part of the process going forward." (Farmwald, Tr. 8179-80).

1565. Rambus's RDRAM licenses form a partnership; Rambus works with the licensee, and receives valuable feedback

and information. (Farmwald, Tr. 8241). For non-DDR by contrast, there is no partnership, and Rambus receives no additional benefits. (Farmwald, Tr. 8241). [redacted] (Teece, Tr. 10535 (*in camera*)).

1566. Complaint Counsel's economic expert admitted that although Rambus's RDRAM licenses have benefits to Rambus that its DDR licenses do not, he did not quantify those benefits when comparing the DDR and RDRAM license rates. (McAfee, Tr. 7835).

1567. Complaint Counsel did not present evidence sufficient to rebut Respondent's showing that its royalty rates were reasonable.

B. Rambus's Royalty Rates Are Nondiscriminatory

1. JEDEC Has Left the Definition of "Nondiscriminatory" to the Market and the Courts

1568. As Rhoden testified, JEDEC takes no position on the definition of questions regarding "non-discriminatory." (Rhoden, Tr. 665). Rather, JEDEC leaves the determination of what terms are nondiscriminatory to the market and, if that fails, to the courts. (J. Kelly, Tr. 1882-83).

1569. For instance, when Dick Foss of Mosaid wrote to JEDEC to ask whether the RAND requirement means that Mosaid had to license its DLL patent on the same terms to licensees currently under a broad patent license from Mosaid as to those who licensed just the DLL technology, Townsend responded that the details of the license terms were left to Mosaid's negotiations with individual companies. (RX 1461 at 1-2). Desi Rhoden also replied that the interpretation of RAND is left to the courts. (RX 1461 at 1).

1570. Similarly, JEDEC did not object when Mosaid indicated that there would be differences in its licenses for its DLL patent depending on whether the licensee licensed only the DLL patent or multiple patents from Mosaid. (*See* CX 400 at 2). In May 1999, Dick Foss wrote to JEDEC stating, "[t]here is inevitably a difference between someone who gets a DLL license thrown in as part of a multi-million settlement on multiple patents and someone who just wants a license for DLL usage." (CX 400 at 2). He also wrote, "[t]here will be differences in terms if company 'a' is a general licensee (and is automatically licensed anyway) and company 'b' is not and so will be expected to take a 'reasonable' license if wanting to use our IP on the item." (CX 400 at 1). Jim Townsend responded that he would presume that this arrangement was acceptable, though he thought Mosaid should ask counsel. (CX 400 at 1). Joe Macri did not recall any objection to Mosaid's two tiered licenses and never raised the issue with Dick Foss. (Macri, Tr. 4714-16; RX 1457).

1571. Robert Goodman of Kentron testified that he understood that a nondiscriminatory rate should be measured at a particular point in time; at different points in time, charging different rates is not discriminatory if there is some reason to charge a different rate. (Goodman, Tr. 6088).

1572. In a September 6, 2001 letter from Christopher Pickett, General Counsel of Tessera, Inc., to John Kelly, EIA's President and General Counsel, Pickett recounted his discussion with Kelly to the effect that either the parties or the courts must resolve whether JEDEC's RAND policy allowed Tessera to charge a higher rate to litigating parties:

> As we discussed on the phone and as is set forth in your letters, this JEDEC policy is intentionally broad in order to allow the parties to negotiate terms and come to their own decision on what the words mean in the particular circumstances. The JEDEC patent policy does not negate the context

> of what is commercially reasonable in determining license terms with a particular licensee. Whether a patent owner may consider a company's adverse action in negotiating licensing terms is a matter that must be resolved, in the first instance, by the negotiating parties themselves. If the parties cannot reach agreement, they may submit the question to the courts for resolution.

(RX 1885 at 1).

2. The Economic Evidence That Rambus's Royalty Rates Are Nondiscriminatory

1573. Discrimination in licensing is a circumstance where different parties are offered different deals. (Teece, Tr. 10538 (*in camera*)). A nondiscriminatory license is one where everyone is offered the same deal at about the same time. (Teece, Tr. 10538 (*in camera*)).

1574. Rambus offered its SDRAM and DDR licenses to everybody on more or less the same terms. (Farmwald, Tr. 8242).

1575. Higher royalties for litigating parties are not discriminatory in an economic sense because litigation involves costs, including legal costs and the diversion of management and litigation involves a risk that the patent will be found invalid or not infringed. (Teece, Tr. 10541 (*in camera*)).

1576. In addition, as patents mature, as they get tested in the courts and are affirmed, they become more valuable because the uncertainty about infringement and invalidity goes down. (Teece, Tr. 10540 (*in camera*)). In other words, the fact that Rambus charged a higher rate after litigation could be justified by changed perceptions regarding the strength of the patents.

1577. If a firm knows that it will receive the same royalty rate as other licensees even if it litigates and loses, then it will have a

disincentive to license because it is a no-lose proposition to take the issue to court. (Teece, Tr. 10542 (*in camera*)). This creates a "heads I win, tails I break even" problem and encourages future litigation by other potential licensees. (Teece, Tr. 10542-43 (*in camera*)).

1578. Charging higher royalties to litigating parties is therefore cost justified in the sense that it avoids future litigation costs. (Teece, Tr. 10542, 10551 (*in camera*)).

1579. Complaint Counsel's economic expert used an analysis based on production costs to conclude that Rambus's DDR royalty rate to Hitachi was discriminatory. (McAfee, Tr. 7827). But for purposes of determining whether patent licenses are discriminatory, it does not make sense to look at the issue in terms of whether the differences are cost justified in a traditional sense because intellectual property is not priced on a cost basis. (Teece, Tr. 10544-45 (*in camera*)). In this context, therefore, it does not make sense to look at traditional marginal costs. (Teece, Tr. 10545 (*in camera*)).

1580. Moreover, Complaint Counsel's economic expert effectively admitted that litigation imposes costs on Rambus and that it is economically rational to develop a strategy to avoid those costs. (McAfee, Tr. 7829). He went on to admit that it would be consistent with economic theory to charge a higher royalty rate to licensees that require the patent holder to incur costs before taking a license. (McAfee, Tr. 7829). Further, he recognized that Hitachi's litigation with Rambus imposed risks on Rambus (McAfee, Tr. 7830), and that a licensing strategy of charging more to companies that choose to litigate would maximize Rambus's profits by reducing its future costs. (McAfee, Tr. 7831).

1581. Complaint Counsel's economic expert did not make any assumption as to whether charging a higher rate to companies that choose to litigate violates the JEDEC nondiscrimination policy. (McAfee, Tr. 7832).

XV. THE EVIDENCE DOES NOT ESTABLISH THAT THE DRAM INDUSTRY IS LOCKED IN TO USING THE RAMBUS TECHNOLOGIES

1582. Complaint Counsel contends that the DRAM industry was "locked in" to using the Rambus technologies once they were adopted into the JEDEC standards. To the contrary, the evidence shows that JEDEC has considered changing its standards and switching to alternatives to Rambus's technologies. (CX 154A at 25-29; RX 1626 at 4).

1583. In 2000, Steve Polzin of AMD discussed alternatives to Rambus's technologies with DRAM manufacturers. (Polzin, Tr. 3988, 3996, 4044).

1584. Also in this time period, JEDEC's Future DRAM Task Group considered alternatives for each of Rambus's technologies, but ended up adopting the Rambus technologies with full knowledge of Rambus's issued patents and demands for royalties. (*See* F. 1022-29).

1585. As Complaint Counsel's own expert conceded, JEDEC members would not be discussing alternatives to Rambus's technologies in 2000 unless they thought that the alternatives were commercially viable and could be adopted. (McAfee, Tr. 7571).

A. An Historical Look at How the DRAM Industry Transitions To New Technologies

1. Statistical Evidence of Co-Existing DRAM Standards

1586. In 1994, fast page mode ("FPM") DRAM accounted for 96.7% of the revenue for DRAM. (Rapp, Tr. 10100, 10248). The remaining 3% of DRAM revenue was accounted for by other DRAM technologies. (Rapp, Tr. 10248).

1587. In 1995, FPM accounted for 87.2%, EDO DRAM for 9.9%, and other DRAM for 2.9% of DRAM revenue. (Rapp, Tr. 10100-01, 10248).

1588. In 1996, FPM accounted for 39.4%, EDO for 52.7%, SDRAM for 4.3%, RDRAM for 0.5%, and other DRAM for 3.1% of DRAM revenue. (Rapp, Tr. 10101, 10248).

1589. In 1997, FPM accounted for 8.1%, EDO for 55.2%, SDRAM for 33.5%, DRAM for 1.3%, and other DRAM for 1.8% of DRAM revenue. (Rapp, Tr. 10101, 10248).

1590. In 1998, FPM accounted for 8.8%, EDO for 27.6%, SDRAM for 60.8%, RDRAM for 1.6%, and other DRAM for 1.3% of DRAM revenue. (Rapp, Tr. 10101, 10249).

1591. In 1999, FPM accounted for 10.5%, EDO for 17.5%, SDRAM for 69.3%, RDRAM for 1.1%, and other DRAM for 1.5% of DRAM revenue. (Rapp, Tr. 10102, 10249).

1592. In 2000, FPM accounted for 5.2%, EDO for 11.1%, SDRAM for 78.4%, RDRAM for 3%, DDR for 0.4%, and other DRAM for 1.9% of DRAM revenue. (Rapp, Tr. 10101, 10249).

1593. In 2001, FPM accounted for 4%, EDO for 7.7%, SDRAM for 69.7%, RDRAM for 12.5%, DDR for 5.3%, and other DRAM for 0.8% of DRAM revenue. (Rapp, Tr. 10101, 10249).

1594. Within each of these categories, there were different speeds (*e.g.*, for SDRAM, PC66, PC100, PC133; for DDR, DDR200, DDR266, DDR333, DDR400). (Rapp, Tr. 10249-50; Gross, Tr. 2348-56; Polzin, Tr. 3998-4005).

1595. These figures show that, in any given year, the DRAM market is divided among multiple incompatible standards and

demonstrate that there is no technological or economic force mandating a single standard in the DRAM industry. (Rapp, Tr. 10103-04).

2. Industry Redesign of DRAM

1596. Brian Shirley, Design Operations Manager for the Computing and Consumer group at Micron Technology (Shirley, Tr. 4133), testified that Micron "taped out," or went through the entire design process, for numerous different DRAM each year. F.1596-1603

1597. [redacted] (Shirley, Tr. 4218 (*in camera*)).

1598. In 1998, [redacted] (Shirley, Tr. 4218-19, 4226 (*in camera*)).

1599. In 1999, [redacted] (Shirley, Tr. 4220-23, 4225-26 (*in camera*)).

1600. In 2000, [redacted] (Shirley, Tr. 4223-25 (*in camera*)).

1601. In 2001, [redacted] (Shirley, Tr. 4227 (*in camera*)).

1602. In 2002, [redacted] (Shirley, Tr. 4228-29 (*in camera*)).

1603. According to Shirley, Micron is constantly, on an everyday basis, designing DRAMs and over time introducing new masks for DRAMs and over time retiring masks for parts that Micron is no longer offering. (Shirley, Tr. 4282 (*in camera*)).

3. The Manufacture of Multiple DRAMs to Accommodate New Technology

1604. Micron CEO Steven Appleton testified that Micron currently manufactures a wide variety of DRAMs, including

EDO, SDRAM, DDR, DDR2, and various specialty DRAMs, such as pseudostatic RAMs. (Appleton, Tr. 6264).

1605. In a "response script" prepared by Micron in December 1996 for use in discussions with customers, Micron described its ability to manufacture various different kinds of DRAMs. (RX 836 at 2-4).

1606. The December 1996 "response script" was prepared by Micron in connection with Intel's announcement that it intended to design its next generation of chipsets to work with Rambus memory devices, then denominated "nDRAM." (RX 836 at 2; Lee, Tr. 6853-54). At the time, Micron did not have a license to manufacture the Rambus device. (RX 836 at 2; Lee, Tr. 6856).

1607. The December 1996 "response script" includes possible questions and proposed answers. One such question is "What would having to make 'nDRAM' or SyncLink mean to Micron?" Micron's answer to this question is instructive:

> Keep in mind that ALL of these DRAM technologies use the same DRAM process, the same DRAM cell, and virtually the same DRAM array.
> . . .
> Switching from one product to another, while still using the same core technology, involves only changing priorities in design and product engineering and may mean some differences in our assembly and test equipment purchases. SDRAM, SLDRAM, nDRAM all use the same fab equipment and core DRAM technology. *In short, while the flavors might change, it's still a DRAM*.

(RX 836 at 3) (emphasis added).

1608. Since the first silicon came out of Infineon's Richmond plant in January 1998, Infineon's has plant manufactured four different types of die shrinks for 64MB SDRAM (through 2001); three different types of die shrinks for the 256 SDRAM (2000-present); the 128MB SDRAM (2001-2002); and two different types of die shrinks for the 256MB DDR (2000-present). (Becker, Tr. 1167-69, 1179-83).

1609. For Infineon, every "shrink" (i.e., reduction in the feature size of the DRAM) and redesign requires a new "mask set" for the product. (Becker, Tr. 1170-73). In the two and a half to three years in which the Infineon Richmond plant manufactured 64MB SDRAMs, it had to make at least 20 different mask sets. (Becker, Tr. 1170-73).

1610. When the Infineon Richmond plant transitioned some of its lines from SDRAM to DDR, Infineon had to purchase additional equipment because DDR requires additional manufacturing processes. (Becker, Tr. 1182-83). Nonetheless, DDR and SDRAM were made in the same processing facility, and except for the additional equipment, its manufacturer used the same processing equipment. (Becker, Tr. 1182-83).

1611. In fact, of the DRAM currently produced by the Infineon Richmond plant, approximately two-thirds are DDR and one-third are SDRAM. (Becker, Tr. 1139).

1612. Infineon's 2002 product information guide lists three Infineon manufacturing plants, which produce the following product categories: DDR SDRAM, SDR SDRAM, Graphics RAM, Mobile-RAM, and RLDRAM. (CX 2466 at 2-3).

1613. The Infineon 2002 product information guide lists the following densities for DDR products as either being currently in production by Infineon or planned for production in 2002: 128 Mb DDR, 256 Mb DDR, 256 Mb FBGA DDR, and 512 Mb DDR. (CX 2466 at 5). Each of these different density products is

produced in three different organizations (e.g., for the 128Mb DDR - 32Mx4, 16Mx8, and 8Mx16). (CX 2466 at 5). Each of these different organizations is produced in several speeds (e.g., for the 512Mb DDR in the 128Mx4 organization – DDR200, DDR266A, and DDR333). (CX 2466 at 5). In all, according to the product guide, Infineon had in production 34 different DDR products in 2002.

1614. The Infineon 2002 product information guide lists the following densities for SDRAM products as either being currently in production by Infineon or would be in production in 2002: 256Mb SDRAM, 256Mb FBGA SDRAM, and 512Mb SDRAM. (CX 2466 at 6-7). Each of these different density products is produced in three different organizations (e.g., for the 256Mb SDRAM - 64Mx4, 32Mx8, and 16Mx16). (CX 2466 at 6). Each of these different organizations is produced in several speeds (e.g., for the 512Mb SDRAM in the 128Mx4 organization – PC100 and PC133). (CX 2466 at 7). In all, according to the product guide, in 2002 Infineon had in production twenty-seven different SDRAM products in 2002.

1615. In addition, the Infineon product guide shows that Infineon produced seven different types of Graphics RAM, twenty different types of Mobile DRAM, and six different types of RLDRAM (according to the part numbers) in 2002. (CX 2466 at 8-9).

1616. Infineon's Richmond plant currently manufactures all twelve of the different types, organizations and speeds of 256-megabit SDRAMs listed in the Infineon 2002 product information guide (CX 2466), as well as DDR products. (Becker, Tr. 1143).

1617. Infineon is able to shift its production of DRAM to a different density within fourteen months. (Becker, Tr. 1146-48). Die shrinks require new equipment, new processes, putting in the capability to run the wafers, electrical performance testing of wafers and process tweaking, design tweaking and "some

redesigns," reliability testing, customer qualification and feedback. All this takes fourteen months. (Becker, Tr. 1158).

1618. Infineon is able to shift its production of DRAM to increased speeds in as little as three to four months. (Becker, Tr. 1148-49).

1619. When Infineon shifted some of its manufacturing lines from producing SDRAM to producing DDR, the shift took sixteen to seventeen months. (Becker, Tr. 1149-50).

1620. If technically feasible, the alternatives proposed by Professor Jacob could, on his statement of "the industry experience of how often a DRAM normally gets revised during its manufacturing cycle," each have been implemented in a six to twelve month time frame. (Geilhufe, Tr. 9674-75).

1621. These facts show that scale economies are not so powerful that they drive the industry necessarily to a single standard technology at any one time. (Rapp, Tr. 9894-95).

1622. Economies of scale occur at the plant level. (Rapp, Tr. 9893). Plants in the industry often produce at the same time a variety of DRAM (using different technologies, DRAM of different speeds, etc.). (Rapp, Tr. 9893). For example, RDRAM, SDRAM, and DDR have coexisted in the marketplace. (Rapp, Tr. 9893-94). Similarly, different subgenerations of DRAM – e.g., PC66, PC100, PC133 – have coexisted in the marketplace. (Rapp, Tr. 9893-94). This shows that the economics of the industry does not require a single standard. (Rapp, Tr. 9893).

1623. The coexistence of multiple standards also shows that network effects in the DRAM industry are not so high as to make it impractical to switch to an alternative technology. (Rapp, Tr. 9895).

4. Coordination of New Industry Standards

1624. That the industry is able to coordinate changes in technology can be seen by the experience of AMD. Prior to its K7 microprocessor, AMD produced microprocessors that were "pin compatible" with Intel processors. (Heye, Tr. 3653). That is, AMD processors could be plugged into sockets designed for Intel processors and could use the entire Intel-based infrastructure. (Heye, Tr. 3653). An infrastructure in a computer consists of a north bridge (also called a chipset), which connects the microprocessor via a bus to the memory, graphics, and the south bridge. (Heye, Tr. 3655-58). The south bridge communicates with peripheral devices, such as the keyboard and mouse, and the BIOS, which communicates with the microprocessor. (Heye, Tr. 3655-58).

1625. During this time, AMD took no more than fifteen to eighteen months to design and produce a K7 north bridge, starting from scratch. (Heye, Tr. 3767-69). In June 1999, AMD launched the first AMD K7 processor, which used the AMD750 chipset with a 200MHz front side bus (FSB) and was compatible with PC100 SDRAM. (Polzin, Tr. 3998-01).

1626. Soon thereafter, third party vendors such as VIA designed and launched chipsets for the K7 processor that were compatible with PC133 SDRAM. (Polzin, Tr. 3994, 4001; Heye, Tr. 3769-70). This change required the development of a different north bridge and a new motherboard. (Heye, Tr. 3769-70).

1627. In September 2000, AMD launched a new version of the K7 processor using a 266 MHz FSB and the newly designed AMD 760 chipset, which was compatible with DDR200 and DDR266. (Polzin, Tr. 4001). The design of the new chipset took only fifteen to eighteen months, and the resulting chipset was not backward compatible with SDRAM. (Heye, Tr. 3767-69).

1628. To transition from using SDRAM to DDR, the newly established AMD infrastructure needed newly designed

motherboards, newly designed DIMMs, and a new BIOS. (Heye, Tr. 3767-69).

1629. As part of this transition to DDR, AMD gave motherboard samples to manufacturers in March 2000, and those manufacturers were able to produce the DDR compatible motherboards in volume by September 2000. (Polzin, Tr. 4017-18).

1630. In fact, according to an internal memorandum, AMD decided to transition to DDR in early 1999, was able to power up a complete system by December 1999, and was shipping units by October 2000. (CX 2158 at 2; Heye, Tr. 3807-10).

1631. In October 2002, AMD launched a new version of the K7 processor with a 333MHz FSB. Third party chipsets made for this version were compatible with DDR333. (Polzin, Tr. 4004).

1632. During these changes, portions of the infrastructure other than the chipset changed as well. For example, DDR333 had different DIMM specification from those of previous generations of DDR. (Polzin, Tr. 4006-07).

1633. In May 2003, AMD launched the K7 processor with a 400MHz FSB. (Polzin, Tr. 4004). Matched with newly designed third party chipsets, this system uses DDR400. (Polzin, Tr. 4004).

1634. In sum, the AMD K7 systems went from using PC100 to PC133 to DDR200 and 266 to DDR333 to DDR400 – 5 transitions – all in the time period from June 1999 to May 2003. (F. 43-53).

1635. Compaq, an OEM that produced personal computers, servers, and workstations, and is now part of HP (Gross, Tr. 2265), has gone through similar transitions. (F. 1636-42).

1636. Compaq started using EDO DRAM in its products in 1995. (Gross, Tr. 2348).

1637. In 1997, Compaq shifted to using PC66 SDRAM in its computers, which required different chipsets and different motherboards. (Gross, Tr. 2348-50). PC66 SDRAM was an Intel standard. (Gross, Tr. 2348-49).

1638. In 1998, Compaq shifted to using PC100 SDRAM in its computers. (Gross, Tr. 2348-49). The PC100 SDRAM was an Intel standard. (Gross, Tr. 2348-49). It was not backward compatible with PC66 SDRAM. (Gross, Tr. 2348-49).

1639. In 1999, Compaq shifted to using PC133 SDRAM in its products. (Gross, Tr. 2353). The PC133 SDRAM was an Intel standard. (Gross, Tr. 2353).

1640. In 2001, Compaq/HP shifted to using DDR 266 in its products. (Gross, Tr. 2354). DDR requires a different chipset than does DRAM. (Bechtelsheim, Tr. 5958). DDR is not backward compatible with SDRAM; a DDR device cannot be used in an SDRAM socket (Bechtelsheim, Tr. 5958).

1641. In late 2002, Compaq/HP shifted to using DDR 333 in its products. (Gross, Tr. 2356).

1642. From 1995 to 2002, therefore, Compaq shifted from using EDO DRAM to PC66 SDRAM to PC100 SDRAM to PC133 SDRAM to DDR266 to DDR333 in its products. (F. 56-61).

1643. There are of course other examples of the rapid product changes in the computer industry. For instance, Barry Wagner, the manager of technical marketing at NVIDIA, a company that produces graphics processors, testified that NVIDIA launched fourteen new products in the space of six years. (Wagner, Tr. 3820, 3875-76).

1644. If there were a change in the existing standards to incorporate alternatives to Rambus's technologies, only a small portion of the overall infrastructure would need to be changed. (Heye, Tr. 3742-43).

1645. Based on evidence of a transition by AMD, a shift to alternative technologies would incur few additional costs or coordination difficulties beyond those that would be incurred when the industry was in transition to a new standard. (See Polzin, Tr. 4040-42).

B. Switching Costs Do Not Support Theory of Industry Lock In

1. Such Costs Are Not Prohibitive

1646. "Lock in" is a term used in economics to identify a situation where switching costs prohibit consumers from changing to another product or technology. (Rapp, Tr. 9873). Switching costs are the costs incurred to transition to an alternative product or technology. (Rapp, Tr. 9873-74).

1647. Specific investments and switching costs are not identical. (Rapp, Tr. 9875-77). For instance, a company may make a specific investment of $100 million in building a coal-burning plant located near a particular coal mine. If, in response to an increase in the price of coal from the coal mine, the only way to avoid paying the price increase is to shut down the plant and build a new plant in another location for $100 million, the switching costs and the specific investment of $100 million are the same. (Rapp, Tr. 9875-77). If, however, the coal plant can be converted to a gas burning plant for a cost of $5 million, the switching costs are $5 million, not the $100 million to build a new plant. (Rapp, Tr. 9875-77).

1648. With respect to DRAM, the cost of constructing and equipping a fabrication facility is not relevant to switching costs. (Rapp, Tr. 9877-78). This is because a DRAM facility may produce several types of DRAM; there is no need to build a new DRAM facility to produce a new type of DRAM. (Rapp, Tr. 9877-78).

1649. The fact that an industry has high fixed costs and low marginal costs does not have any bearing on switching costs unless the fixed costs have to be replicated in their entirety in order to switch to a new technology. (Rapp, Tr. 9880).

1650. Complaint Counsel's economic expert admitted on cross-examination that he did not quantify or "add up" any switching costs. (McAfee, Tr. 7716-17, 11356). By contrast, Respondent's expert, Geilhufe, testified regarding his estimates of these costs. (Rapp, Tr. 9884-85, 10122-24).

1651. It is not possible for an economist to make a sound judgment about whether switching costs are high enough to create lock in without quantifying those costs. (Rapp, Tr. 9881).

1652. The switching costs for a DRAM manufacturer to shift from using the Rambus technologies to alternative technologies may be calculated by summing the additional one-time-only fixed costs associated with switching to the alternative technologies. (Rapp, Tr. 9883-85).

1653. Dr. Rapp's calculations show that switching costs associated with shifting to alternatives to Rambus's technologies were relatively low in comparison with the expenses associated with manufacturing DRAMs in general and that DRAM manufacturers could therefore have switched at any point. (Rapp, Tr. 9878).

1654. For example, to maintain the functionality provided by programmable CAS latency and programmable burst length when

switching to fixed CAS latency and fixed burst length requires twelve different parts (three different CAS latencies and four different burst lengths). (Rapp, Tr. 9883-85). The additional fixed costs associated with switching to fixed CAS latency and fixed burst length are: $300,000 in additional design costs for the three CAS latencies; $400,000 in additional design costs for the four different burst types; $250,000 per part in additional qualification costs times twelve different parts; and $50,000 in additional photo-tooling costs times twelve different parts – this totals $4.3 million. (Rapp, Tr. 9885).

1655. The total of the cost estimates provided by Geilhufe, although not inclusive of all switching costs, is low, relative to DRAM production costs in general, (Rapp, Tr. 9886), and less than the royalties paid to Rambus to license the use of programmable burst length in SDRAM. (Rapp, Tr. 9886-87). If fixed CAS latency and fixed burst length for example, were truly viable non-infringing alternatives, a manufacturer might profitably switch to those alternatives. (Rapp, Tr. 9886-87).

1656. The evidence shows assuming that the alternatives were preferable in cost performance terms, certain of the proposed alternatives to programmable CAS latency might have been implemented when manufacturers were going through technology upgrades or at the time of the transition from SDRAM to DDR SDRAM. (Soderman, Tr. 9418). Such regular redesigns happened on the order of every six to twelve or eighteen months. (Soderman, Tr. 9418; Geilhufe, Tr. 9615). For example, Bill Hovis of IBM could have accepted proposals regarding alternatives to programmable CAS latency for DDR2, but rejected them even though he was “currently not locked in.” (RX 1626 at 3-4).

1657. The switching costs for any combination of alternatives for Rambus’s four technologies may be calculated by summing the design, qualification, and photo-tooling costs associated with those alternatives as provided by Geilhufe. (Rapp, Tr. 10123-24).

The switching costs for the fixed CAS latency and fixed burst length alternatives are assumed to be typical, if not higher than, the switching costs for the other alternatives. (Rapp, Tr. 10124).

1658. Complaint Counsel's economic expert was not persuasive because he admitted that he did not quantify or "add up" any switching costs. (*See* McAfee, Tr. 7716-17; 11356). He also admitted that switching from Rambus's technologies to alternative technologies would be less costly than the switch from SDRAM to RDRAM. (McAfee, Tr. 7717-18).

2. Coordination Issues Would Not Preclude Switching to New Technology

1659. Complaint Counsel's economic expert admitted that switching away from Rambus's technologies to alternative technologies would involve the same categories of costs that were incurred when the industry went from SDRAM to DDR, and from PC100 SDRAM to another grade of PC SDRAM. (McAfee, Tr. 7714-15, 11357).

1660. Coordination issues with producers of complementary goods would not prevent switching away from the Rambus technologies. (Rapp, Tr. 9889). It is assumed that coordination of this sort is not uncommon in the industry; there is no evidence that suggests that any coordination issues with switching away from Rambus's technologies could not be resolved in the ordinary course of business. (Rapp, Tr. 9889-90).

1661. Coordination for a switch away from Rambus's technologies would not be difficult even if the DRAM industry has made investments in using the Rambus technologies. (Rapp, Tr. 9890). If there were truly viable non-infringing alternatives, it is assumed that the coordination issues faced by the industry would not be any more difficult than those that the industry faces routinely in other situations. (Rapp, Tr. 9890-91).

1662. Complaint Counsel contend that coordination would be difficult because some DRAM manufacturers are licensed under Rambus's patents, but others are not. But the fact that some DRAM manufacturers are licensed to use Rambus's technologies and others are not would assumably not affect the ability of the industry to coordinate switching, because all manufacturers have an interest in using alternatives that are best in cost-performance terms. (Rapp, Tr. 9891-92).

1663. Complaint Counsel's economic expert admitted that he did not reach a conclusion as to whether the interests of the fifty percent who have licensed from Rambus have interests regarding a standard that eliminates the patented technologies that are different from the fifty percent who have not taken a license. (McAfee, Tr. 7723).

1664. DRAM manufacturers were not locked in to using the Rambus's technologies at any point in time from 1990 to today. (Rapp, Tr. 9896). Their continued used of the Rambus technologies is due to the fact that the four Rambus technologies are superior in cost-performance terms to any alternatives. (Rapp, Tr. 9896-99). This is true for the two Rambus technologies used in SDRAM, the four used in DDR, and the four used in DDR2. (Rapp, Tr. 9896-99).

1665. The fact that the DRAM industry continues to use the four Rambus technologies in DDR2 when that standard was developed after Rambus's issued patents and their claimed scope were well known in the industry, demonstrates that Rambus's technologies were superior in cost-performance terms even taking into account Rambus's royalty rates. (Rapp, Tr. 9898-99).

PART THREE: ANALYSIS AND CONCLUSIONS OF LAW

I. PROCEDURAL ISSUES

A. Standard of Proof

The parties' burdens of proof are governed by Commission Rule 3.43(a), Section 556(d) of the Administrative Procedure Act ("APA"), and case law. FTC Rules of Practice, Interim rules with request for comments, 66 Fed. Reg. 17,622, 17626 (April 3, 2001). Pursuant to Commission Rule 3.43(a), "counsel representing the Commission . . . shall have the burden of proof, but the proponent of any factual proposition shall be required to sustain the burden of proof with respect thereto." 16 C.F.R. § 3.43(a).

The preponderance of the evidence standard typically governs in FTC enforcement actions. *In re Adventist Health System/West*, 117 F.T.C. 224, 297 (1994) ("Each element of the case must be established by a preponderance of the evidence"); *FTC v. Abbott Laboratories*, 853 F. Supp. 526, 535 (D.D.C. 1994) (government must show "by a preponderance of the evidence that [defendant's] action was the result of collusion with its competitors"). *See also Herman & MacLean v. Huddleston*, 459 U.S. 375, 387-91 (1983) (preponderance of the evidence standard applies to enforcement of antitrust laws); *Steadman v. SEC*, 450 U.S. 91, 95, 102 (1981) (APA establishes preponderance of the evidence standard of proof for formal administrative adjudicatory proceedings).

The Complaint, although it alleges that Respondent engaged in deception, does not assert a cause of action for fraud, nor must fraud be proven to establish antitrust liability in this case. Enforcement actions brought under Section 5 of the FTC Act often involve allegations of deception, sometimes even labeled "fraud," and yet in such cases courts nevertheless apply a preponderance of the evidence standard. *See, e.g., FTC v. Renaissance Fine Arts, Ltd.*, 1994 WL 543048, *8 (N.D. Ohio

1994) (finding, by preponderance of evidence, that defendants had violated Section 5 through "a lucrative scheme to defraud"); *In re Amrep Corp.*, 102 F.T.C. 1362, 1640-41 (1983) (applying preponderance standard to practices described as "land sale fraud"). *See also Herman & MacLean*, 459 U.S. at 387-91 (1983) (In securities fraud case, the Supreme Court declined "to depart from the preponderance of the evidence standard generally applicable in civil actions" and reversed the Fifth Circuit's application of the traditional fraud clear and convincing standard.).

Respondent argues that a heightened standard of proof is required in this case based on *Walker Process Equipment, Inc. v. Food Machinery & Chemical Corp.*, 382 U.S. 172 (1965) and its progeny. RPHRB at 5 ("The crux of the anticompetitive conduct alleged here – the failure to disclose material information and the bad faith enforcement of patents against manufacturers practicing JEDEC standards – is identical to the conduct that was held to the clear and convincing standard of proof in the *Walker Process* line of cases."). The heightened burden of proof applied in *Walker Process* cases flows from the statutory presumption of patent validity (35 U.S.C. § 282 (2003)) and the duty of candor owed to the Patent and Trademark Office (*Charles Pfizer & Co., Inc. v. FTC*, 401 F.2d 574, 579 (6th Cir. 1968) (patent applicant "stood before the Patent Office in a confidential relationship and owed the obligation of frank and truthful disclosure")). "The road to the Patent Office is so tortuous and patent litigation is usually so complex, that 'knowing and willful fraud' as the term is used in *Walker*, can mean no less than clear, convincing proof of intentional fraud involving affirmative dishonesty . . . ." *Cataphote Corp. v. DeSoto Chemical Coatings, Inc.*, 450 F.2d 769, 772 (9th Cir. 1971).

Respondent's argument, however, is unpersuasive. There is a fundamental difference between the failure to disclose material information to the Patent Office, to whom a duty of candor is owed, and the failure to disclose information to competitors, as

alleged here. Thus, in this case, which Complaint Counsel characterize as based on antitrust theories, where the Complaint does not allege conduct involving "knowing and willful fraud," and where the Complaint does not allege fraud on the patent office, the standard of clear and convincing evidence is not appropriate.

Respondent also argues that the remedy proposed in the Complaint mandates a heightened level of scrutiny. The Notice of Contemplated Relief proposes "requiring Respondent to cease and desist all efforts it has undertaken by any means . . . through or in which Respondent has asserted that any person or entity, by manufacturing, selling, or otherwise using JEDEC-compliant SDRAM and DDR SDRAM technology (including future variations of JEDEC-compliant SDRAM and DDR SDRAM technology), infringes any of Respondent's current or future United States patents that claim priority back to U.S. Patent Application Number 07/510,898 filed on April 18, 1990 or any other U.S. Patent Application filed before June 17, 1996." ¶ 1. The Notice of Contemplated Relief also proposes that a cease and desist order prohibit Respondent from undertaking any new efforts to enforce current or future domestic or foreign patents that claim priority back to U.S. Patent Application Number 07/510,898 or any other patent application filed before June 17, 1996. ¶¶ 2-4. As set forth below, Complaint Counsel have not met their burden of proving liability on any of the violations alleged. Because of this finding on liability, no determination on remedy is made. Consequently, whether the remedy sought would mandate a heightened burden of proof need not be determined.

For these reasons, the government's case in this proceeding shall be adjudicated under the preponderance of evidence standard.

B. The Adverse Presumptions Are Not Material to the Disposition of the Case

In the Order On Complaint Counsel's Motions For Default Judgment And For Oral Argument, issued February 26, 2003, seven rebuttable adverse presumptions were imposed against Respondent. ("February 26, 2003 Order"). The February 26, 2003 Order was issued to resolve Complaint Counsel's motion for default judgment relating to Respondent's destruction of evidence. In that Order, the Court determined that "[w]hen Rambus instituted its document retention policy in 1998, it did so, in part, for the purpose of getting rid of documents that might be harmful" in future anticipated litigation involving "its JEDEC related patents." February 26, 2003 Order at 5 (internal quotations omitted). Moreover, this Court has expressed "significant and ongoing concerns about the Respondent directing its employees to conduct a wholesale destruction of documents and failing to create an inventory of what was destroyed." Order Denying Complaint Counsel's Motion for Additional Adverse Inferences and Other Appropriate Relief, issued April 15, 2003, at 4. The Court further indicated that the spoliation issue is not "closed to future reconsideration *after trial*." *Id.* at 4 n.2 (emphasis in original).

While the Commission will not tolerate spoliation efforts affecting its Part 3 administrative proceedings, the document destruction issue in this case, based on the conclusions reached herein, does not warrant the Court's continued attention. Rambus's conduct in this regard is, at best, troublesome. In a different cause of action, the Court might well have sanctioned Rambus for having deprived Complaint Counsel of their ability to present the merits of the case and thereby prejudicing Complaint Counsel and the adjudicative process. *See, e.g., Anderson v. Cryovac, Inc.*, 862 F.2d 910, 925 (1st Cir. 1988).

However, the process here has not been prejudiced as there is no indication that any documents, relevant and material to the

disposition of the issues in this case, were destroyed. In fact, Complaint Counsel noted that the record shows "an unusual degree of visibility into the precise nature of Rambus's conduct." (Opening Statement, Tr. 15). Moreover, as discussed below, none of the adverse presumptions are material to the disposition of the case.

1. The First and Second Adverse Presumptions Are Moot

The first presumption entered was that "Rambus knew or should have known from its pre-1996 participation in JEDEC that developing JEDEC standards would require the use of patents held or applied for by Rambus." February 26, 2003 Order at 9. The evidence shows that even if Rambus knew that developing JEDEC standards would require the use of Rambus patents, Rambus was not required to disclose those patents or applications, as the disclosure of intellectual property was voluntary. F. 766-71. Therefore, the presumption is moot.

The second presumption was that "Rambus never disclosed to other JEDEC participants the existence of these patents." February 26, 2003 Order at 9. The evidence, as described throughout this decision, shows that Rambus, through its conduct, raised sufficient red flags to put members of JEDEC and others on notice that there were patent applications pending, and that members of JEDEC, in fact, were well aware that Rambus sought to make intellectual property claims on the relevant technology. *E.g.*, F. 786-806. The evidentiary record in this case is replete with instances where participants in JEDEC were thoroughly familiar with Rambus's intellectual property rights and acted despite this knowledge. F. 1486-1518. Moreover, as the JEDEC disclosure responsibility is voluntary, this presumption, like the first, is rendered moot.

2. The Five Remaining Adverse Presumptions Are Not Relevant to Any Material Issues

The five remaining adverse presumptions – Rambus knew that its failure to disclose the existence of these patents to the JEDEC participants could serve to equitably estop Rambus from enforcing its patents as to other JEDEC participants; Rambus knew or should have known from its participation in JEDEC that litigation over the enforcement of its patents was reasonably foreseeable; Rambus provided inadequate guidance to its employees as to which documents should be retained and which documents could be discarded as part of its corporate document retention program; Rambus's corporate document retention program specifically failed to direct its employees to retain documents that could be relevant to any foreseeable litigation; and Rambus's corporate document retention program specifically failed to require employees to create and maintain a log of the documents purged pursuant to the program – are not relevant to any of the issues that remain to be decided. *See infra* Section II.

3. A "Missing Witness" Inference Is Not Appropriate

Complaint Counsel also contend that they are entitled to a "missing witness" inference because Respondent chose not to call Rambus executives William Davidow, Geoff Tate, or David Mooring to testify live during its case-in-chief, but instead relied on prior recorded testimony. Complaint Counsel and Respondent each listed Davidow, Tate, and Mooring as trial witnesses. During their case-in-chief, Complaint Counsel presented prior recorded testimony from each of these individuals.

None of the cases cited by Complaint Counsel in support of their request for a missing witness inference involved a situation where the parties actually introduced deposition testimony from the missing witnesses. This distinction is critical, for when witnesses testify at trial by way of deposition – as Davidow, Tate, and Mooring did – they are not "missing." *Bogosian v.*

Woloohojian Realty Corp., 323 F.3d 55, 67 n.10 (1st Cir. 2003) (individuals "were not 'missing witnesses' at all, since their depositions were admitted at trial"); *Boehringer Ingelheim Vetmedica, Inc. v. Schering-Plough Corp.*, 106 F. Supp.2d 667, 694 n.14 (D.N.J. 2000) ("By offering their deposition testimony instead of pursuing their live testimony . . . Schering . . . should not now be permitted to benefit from a negative inference be[ing] drawn against Boehringer."). *See also Oxman v. WLS-TV*, 12 F.3d 652, 661 (7th Cir. 1993) (holding that a defendant's decision not to call two witnesses did not justify a missing witness inference because the plaintiff, by using the deposition process, could "have ensured that their testimony was presented" at trial).

The missing witness inference is not appropriate under these facts, where Complaint Counsel deposed the witnesses and chose to present testimony from the witnesses via deposition. *See Jones v. Otis Elevator Co.*, 861 F.2d 655, 659 (11th Cir. 1988) (questioning the soundness of the missing witness inference); *Cameo Convalescent Center, Inc. v. Senn*, 738 F.2d 836, 844 (7th Cir. 1984) ("the justification for the missing witness instruction diminishes with the availability of the tools of discovery"). Indeed, in their Proposed Findings of Fact, Complaint Counsel cite to Davidow's deposition to support twenty-three of their proposed findings; Tate's, to support nine; and Mooring's, to support fifteen. CCPFF 88, 89, 703, 735, 736, 749, 925, 927, 937, 938, 941, 975, 1064, 1073, 1089, 1241, 1676, 1682, 1706, 1714, 1751, 1756, 1822, 1827, 1851, 1869-72, 1875, 1916, 1920, 1952, 1977, 1978, 1980, 1984, 1992, 1994, 2001, 2025, 2029, 2039, 2103, 2104, and 3213. Having failed to establish entitlement to the inference, Complaint Counsel's request to allow it is denied.

C. The Infineon Litigation

Rambus filed a patent infringement suit against Infineon Technologies, AG ("Infineon") in the United States District Court for the Eastern District of Virginia. *Rambus Inc. v. Infineon Technologies AG*, 164 F. Supp.2d 743 (E.D. Va. 2001), *aff'd in*

part, vacated in part, rev'd in part, 318 F.3d 1081 (Fed. Cir. 2003), *cert. denied*, 124 S. Ct. 227 (2003). Infineon filed counterclaims, including an allegation that Rambus committed fraud by failing to disclose to JEDEC patents and patent applications held by Rambus that allegedly related to Synchronous Dynamic Random Access Memory ("SDRAM") and the Double Data Rate SDRAM ("DDR SDRAM") standards adopted by JEDEC. 164 F. Supp.2d at 746.

At the conclusion of a two and one-half week trial, the jury found Rambus liable for committing actual and constructive fraud in its conduct at JEDEC with respect to both the SDRAM and DDR SDRAM standards adopted by JEDEC. *Id.* at 747. Rambus moved for judgment as a matter of law ("JMOL"). *Id.* at 746. The district court granted Rambus's JMOL and set aside the fraud verdict for DDR SDRAM on grounds that because the standard setting process for DDR SDRAM did not actually begin until after Rambus had left JEDEC, Rambus had had no duty to disclose. *Id.* at 765-66. The district court denied Rambus's JMOL and let stand the jury finding that Rambus committed fraud in its conduct at JEDEC with respect to the SDRAM standards adopted by JEDEC. *Id.* at 747.

On appeal to the Court of Appeals for the Federal Circuit, the Federal Circuit upheld the district court's grant of JMOL that set aside the fraud verdict on the DDR SDRAM standards and reversed the district court's denial of JMOL that let the fraud verdict stand on the SDRAM standards. *Rambus Inc. v. Infineon Technologies AG*, 318 F.3d 1081, 1084 (Fed. Cir. 2003), *cert. denied*, 124 S. Ct. 227 (2003). With respect to the DDR SDRAM standards, the Federal Circuit held that Infineon did not show that Rambus had a duty to disclose before the DDR-SDRAM standard setting process began, thus the district court properly granted JMOL of no fraud in Rambus's favor. *Id.* at 1105. With respect to the SDRAM standards, the Federal Circuit held "substantial evidence does not support the jury's verdict that Rambus breached its duties under the EIA/JEDEC policy." *Id.* at 1105.

D. Jurisdiction

The Complaint charges Respondent with violations of Section 5 of the FTC Act. 15 U.S.C. § 45. Section 5 of the FTC Act gives the Commission jurisdiction to prevent unfair methods of competition by "persons, partnerships, or corporations." 15 U.S.C. § 45. Respondent is a corporation engaged in the licensing of intellectual property. F. 60. Respondent designs, develops, licenses, and markets high-speed chip connection technology to enhance the performance of computers, consumer electronics, and communications systems. F. 60. The Commission has jurisdiction over acts or practices "in or affecting commerce," providing that their effect on commerce is substantial. *McLain v. Real Estate Bd. of New Orleans, Inc.*, 444 U.S. 232, 241-42 (1980); *Hospital Bldg. Co. v. Trs. of Rex Hosp.*, 425 U.S. 738, 745-46 (1976). Respondent's challenged activities relating to the licensing of intellectual property have an obvious nexus to interstate commerce. F. 58-66. Accordingly, the Commission has jurisdiction over Respondent and the subject matter of this proceeding.

II. OVERVIEW OF VIOLATIONS ALLEGED

Before turning to an analysis of the evidence bearing on liability, this section provides an overview of the violations alleged. Complaint Counsel have asserted three separate violations. Counts I and II set forth Sherman Act based claims of monopolization and attempted monopolization similar to those arising under 15 U.S.C. § 2. Count III sets forth a claim of unfair methods of competition which arises under Section 5 of the FTC Act, 15 U.S.C. § 45.

Count I, monopolization, requires the possession of monopoly power in the relevant markets and the willful acquisition or maintenance of that power. *United States v. Grinnell Corp.*, 384 U.S. 563, 570-71 (1966). "A firm violates § 2 only when it

acquires or maintains, or attempts to acquire or maintain, a monopoly by engaging in exclusionary conduct." *United States v. Microsoft Corp.*, 253 F.3d 34, 58 (D.C. Cir. 2001). Further, the offense of monopolization requires a showing that respondent's acquisition of power caused unreasonable exclusionary or anticompetitive effects. *Trans Sport, Inc. v. Starter Sportswear, Inc.*, 964 F.2d 186, 188 (2d Cir. 1992).

Count II, attempted monopolization, requires proof of three elements: (1) exclusionary or anticompetitive conduct; (2) specific intent to monopolize; and (3) a dangerous probability of achieving monopoly power. *Spectrum Sports, Inc. v. McQuillan*, 506 U.S. 447, 456 (1993).

Count III, unfair methods of competition, is alleged in the Complaint in this case to entail the willful engagement in a pattern of anticompetitive and exclusionary acts whereby Respondent unreasonably restrained trade in the relevant markets. Complaint ¶ 124. Complaint Counsel describe the elements of Count III as follows:

> [t]his claim differs from the monopolization claim (Count I) principally in that there is no need to demonstrate actual monopoly power – proof of market power and material adverse effects on competition will suffice. The unfair methods of competition claim differs from the attempted monopolization claim (Count II) in two respects: (1) it requires proof of actual (as opposed to probable) adverse effects on competition, albeit not necessarily rising to the level of monopolization; and (2) in order to establish liability for unfair methods of competition, specific intent need not be shown.

CCPHB at 19. Thus, the unfair methods of competition claim that Complaint Counsel set out to prove requires: (1) willful

engagement of anticompetitive and exclusionary acts; (2) market power; and (3) material adverse effects on competition. Complaint ¶ 124; CCPHB at 18-19.

The section that follows analyzes each of the elements necessary to support the violations alleged and whether Complaint Counsel have presented sufficient evidence to prove liability. The elements of liability are: monopoly power, exclusionary conduct, intent, causation, and anticompetitive effects. The following section also analyzes the theory of liability that Complaint Counsel assert serves as a basis for all three of the alleged violations: Respondent's "pattern of anticompetitive acts and practices." In addition, the following section includes an analysis of the economic evidence and Complaint Counsel's theory of lock in.

III. ELEMENTS OF LIABILITY

A. Possession of Monopoly Power in the Relevant Markets

1. Relevant Markets

Establishing the relevant market is the first step in assessing whether a respondent possesses monopoly power. *Spectrum Sports*, 506 U.S. at 455-56 (to establish monopolization or attempted monopolization, it is "necessary to appraise the exclusionary power of the illegal patent claim in terms of the relevant market for the product involved") (citations omitted). "The purpose of defining a relevant market is to identify a market in which market power might be exercised and competition thereby diminished." *In re Coca-Cola Bottling Co.*, 118 F.T.C. 452, 540 (1994). Complaint Counsel carry the burden of describing a well-defined relevant market, both geographically and by product. *H.J., Inc. v. Int'l Tel. & Tel.*, 867 F.2d 1531, 1537 (8th Cir. 1989).

a. Geographic Market

The relevant geographic market is the region "in which the seller operates, and to which the purchaser can practicably turn for supplies." *Tampa Elec. Co. v. Nashville Coal Co.*, 365 U.S. 320, 327 (1961); *Re/Max Int'l, Inc. v. Realty One, Inc.*, 173 F.3d 995, 1016 (6th Cir. 1999) (a geographic market is defined as an area of effective competition or the locale in which consumers can turn for alternative sources of supply).

Technologies, such as those described in the Complaint as the relevant product markets, tend to be licensed worldwide, tend to flow across national borders, have negligible transportation costs, and tend to be worldwide markets. F. 1017. Buyers of the relevant products typically do not care about the geographic source of the technology. F. 1017. The products downstream from the relevant products are produced and used worldwide. F. 1017. Therefore, the geographic market in this case is the world. F. 1016.

b. Product Markets

The relevant product market is "composed of products that have reasonable interchangeability for the purposes for which they are produced – price, use and qualities considered." *United States v. E.I. du Pont de Nemours & Co.*, 351 U.S. 377, 404 (1966). "In defining the relevant product market, the courts and the Commission generally examine what products are reasonable substitutes for one another." *In re Int'l Assoc. of Conference Interpreters*, 123 F.T.C. 465, 640 (1997).

The relevant product markets at issue here involve technologies that are incorporated in DRAM for use in current and recent-generation personal computers and other electronic memory devices. See F. 1010-15. Each market consists of a type of technology that addresses a specific aspect of memory design and operation. The four markets, described more fully in the Findings of Fact, are the latency technology market, the burst

length technology market, the data acceleration technology market, and the clock synchronization technology market. F. 1013. In addition, the Complaint describes a cluster market of synchronous DRAM technologies. F. 1014. A cluster market can be established if (1) there is only one real source of market power in each of the individual markets, or (2) the defendant has the same market share, competitors, and barriers to entry in each market. HERBERT HOVENKAMP, FEDERAL ANTITRUST POLICY 102 (2d ed. 1999); *see United States v. Philadelphia National Bank*, 374 U.S. 321, 356 (1963) (cluster of banking services constituted relevant market); *United States v. Central State Bank*, 817 F.2d 22, 23-24 (6th Cir. 1987) (same). Rambus's economic experts have not contested Complaint Counsel's market definitions. F. 1015. Accordingly, Complaint Counsel have established the relevant product markets.

2. Monopoly Power

Monopoly power is defined as "the power to control prices or exclude competition." *E.I. du Pont*, 351 U.S. at 391; *Aspen Skiing Co. v. Aspen Highlands Skiing Corp.*, 472 U.S. 585, 596, n.20 (1985). There are two ways to establish monopoly power. "The first is by presenting direct evidence of actual control over prices or the actual exclusion of competitors." *Re/Max Int'l, Inc. v. Realty One, Inc.*, 173 F.3d 995, 1016 (6th Cir. 1999) (citations omitted). The second way to establish that a respondent has monopoly power is by showing a high market share within a defined market. *Id.* (citations omitted). "The existence of such power ordinarily may be inferred from the predominant share of the market." *Grinnell*, 384 U.S. at 571; *United States v. Microsoft Corp.*, 253 F.3d 34, 51 (D.C. Cir. 2001) ("monopoly power may be inferred from a firm's possession of a dominant share of a relevant market that is protected by entry barriers"). Barriers to entry include patents. *Image Technical Services, Inc. v. Eastman Kodak Co.*, 125 F.3d 1195, 1208 (9th Cir. 1997); *Axis S.p.A. v. Micafil, Inc.*, 870 F.2d 1105, 1107 (6th Cir. 1989).

This element requires only that monopoly power exists, not that it be exercised. In *American Tobacco Co. v. United States*, 328 U.S. 781 (1946), the Supreme Court held "that the material consideration in determining whether a monopoly exists is not that prices are raised and that competition actually is excluded but that power exists to raise prices or to exclude competition when it is desired to do so." *Id.* at 811.

Complaint Counsel have demonstrated that Respondent has monopoly power in the relevant markets. Rambus's market share of over ninety percent in the relevant markets (F. 1020-21), where there are barriers to entry (*see* F. 94-95), demonstrates monopoly power. "[T]he existence of [monopoly] power ordinarily may be inferred from the predominant share of the market." *Grinnell*, 384 U.S. at 571 (eighty-seven percent of the relevant market left no doubt that defendants had monopoly power). In addition, Rambus has asserted that certain of its patents cover features specified in JEDEC's SDRAM and DDR SDRAM standards, including the four "Rambus" technologies. F. 1022-29. When the government has granted the seller "a patent or similar monopoly over a product, it is fair to presume that the inability to buy the product elsewhere gives the seller market power." *Jefferson Parish Hosp. Dist. No. 2 v. Hyde*, 466 U.S. 2, 16 (1984).

Complaint Counsel have demonstrated that Respondent has acquired monopoly power in the relevant markets. However, as discussed in the following sections, Complaint Counsel have not demonstrated that Respondent's acquisition or maintenance of monopoly power was unlawful.

B. No Pattern of Anticompetitive Acts and Practices

Complaint Counsel assert that the theory of liability that serves as the basis for all three of their claims is the alleged "pattern of anticompetitive acts and practices" including Respondent's concealment of patent-related information "in violation of JEDEC's own operating rules and procedures," as well as "other bad-faith, deceptive conduct." CCPHB at 19

(quoting Complaint ¶¶ 1-2). The pattern of bad-faith, deceptive acts alleged in the Complaint are Respondent's failure to disclose material, patent-related information to JEDEC and Respondent's affirmative misleading statements and actions through which Respondent (before and after withdrawing from JEDEC) purposefully sought to convey to JEDEC's members the impression that Respondent did not possess intellectual property rights that would, or might, be infringed by JEDEC's SDRAM and DDR SDRAM standards. CCPHB at 19. The Complaint alleges that Respondent's omissions and misrepresentations violated or subverted: (1) JEDEC's patent disclosure rules; (2) JEDEC's "'basic rule' that standardization programs conducted by the organization 'shall not be proposed for or indirectly result in . . . restricting competition, giving a competitive advantage to any manufacturer, [or] excluding competitors from the market'"; and (3) a variety of other policies, rules, and procedures through which JEDEC sought "to avoid, where possible, the incorporation of patented technologies into its published standards, or at a minimum to ensure that such technologies, if incorporated, will be available to be licensed on royalty-free or otherwise reasonable and non-discriminatory terms." CCPHB at 20.

In this case, to evaluate whether Respondent is liable under Section 5 of the FTC Act for the alleged pattern of anticompetitive acts and practices requires the following determinations: (1) whether the conduct alleged by Complaint Counsel states a legally cognizable cause of action under Section 5 of the FTC Act; (2) whether JEDEC's rules and policies created clear and unambiguous standards upon which liability could be based; (3) whether the evidence presented demonstrates that Respondent's conduct amounted to a pattern of anticompetitive acts and practices; (4) whether the evidence presented demonstrates that Respondent made affirmative, misleading statements to JEDEC; and (5) whether Respondent's amendments to claims to broaden its patent applications were improper.

1. The Legal Theory Upon Which Complaint Counsel Challenge Respondent's Conduct Lacks a Reasonable Basis in Law

Section 5 of the FTC Act authorizes the Federal Trade Commission to define and proscribe "unfair methods of competition." 15 U.S.C. § 45(a)(1). Accordingly, the Commission may proscribe "conduct which, although not a violation of the letter of the antitrust laws, is close to a violation or is contrary to their spirit." *E.I. Du Pont de Nemours & Co. v. FTC*, 729 F.2d 128, 136-37 (2d Cir. 1984); *see also FTC v. Sperry & Hutchinson Co.*, 405 U.S. 233, 239 (1972); *Grand Union Co. v. FTC*, 300 F.2d 92, 98-99 (2d Cir. 1962). The FTC Act empowers the Commission with broad authority to "declare trade practices unfair." *FTC v. Brown Shoe Co.*, 384 U.S. 316, 321 (1966).

While "Congress intentionally left development of the term 'unfair' to the Commission rather than attempting to define 'the many and variable unfair practices which prevail in commerce,'" the determination that conduct constitutes an unfair method of competition must have "a reasonable basis in law." *Atlantic Refining Co. v. FTC*, 381 U.S. 357, 369 (1965). *Accord Luria Bros. & Co. v. FTC*, 389 F.2d 847, 860 (3rd Cir. 1968). "[S]tandards for determining whether [conduct] is 'unfair' within the meaning of § 5 must be formulated to discriminate between normally acceptable business behavior and conduct that is unreasonable or unacceptable." *Du Pont*, 729 F.2d at 138. Complaint Counsel do not challenge Respondent's conduct as collusive, coercive, or predatory. Furthermore, as explained *infra* Section III.C, Complaint Counsel have not demonstrated that Respondent's conduct was exclusionary. Therefore, to prevail, Complaint Counsel must support their theory by some other "reasonable basis in law."

Complaint Counsel assert that, regardless of whether Respondent's actions violated JEDEC's rules or reflected a conscious effort to subvert the spirit and purpose of JEDEC's

open standards process, when such conduct results in the acquisition of monopoly power, a dangerous probability of monopolization, or material adverse effects of competition in a well-defined market, liability attaches under Section 5 of the FTC Act. CCPHB at 21-22. Complaint Counsel argue that "this is an antitrust case, arising under Section 5 of the FTC Act." CCPHB at 79. Complaint Counsel further assert that "the basis for imposing antitrust liability in these circumstances is well-established." CCPHB at 21. Despite this assertion, Complaint Counsel cite to only a single case, *Indian Head, Inc. v. Allied Tube & Conduit Corp.*, 817 F.2d 938 (2d Cir. 1987) ["*Indian Head*"], *aff'd, Allied Tube & Conduit Corp. v. Indian Head, Inc.* 486 U.S. 492 (1988) ["*Allied Tube*"], and to the consent decree entered in *In re Dell Computer Corp.*, 121 F.T.C. 616, 626, 1996 FTC LEXIS 291 (1996) for support. Complaint Counsel argue, under the authority of *Indian Head*, that JEDEC's "duty of good faith" provides a basis for liability in this case. (CCRB at 8-9).

The language upon which Complaint Counsel rely in *Indian Head* is the following statement by the Court of Appeals for the Second Circuit: "We refuse to permit a defendant to use its literal compliance with a standard-setting organization's rules as a shield to protect such conduct from antitrust liability." CCPHB at 21 (quoting *Indian Head*, 817 F.2d at 941). In *Indian Head*, the Second Circuit found that defendant conspired with other steel companies to take control of the standard setting organization. 817 F.2d at 497. Allegations of collusion or conspiracy or tampering with the voting process of JEDEC, however, are not presented by the instant Complaint. Moreover, unlike in *Indian Head*, the Complaint here does not challenge Respondent's activities in compliance with JEDEC's rules, but rather alleges that Respondent's lack of compliance with the rules should result in liability.

On appeal, the Supreme Court in *Allied Tube* upheld the jury verdict against members of the steel industry who conspired to pack the annual meeting with new members who had the sole

purpose of voting against inclusion of polyvinyl chloride conduit as an approved conduit in the National Electrical Code published by the National Fire Protection Association. 486 U.S. at 495. The association's board of directors, reviewing this vote, had found that, although the association's rules had been circumvented, the rules had not been violated. *Id.* at 497.

The Supreme Court rejected the argument that *Noerr-Pennington* immunity protected the steel industry activity without addressing the specific requirements of standard setting organizations under the Sherman Act stating:

> [a]lthough we do not here set forth the rules of antitrust liability governing the private standard-setting process, we hold that at least where, as here, an economically interested party exercises decisionmaking authority in formulating a product standard for a private association that comprises market participants, that party enjoys no *Noerr* immunity from any antitrust liability flowing from the effect the standard has of its own force in the marketplace.

Id. at 509-10. The Supreme Court noted that its "holding is expressly limited to cases where an 'economically interested party exercises decisionmaking authority in formulating a product standard for a private association that comprises market participants.'" *Id.* at 510 n.13.

The conduct challenged in this case differs greatly from that in *Allied Tube* in a number of essential ways. Here, Respondent did not exercise "decisionmaking authority" during its participation in JEDEC. To the contrary, Rambus did not propose or promote any technology and was not even permitted to present its proprietary Rambus DRAM ["RDRAM"] technology for consideration by the standardization committee. F. 824-25. Respondent only voted on four preliminary ballots relating to technologies proposed for the

SDRAM standard. F. 330. Rambus did not vote on the final set of SDRAM ballots. F. 330. Rambus was not even participating in JEDEC when JEDEC adopted the DDR standard. F. 968-82.

The antitrust implications of *Allied Tube* were expressly limited to the facts before it and cannot be read to imply a "duty of good faith" requiring disclosure of proprietary intellectual property solely by virtue of membership in a standard setting organization. Further, *Allied Tube* cannot be read to hold that violation of a standard setting organization's rules or policies forms a basis for antitrust liability.

Complaint Counsel rely also on the consent decree entered in *Dell*, 121 F.T.C. 616 (1996). Such reliance is misplaced. Consent decrees provide no precedential value. "[T]he circumstances surrounding . . . negotiated [consent decrees] are so different that they cannot be persuasively cited in a litigation context." *United States v. E.I. du Pont de Nemours & Co.*, 366 U.S. 316, 331 n.12 (1961). Indeed, the *Dell* consent decree acknowledges that the agreement is for settlement purposes only and does not constitute an admission of a law violation. *Dell*, 121 F.T.C. at 619.

Nevertheless, two cases have been found that cite to the *Dell* consent decree. The first, *Townshend v. Rockwell Int'l Corp.*, 2000 U.S. Dist. LEXIS 5070 (N.D. Cal. 2000), distinguished *Dell* on the facts presented. The second, *Intel Corp. v. VIA Technologies, Inc.*, 2001 WL 777085 (N.D. Cal. 2001), reserved judgment at the motion to dismiss stage on "whether *Dell*-type conduct . . . would be actionable under the Sherman Act" and on "whether a *Dell*-type theory is reconcilable with the statement of the Federal Circuit that "'in the absence of any indication of illegal tying, fraud in the Patent and Trade Office, or sham litigation, the patent holder may enforce the statutory rights to exclude others [under the patent] free from liability under the antitrust laws.'" *Intel*, 2001 WL 777085 at *6 (quoting *In re Independent Service Organizations Antitrust Litigation*, 203 F.3d

1322, 1327 (Fed. Cir. 2000)). The doubts expressed by the court in *Intel* apply with equal force to this case.

Moreover, even if the consent decree in *Dell* was persuasive authority, the facts are distinguishable. Dell participated in a Video Electronic Standards Association ("VESA") standard setting organization where, as part of the approval process, members certified in writing that they did not possess intellectual property rights that would infringe or conflict with the proposed standard. *Dell*, 121 F.T.C. at 617. On two occasions, Dell's representative to the body made such a certification, stating in writing that, to the best of his knowledge, "this proposal does not infringe on any trademarks, copyrights, or patents" that Dell possessed. *Id.* Thereafter, Dell sought to enforce a patent against companies that had implemented the standard after the standard became widely adopted into newly manufactured computers. *Id.* at 617-18.

In the Commission Statement accompanying the Dell consent agreement, the Commission points out that VESA's affirmative disclosure requirement differed from disclosure requirements of other standard setting organizations. *Id.* at 625. For example, the Commission specifically noted that "the VESA policy for dealing with proprietary standards is not very like ANSI's patent policy. ANSI does not require that companies provide a certification as to conflicting intellectual property rights. Therefore, its policy, unlike VESA's, does not create an expectation that there is no conflicting intellectual property." *Id.* at 625 n.6 (internal quotation omitted).

The language of the American National Standards Institute ("ANSI") patent policy was "essentially identical" to the Electronic Industries Association ("EIA")/JEDEC policy and the ANSI policy was circulated to JC 42.3 members in 1992 and 1994 because it provided insight into the EIA/JEDEC patent policy. F. 639-40. The ANSI patent policy guidelines "seek to encourage the early disclosure and identification of patents that may relate to

standards under development." F. 643. The ANSI policy, like the EIA/JEDEC policy, does not mandate disclosure of intellectual property and therefore, as the Commission stated in *Dell*, is substantially different from the policy which mandated disclosure in *Dell*.

Neither *Allied Tube* nor the consent decree entered in *Dell* provide a "reasonable basis" for finding liability under Section 5 of the FTC Act. No case has been cited to or was found holding that Section 5 of the FTC Act imposes a duty upon corporations that participate in standard setting organizations to comply with the rules of the standard setting organizations, to disclose their patent applications, or to act in good faith towards other members. Although Respondent's conduct may provide a basis for private causes of action, such as breach of contract, fraud, or equitable estoppel, no such duty is created by the provisions of the FTC Act. Concomitantly, the Federal Circuit in *Infineon* found that under the EIA/JEDEC policy statements, "[t]here is no indication that members ever legally agreed to disclose information." *Infineon*, 318 F.2d at 1098. With no such duty arising in law, the Court will not infer such a duty.

2. The Duties Upon Which Complaint Counsel Base Their Challenge Must Be Clear

Even if a cause of action exists under the FTC Act based upon a company's alleged anticompetitive conduct before a standard setting organization, to find liability based upon a participant's failure to comply with the organization's rules or policies or based upon a failure to disclose patents and patent applications requires a finding that Respondent was obligated to comply with those rules or policies or otherwise had a duty to disclose such information. As set forth below, any such obligation or duty must be clear and unambiguous to form the basis for antitrust liability or liability under Section 5 of the FTC Act.

Courts have repeatedly recognized the need for clarity of rules on which antitrust liability can be based. *E.g.*, *Concord v. Boston Edison Co.*, 915 F.2d 17, 22 (1st Cir. 1990); *International Distribution Centers, Inc. v. Walsh Trucking Co., Inc.*, 812 F.2d 786, 796 n.8 (2nd Cir. 1987) ("A major concern underlying antitrust jurisprudence lies in the fear of mistakenly attaching antitrust liability to conduct that in reality is the competitive activity the Sherman Act seeks to protect."). Where rules are ambiguous or indefinite, businesses are unfairly left to speculate whether their conduct will expose them to potential antitrust liability. In such situations, the ambiguity may result in a chilling effect on otherwise procompetitive conduct. *See Westman Comm'n Co. v. Hobart Int'l, Inc.*, 796 F.2d 1216, 1220 (10th Cir. 1986) ("if the antitrust laws applicable to vertical dealings are uncertain or inefficient, they are likely to have a chilling effect on beneficial, procompetitive market interaction").

Similarly, liability under Section 5 of the FTC Act must be based on clear standards. *Du Pont*, 729 F.2d at 139 ("The Commission owes a duty to define the conditions under which conduct claimed to facilitate price uniformity would be unfair so that businesses will have an inkling as to what they can lawfully do rather than be left in a state of complete unpredictability."); *Grand Union v. FTC*, 300 F.2d 92, 100 (2nd Cir. 1962) ("In this highly uncertain area of the law, [respondent] cannot be held to have known to a certainty that its part in the transactions was a violation of § 5.").

In the *Infineon* case, the Federal Circuit explained that a duty of disclosure must be clear and unambiguous if it is to support a fraud claim:

> [w]hen direct competitors participate in an open standards committee, their work necessitates a written patent policy with clear guidance on the committee's intellectual property position. A policy that does not define clearly what, when,

> how, and to whom the members must disclose does not provide a firm basis for the disclosure duty necessary for a fraud verdict.

Infineon, 318 F.3d at 1102. *See also Bank of Montreal v. Signet Bank*, 193 F.3d 818, 827 (4th Cir. 1999) ("Silence does not constitute concealment in the absence of a duty to disclose."). In addition, the patent-related equitable estoppel case law upon which Complaint Counsel rely holds that "silence alone will not create an estoppel unless there was a clear duty to speak, or somehow the patentee's continued silence reinforces the defendant's inference from the plaintiff's known acquiescence that the defendant will be unmolested." *A.C. Aukerman Co. v. R.L. Chaides Cons. Co.*, 960 F.2d 1020, 1043-44 (Fed. Cir. 1992) (internal citations omitted). This well-established reasoning similarly applies in assessing Complaint Counsel's allegations against Rambus in this case.

As set forth in the analysis below, JEDEC merely encouraged the disclosure of intellectual property and any duties Respondent may have had towards other JEDEC members were so unclear and ambiguous that they cannot form the basis for finding liability in this case.

3. The Evidence Presented at Trial Does Not Provide a Factual Basis for Finding a Pattern of Anticompetitive Acts and Practices

Complaint Counsel concede that the Complaint does not allege that Rambus's JEDEC-related patent disclosure obligation arises from antitrust law or from overriding principles of public policy. Complaint Counsel's Memorandum in Opposition to Respondent Rambus Inc.'s Motion for Summary Decision, March 25, 2003 at 6. Rather, Complaint Counsel argue that a duty to disclose intellectual property can be inferred from the duty of good faith found in the EIA Legal Guides, that it can be inferred from JEDEC's goal of developing open standards, and that it is

found in rules and policies as interpreted and explained by trial testimony. *Id.* at 11-25; CCPHB at 38-41, 54-55. To be enforceable, the duty must be clear and unambiguous.

As summarized below and as set forth in detail in the Findings of Fact, Complaint Counsel have not met their burden of demonstrating that Respondent was under a clear duty to disclose to JEDEC or its members its proprietary intellectual property, regardless of whether the alleged duty arises from good faith, open standards, or rules and policies. At most, the EIA/JEDEC patent policy encouraged the voluntary disclosure of essential patents when submitting committee ballots.

a. No Duty to Disclose Intellectual Property Based on Good Faith

The EIA Legal Guides do not support Complaint Counsel's contention that there was a good faith based duty imposed upon JEDEC members to disclose intellectual property. F. 587-91. It is apparent from the context of the language that the referenced "good faith duty" is not directed to individual members, but rather is a general directive to the administrators who "conduct" the EIA's standardization activities, directing them to adopt "policies and procedures which will assure fairness and unrestricted participation." F. 591. The duty of good faith found in the Legal Guides seeks to ensure that all participants are treated fairly and in accordance with the policies and practices of JEDEC. F. 588. It would be unreasonable to infer from this language an additional mandatory requirement that members disclose proprietary intellectual property, particularly when that duty is not found elsewhere in JEDEC or EIA manuals.

b. No Duty to Disclose Intellectual Property Based on Open Standards

The parties agree that one goal of JEDEC was to develop "open standards." RPHRB at 19. Complaint Counsel argue that

the concept of open standards includes "prohibiting the incorporation of patented technology into a standard unless the patent owner is willing to grant a license on reasonable terms.'" CCPHB at 39 (quoting *Amicus Curiae* Brief of JEDEC Solid State Technology Association in Support of [Infineon's] Petition for Rehearing and Rehearing *En Banc*). Respondent replies that the concept of "open standards" did not exclude the use of patented technology and that if JEDEC was committed to avoiding patented technology, then its purpose would be inconsistent with established antitrust principles. RPHRB at 19.

According to the EIA Legal Guides, standards "are proposed or adopted by EIA without regard to whether their proposal or adoption may in any way involve patents on articles, materials, or processes." F. 633. Indeed, the evidence demonstrates that "open standards" means that all relevant participants may participate in the development phase and that once standards are developed, the standards are available to everyone on a reasonable and nondiscriminatory basis. F. 600. Moreover, where JEDEC members were aware of a patent, they generally sought assurances for reasonable and nondiscriminatory ("RAND") terms from the patent owner. F. 601. As a matter of practice, patented technologies were regularly and knowingly included in JEDEC standards once RAND assurances were received. F. 604.

Refusing to include patented technology in industry standards may subject standard setting organizations to antitrust claims and denies consumers superior products. In 1985, the Commission filed a Complaint against a standard setting organization alleging violation of Section 5 of the FTC Act based on the organization's refusal to consider for standardization technology which was patented or manufactured by only one manufacturer. *In re American Society of Sanitary Engineering*, 106 F.T.C. 324; 1985 FTC LEXIS 20 (1985). In 1996, in its correspondence to the Commission regarding the *Dell* case, EIA recognized that by "allowing standards based on patents, American consumers are assured of standards that reflect the latest innovation and high

technology the great technical minds of this country can deliver. . . . [T]here is a positive and pro-competitive benefit to incorporating intellectual property in standards." F. 605.

There is therefore no basis in the facts of this case to infer a duty to disclose proprietary intellectual property based on JEDEC's goal of creating open standards – to do so would be contrary to the meaning given "open standards" by JEDEC members and could potentially run afoul of antitrust considerations.

c. No Duty to Disclose Intellectual Property Based on the EIA/JEDEC Patent Policy

To support their contention that the EIA/JEDEC policy required disclosure of intellectual property, Complaint Counsel rely on the language in JEP 21-I § 9.3.1 that the "Chairperson of any JEDEC committee, subcommittee, or working group must . . . call attention to the obligation of all participants to inform the meeting of any knowledge they may have of any patents, or pending patents, that might be involved in the work they are undertaking" and the language in JEP 21-I and other EIA/JEDEC manuals requiring the chairperson to ensure that no known patented technology was included in a JEDEC standard unless the committee received advance, written assurance from the intellectual property owner that it agreed to license either royalty free or on RAND terms. CCPHB at 40-41.

As an initial matter, it is important to note that JEP 21-H was in effect when Respondent joined JEDEC. F. 606. The only mention of intellectual property in JEP 21-H is that "JEDEC standards are adopted without regard to whether or not their adoption may involve patents on articles, materials or processes." F. 607. JEP 21-I was not published until October of 1993. F. 610. Respondent did not receive a copy of JEP 21-I until 1995. F. 629. It is not clear that JEP 21-I was ever formally adopted by JEDEC because there was no evidence that the manual received the EIA

Engineering Department Executive Council approval necessary to become effective. F. 627-28. In any event, the SDRAM standard was balloted *prior* to publication of JEP 21-I, thereby casting doubt on what effect, if any, JEP 21-I could have pertaining to disclosure obligations under the SDRAM standard. *See* F. 351, 610.

Moreover, JEP 21-I section 9.3.1 does not impose a disclosure duty. Instead it advises committee chairs to call attention to the alleged duty. It goes on to say that "Appendix E (Legal Guides Summary) provides copies of viewgraphs that should be used at the beginning of the meeting to satisfy this requirement." F. 616. The viewgraphs in appendix E, which are substantially the same as EIA EP-7-A section 3.4, do not impose or even mention an obligation to disclose intellectual property, but rather explain the process for obtaining RAND assurances. F. 618-20. At most, JEP 21-I created ambiguity; its indirect reference to an otherwise undefined duty cannot form the basis of an antitrust claim. *See* F. 744-47.

Throughout the relevant time period, JEDEC was an unincorporated subpart or activity within EIA. F. 222, 740. The EIA Legal Guides governed all EIA engineering standardization and related programs and were required to be followed by JEDEC members. F. 740, 743. Indeed, the patent policy is often referred to as the "EIA/JEDEC" policy without distinguishing between the organizations. *E.g.*, F. 622. The EIA Legal Guides and style manuals do not contain any reference to any obligation to disclose intellectual property. *See* F. 633-38. Rather, these manuals merely spell out the procedures for including known patented technologies in standards. F. 633-38.

Respondent's actions must be viewed in light of JEDEC's policies as they existed during the relevant time period. As the Federal Circuit notes in *Infineon*, "after-the-fact morphing of a vague, loosely defined policy to capture actions not within the actual scope of that policy . . . would chill participation in open

standard-setting bodies." 318 F.3d at 1102 n.10. Indeed, standard setting organizations, in their *amicus* briefs to the Supreme Court in the *Infineon* case, refer to the need for courts to interpret the patent policies as developed and *written* by standard setting organizations. *Amicus Curiae* Brief of JEDEC Solid State Technology Association in Support of [Infineon's] Petition for Rehearing and Rehearing *En Banc* at 14; Brief of The Commonwealth of Virginia, *et al.* as *Amici Curiae* in Support of [Infineon] at 2, 8, 13-14. The EIA/JEDEC policy, both in its express written terms and practice, merely encouraged the voluntary disclosure of patents prior to submission of committee ballots. F. 587-785.

The contemporaneous evidence in this proceeding conflicted with trial testimony which, at times, conflicted with other trial testimony (sometimes by the same witness). In weighing this conflicting evidence, greater weight was given to contemporaneous documents than to the after-the-fact testimony by interested witnesses. *See United States v. United States Gypsum Co.*, 333 U.S. 364, 395 (1947) (where trial testimony is in conflict with contemporaneous documents, the trial testimony is entitled to little weight); *see also United States v. International Business Machines Corp.*, 1974 WL 899, *2 (S.D.N.Y. 1974) (The *Gypsum* rule "instructs that when oral testimony is contradicted by contemporaneous documents the trier of fact should give little weight to the oral testimony.").

The *Gypsum* rule is especially appropriate here, where witnesses would directly benefit from the outcome of this litigation because they work for companies that either manufacture or use DRAMs that may infringe Rambus's patents, work for entities that are entirely controlled by DRAM manufacturers, or are committed to developing technologies that will compete with Rambus's technologies.

i. Disclosure of Intellectual Property Under the EIA/JEDEC Patent Policy Was Voluntary

There is overwhelming evidence from contemporaneous documents, the conduct of participants, and trial testimony that the disclosure of intellectual property interests was encouraged and voluntary, not required or mandatory. The Federal Circuit in *Infineon* found "no language – in the membership application or manual excerpts – expressly requiring members to disclose information." *Infineon*, 318 F.3d at 1098. When questioned in closing arguments, Complaint Counsel pointed only to the language of JEP 21-I and after-the-fact trial testimony to support their argument that there was a duty to disclose intellectual property based on the policies and procedures of JEDEC. Closing Argument, Tr. 11760-62. As summarized below (and detailed extensively in the Findings), the manuals which discuss the patent policy, a March 1994 memorandum by JEDEC's secretary, the EIA's comments to the FTC in connection with the *Dell* consent decree, JEDEC's internal memoranda, the ANSI patent policy guidelines, the actions of other JEDEC members in not disclosing patents and JEDEC's reaction thereto, the ballot for voting on technology, and the patent tracking list, are all evidence that disclosure of intellectual property under the EIA/JEDEC patent policy was not mandatory.

The manuals which discuss the EIA/JEDEC patent policy include: JEP 21-H, JEP 21-I, EIA Legal Guides, EP-3-F and EP-7-A. None of these manuals require disclosure of intellectual property; rather, they provide merely a general statement that patented items are not favored and spell out detailed requirements for including known patents in JEDEC standards including the procedure for obtaining RAND assurances. F. 609, 631-32, 634, 638.

In March 1994, JEDEC Secretary Ken McGhee sent a memorandum to JC 42 Chairman Jim Townsend stating that JEDEC's legal counsel said:

> he didn't think it was a good idea to *require* people at JEDEC standards meetings to sign a document assuring anything about their company's patent rights for the following reasons:
>
> 1) It would have a chilling effect at future meetings
> 2) The general assurances wouldn't be worth that much anyway
> 3) It needs to come from a VP or higher within the company–engineers can't sign such documents
> 4) It would need to be done at each meeting slowing down the business at hand.

F. 671 (emphasis added). This memorandum would not make sense if members were *already* required to disclose intellectual property as a result of JEP 21-I or any other rules or policies of JEDEC. In addition, it explains why such a mandatory policy was *not* adopted by JEDEC.

In connection with the *Dell* consent decree, the EIA submitted comments to the Commission which, in part, described the EIA patent policy. In the correspondence, EIA states clearly and unequivocally that they "encourage the early, voluntary disclosure of patents." F. 674. Commission Secretary Donald Clark responded, confirming his understanding that EIA "encourage[s] the early, voluntary disclosure of patents, but do[es] not require a certification by participating companies regarding potentially conflicting patent interests." F. 676.

In 2000, JEDEC Secretary McGhee wrote in an email to JEDEC members that disclosure of patent applications, or pending

patents, is "not required" by JEDEC, even though it is "encouraged." F. 684-85. The "spirit of the law" is to disclose patent applications even though disclosure "cannot be required of members," wrote McGhee. F. 684-85.

ANSI is an umbrella organization that accredits various standard setting organizations, including the EIA. The ANSI Patent Policy Guidelines were circulated to JC 42.3 members in 1992 and 1994 because they "provided insight into the proper interpretation of the EIA and JEDEC patent policy." F. 639-40. The ANSI guidelines "encourage the early disclosure and identification of patents that may relate to standards under development." F. 643.

Gordon Kelley, IBM representative and JC 42.3 committee chair, announced on a number of occasions, as recorded by the meeting minutes, that IBM would not disclose intellectual property and, indeed, from December 1993 to December 1995, no IBM patents or patent applications were added to the patent tracking list. F. 691-94. According to IBM, "[i]t is up to the user of the standard to discover which patents apply." F. 693; *see* F. 692. IBM's statements coincide with the publication of JEP 21-I and may have been an attempt to assure that IBM would not be liable for any undisclosed patents which ultimately became part of JEDEC standards. There is no record evidence that IBM was sanctioned for its refusal to disclose the company's intellectual property as would have been expected had disclosure been a mandatory requirement for JEDEC members. F. 698.

Hewlett-Packard similarly indicated that it would not be disclosing intellectual property. F. 699. Again, there is no evidence that Hewlett-Packard was sanctioned for its refusal to disclose the company's intellectual property, as would have been expected had this been a mandatory requirement for JEDEC members. F. 700.

In contrast, two other companies *were* sanctioned for failing to disclose intellectual property. In both cases, the companies involved were not merely participants, as Rambus was, but had actually presented and promoted their technology for inclusion in a standard. In the first case, JEDEC chose to standardize a different technology after SEEQ refused to provide RAND assurances. F. 686-88. In the second case, there was private litigation between Texas Instruments ["TI"] and the alleged infringer in which it was ultimately found that the patent was not violated. F. 701-07.

The ballot for voting on which technology to include in standards uses the word "please" to request the disclosure of patents. In contrast, the same ballot employs the term "MANDATORY" to describe the requirement of a member to state the "detailed reason(s) for . . . disapproval" of the content of a ballot topic. F. 654-55. When this language was first added to the ballots in 1989, there was a discussion in a JEDEC meeting of the purpose of the new ballot language. The minutes from that discussion state: "TI was concerned that Committee members could be held liable if they didn't inform Committee members correctly on patent matters. Committee responded that the question was added on ballot voting sheets for information only and was not going to be checked to see who said what." F. 656. It is clear from the plain language of the committee ballot that a "no" vote mandates an explanation, while patent disclosure is requested only on a voluntary basis. F. 658

The patent tracking list maintained by Chairman Townsend was an incomplete list of the patents or patent applications disclosed to JEDEC. F. 666-68. Indeed there was no complete list of patents disclosed. If mandatory disclosure had been central to obtaining appropriate standards, there would have been a formal and accurate method of tracking disclosures, similar to the explicit and detailed requirements for submitting RAND assurances. *See* F. 612 (JEP 21-I requiring submission in writing of a letter to the General Counsel prior to or at the time of balloting). Thus, the

informal and unofficial patent tracking list cannot form the basis for a mandatory duty.

Even witnesses who testified that there was an obligation to disclose patent applications failed to act in a manner consistent with their testimony. For example, JEDEC Chairman Desi Rhoden was a named inventor of a patent covering the SLDRAM standard. F. 713. He failed to disclose the patent application to JEDEC. F. 717. At trial, however, Rhoden testified that even non-members, including visiting guest scientists or engineers from foreign countries, were obligated to disclose their company's patents and patent applications that were related in some general way to a subject being discussed at JEDEC. F. 717. Under the *Gypsum* rule, Rhoden's testimony, which was inconsistent with his actions, can be accorded little, if any weight. *See Gypsum*, 333 U.S. at 395.

ii. The EIA/JEDEC Patent Policy Was Limited to Issued Patents, Not to Patent Applications or Intentions to File

The EIA/JEDEC patent policy encouraged the disclosure of patents, not patent applications or intentions to file patent applications. The minutes of the February 2000 meeting of the JEDEC Board of Directors state unequivocally that disclosure of patent applications is "not required under JEDEC bylaws." F. 773. A few days after the meeting, JEDEC Secretary McGhee explained to the members of JEDEC 42.4 that the disclosure of patent applications went "one step beyond" the patent policy. F. 773. These clear and unambiguous official statements of policy cannot be reconciled with Complaint Counsel's contention that JEDEC had a mandatory policy requiring the disclosure of patent applications or intentions to file patent applications. Indeed, the Federal Circuit in *Infineon* specifically concluded that the EIA/JEDEC disclosure policy did not extend "to a member's plans or intentions." *Infineon*, 318 F.3d at 1102.

There is more than just contemporaneous written evidence that conflicts with Complaint Counsel's after-the-fact construction of the patent policy; actual conduct of JEDEC participants also contradicts that construction. In addition to the actions of Desi Rhoden, discussed in F. 713-17, there were other instances in which named inventors were present during a JEDEC meeting while proposals relating to their patent applications were being discussed, but did not disclose those applications. F. 701-17.

The most that the record evidence can be understood to support is an argument that *presenters* were required to disclose patent applications that related to technologies that they were asking that JEDEC standardize. F. 752, 774. This is consistent with the focus in *Allied Tube* on actions of economially interested companies which exercise control over the decisionmaking process. *Allied Tube*, 486 U.S. at 509-10. Rambus, which was prohibited from presenting its technology (F. 824-25), would not be obligated to disclose under such a policy.

In sum, the record shows that JEDEC did not require disclosure of patent applications or intentions to file patent applications by anyone other than possibly presenters, although the voluntary, early disclosure of intellectual property was encouraged. The only contrary evidence, a vague reference in a draft manual and the after-the-fact testimony of interested witnesses, is not persuasive and is contradicted by the bulk of the contemporaneous evidence.

iii. The EIA/JEDEC Patent Policy Applied to Essential Patents

Complaint Counsel further contend that patents or applications that *might be involved* in the standards under development were required to be disclosed. (CCPHB at 45). In support of this proposition, they cite to nothing more than after-the-fact testimony by interested witnesses. That testimony is contradicted by the contemporaneous record.

JEDEC members were encouraged to disclose patents that were "essential" to a standard, i.e., those patents that were necessary for the manufacture or use of a product that complied with the standard. For example, the EIA's January 1996 letter to the Commission states that EIA "follows the ANSI intellectual property rights (IPR) policy as it relates to *essential* patents." F. 674 (emphasis added). JEDEC Secretary McGhee's July 10, 1996 memorandum to JEDEC Council members states that EIA encourages the voluntary disclosure of "known *essential* patents." F. 678 (emphasis added). EIA Manual EP-3-F refers only to standards that "*call for the use* of patented items." F. 635 (emphasis added). EIA Manual EP-7-A refers only to standards "that *call for the exclusive use* of a patented item or process." F. 636 (emphasis added).

The weight of the testimony supports the same conclusion. Hewlett-Packard representative Thomas Landgraf testified that he understood the patent policy to involve disclosure if "the standard required someone else's idea to be used . . . in order for it to operate." F. 776. JEDEC 42.3 chairman and IBM representative Gordon Kelley similarly testified that the disclosure duty was triggered by a patent claim that "reads on or applies" to the standard, meaning that "if you exercise the design or production of the component that was being standardized [it] would require use of the patent." F. 777. Another IBM JEDEC representative, Mark Kellogg, testified that his understanding was that "you have to disclose intellectual property that reads on the standard." F. 778.

Complaint Counsel failed to prove that the EIA/JEDEC patent policy applied to anything other than "essential" patents. Because disclosure is not required it may be splitting hairs to determine the precise nature of the patents that were encouraged to be disclosed. However, a broad duty, applicable to any potentially related patent would be too vague and difficult to apply with any consistency. As the Federal Circuit explained, any rule that

required disclosure of patent claims that were not necessary or essential in order to practice the standard would be overbroad:

> [t]o hold otherwise would . . . render the JEDEC disclosure duty unbounded. Under such an amorphous duty, any patent or application having a vague relationship to the standard would have to be disclosed. JEDEC members would be required to disclose improvement patents, implementation patents, and patents directed to the testing of standard-compliant devices – even though the standard itself could be practiced without licenses under such patents.

Infineon, 318 F.3d at 1101. Rather, the Federal Circuit held that the duty to disclose "extended only to claims . . . that reasonably might be necessary to practice the standard." *Infineon*, 318 F.3d at 1100.

iv. The EIA/JEDEC Patent Policy Was Triggered At the Time of Submitting Committee Ballots

Complaint Counsel contend that JEDEC members were required to disclose their intellectual property "as early as possible in the process." (CCPHB at 46). Again, they rely on after-the-fact testimony for support, but even that evidence, when considered in its entirety, supports the proposition that disclosure was not expected until formal balloting. F. 783-85. *See also* F. 761-65 (revealing conflict in testimony regarding the timing of disclosure). The committee ballot was considered the deadline for when disclosure should be made. F. 784. The informal patent tracking list reinforced this view, because it asked the committee chair to "resolve patent status prior to (choose one)," and then presented a list to choose from, from presentation to balloting. F. 785.

d. The Unsuccessful Attempt to Expand the EIA/JEDEC Patent Policy Created Ambiguity and Confusion

According to the January 1993 JEDEC Council meeting minutes, "Consensus was expressed that more strength is needed in our policy, however under existing laws, it seemed difficult to do." F. 733-35. The record shows that some JEDEC Council members wanted to expand EIA/JEDEC's patent policy to be mandatory, instead of voluntary, and to include patent applications and intentions to file a patent application. F. 724-39. Under governing EIA rules, however, JEDEC was prevented from making any changes to the patent policy. F. 735. At that time, JEDEC was a subpart or activity within EIA, not a separate entity, and was obligated to follow EIA's patent policy. F. 222, 740. Moreover, it is not clear that, even among those who wanted a more expansive policy, there was agreement on what the policy should be, as evidenced by the inconsistent trial testimony. *See* F. 748-65. There were a number of suggestions made regarding ways to change the policy, none of which were adopted. F. 726.

Instead of explicitly and formally changing the JEDEC policy from the EIA policy, the Council unsuccessfully attempted to redefine the word "patent." F. 744-47. Committee Chair G. Kelley stated that the Council "discussed the conflict between the EIA wording" and the proposed change to JEP 21-I and "we believed as a group that the concept of patents includes patent applications." F. 737. G. Kelley also testified that in 1991, the committee agreed to "work to that new definition of patents." F. 731. This attempted redefinition of the policy marked a departure both from established JEDEC policy and from EIA patent policy and caused confusion by creating ambiguity in the policy. F. 738.

During this time, ambiguous language was added to the sign-in/attendance roster and members' manual, as well as to JEP 21-I. This language was added as part of the unsuccessful attempt to expand the EIA/JEDEC patent policy. *See* F. 724-39. For example, the reference to "patentable or patented items," on the

front page of the meeting attendance roster confused rather than expanded the policy because the front page specifically refers to the EIA guides which appear on the reverse side and apply only to *issued* patents. F. 650-51. Similarly, the members' manual misstates the EIA policies to which it expressly refers and exemplifies the confusion surrounding members' interpretation of the policy. F. 662, 664.

The evidence indicates that members had different understandings of EIA/JEDEC's patent policy. JEDEC members described the policy as "not real clear . . . it was pretty vague," and "unclear." F. 721, 722, 723. One member described "a written policy," "an in-process modified policy," and "an expected policy." F. 720, 723. Texas Instruments presented a letter to JEDEC on March 9, 1994, regarding ambiguities in the EIA/JEDEC patent policy. The letter noted "Texas Instruments believes that the JC 42.3 Committee . . . should review and clarify its interpretation of the JEDEC Patent Policy." ". . . TI is concerned that the committee, or at least some of its members, have interpreted the scope of the JEDEC Patent Policy in a manner that is not only incorrect, but unworkable as well. *The resulting confusion has made it impossible for TI and other members to determine the appropriate course of conduct.*" F. 701 (emphasis added). The issue erupted after TI became embroiled in a disclosure dispute with JEDEC. Cray's representative testified that "some members agreed that [TI] didn't need to [disclose] and other[s] felt that they were in violation of the JEDEC policy by not [disclosing]." F. 706. It is thus evident, that by 1994, there was no clear understanding among members as to the requirements of the EIA/JEDEC patent policy. F. 707.

The Federal Circuit criticized this lack of clarity stating:

> In this case there is a staggering lack of defining details in the EIA/JEDEC patent policy. . . . JEDEC could have drafted a patent policy with a broader disclosure duty. It could have drafted a policy broad enough to capture a member's failed

> attempts to mine a disclosed specification for broader undisclosed claims. It could have. It simply did not.

Infineon, 318 F.3d at 1102.

e. Rambus Had No Patents or Pending Patents That Would Have Been Required to be Disclosed by the EIA/JEDEC Patent Policy

As found in Findings of Fact F. 766-71, disclosure of patents and pending patents was not required under the EIA/JEDEC patent policy. In addition, for the policy to apply, the JEDEC representative must have had actual knowledge of the pending patent or patent application. F. 780. Complaint Counsel failed to prove that Richard Crisp, Rambus's representative to JEDEC, had such actual knowledge. F. 781. Moreover, the patent policy was only triggered when submitting a committee ballot. F. 784-85. As discussed below, many of the presentations relied upon by Complaint Counsel never were balloted at JEDEC and thus the patent policy was never triggered.

i. SDRAM

The SDRAM standard was adopted in March 1993. F. 351. The only EIA or JEDEC policy Complaint Counsel cite in support of their interpretation of the patent policy is JEP 21-I which, as noted earlier, was not published until October of 1993 (F. 610), seven months *after* approval of the SDRAM standard.

The parties stipulated that, as of January 1996, Rambus had no U.S. patents that were essential to the manufacture or use of any JEDEC-compliant device and that prior to the adoption of the JEDEC SDRAM standard in 1993, Rambus had no claims in any pending patent applications that, if issued, would necessarily have been infringed by the manufacture or use of any SDRAM device manufactured in accordance with the 1993 JEDEC SDRAM

standard. F. 939, 959. Complaint Counsel, in seeming contradiction to these stipulations, nonetheless argue that Rambus should have disclosed U.S. Patent No. 5,513,327 (the '327 patent) as well as a number of patent applications. CCPHB at 64-67.

Complaint Counsel allege that Rambus's duty to disclose the '327 patent was triggered by three presentations at JEDEC: (1) a presentation by William Hardell of IBM contained in the May 1992 minutes of the JEDEC 42.3 subcommittee (the "Hardell presentation"), (2) a "Future SDRAM Features Survey Ballot contained in the December 1995 minutes of the JEDEC 42.3 subcommittee (the "Survey Ballot"), and (3) a presentation by Samsung entitled "Future SDRAM," contained in the March 1996 minutes of the JEDEC 42.3 subcommittee (the "Samsung presentation"). CCPHB at 70; F. 940-41. All three presentations were made before the '327 patent issued, so that Rambus could not have disclosed the '327 patent at the time of these presentations. F. 942.

None of these three presentations ever rose to the level of a balloted proposal. F. 951, 954, 956. As such, they did not specify how the features would actually be implemented. The Hardell presentation states simply "dual clock edge," the Survey Ballot only that there was "mixed support" for "using both edges of the clock for sampling inputs," and the Samsung presentation only that "[d]ata in sampled at both edge [sic] of Clock into memory." F. 950, 953, 955. As Complaint Counsel's technical expert, Professor Jacob, concedes, the '327 patent does not cover the broad concept of dual edge clocking, but only certain "specific implementations" of dual edge clocking. F. 945. Because these presentations did not provide sufficient implementation details, it would not be possible to determine whether or not the '327 patent covered the presentations. F. 957. Rambus has not asserted the '327 patent against any manufacturer of SDRAM or DDR SDRAM devices. F. 958.

Rambus did not have any undisclosed *patent applications* during the time it was a JEDEC member that it should have disclosed. Complaint Counsel allege that Rambus had four patent applications pending during the time that it was a JEDEC member that should have been disclosed to JEDEC, including application nos. 07/847,961 (the '961 application) and 08/469,490 (the '490 application). F. 960.

In both of these cases, the claims raised by Complaint Counsel were pending only briefly in 1995, over a year after the SDRAM standard was published, before being cancelled. F. 961-62. In an April 16, 1995 office action, the U.S. Patent and Trademark Office ("PTO") rejected all of the claims raised by Complaint Counsel regarding the '961 application and, in particular, found that claims 151-165 were indefinite. F. 961. The claims at issue in the '490 application were either not pursued or withdrawn from consideration by Rambus. F. 962. EIA/JEDEC rules certainly cannot be understood to require disclosure of claims withdrawn or rejected by the PTO.

Moreover, the Federal Circuit noted that the claims of the '961 application would not read on a device built to the JEDEC SDRAM standard. The Federal Circuit stated: "[t]his court has examined the claims of the cited applications as well as the relevant portions of the SDRAM standard. Based on this review, this court has determined that substantial evidence does not support the finding that these applications had claims that read on the SDRAM standard." *Infineon*, 318 F.3d at 1103. The Federal Circuit further held that "claims in the '961 application were limited to the device identifier feature" which is not "necessary to practice the SDRAM standard." *Id. See Key Pharms. v. Hercon Labs. Corp.*, 161 F.3d 709, 716 (Fed. Cir. 1998) (Federal Circuit decisions on claim construction have "national *stare decisis* effect") (citing *Markman v. Westview Instruments, Inc.*, 517 U.S. 370, 391 (1996)).

There are only two other applications that Complaint Counsel allege should have been disclosed by Rambus: application nos. 07/847,692 (the '692 application) and 08/222,646 (the '646 application). F. 960. These applications are not alleged to cover any JEDEC standard, but instead are alleged to cover certain JEDEC presentations concerning on-chip phase locked loop ("PLL") and dual-edge clocking. As with the '327 patent, the events that Complaint Counsel contend "triggered" a duty to disclose certain claims in patent applications were merely discussions or presentations, not ballot proposals, and thus the patent disclosure policy was not triggered. F. 964-67.

Complaint Counsel likewise have not presented evidence sufficient to find that presentations of voltage swing signaling, dual bank design, auto-precharge, or synchronous clocking were ever included in a standard, formally balloted for inclusion in a standard, or that Crisp had actual knowledge of any patents or patent applications with any claims that might cover the technologies presented. F. 334-50, 781.

Finally, Complaint Counsel cannot salvage their case by relying on proof that Rambus might have believed (albeit wrongly) that claims in its applications, if issued, would have covered technologies being standardized by JEDEC. As the Federal Circuit observed:

> The JEDEC policy, though vague, does not create a duty premised on subjective beliefs. JEDEC's disclosure duty erects an objective standard. It does not depend on a member's subjective belief that its patents do or do not read on the proposed standard. Otherwise the standard would exempt a member from disclosure, if it truly, but unreasonably, believes its claims do not cover the standard. . . . [T]he JEDEC test in fact depends on whether claims reasonably might read on the standard. A member's subjective beliefs, hopes, and desires are

> irrelevant. Hence, Rambus's mistaken belief that it had pending claims covering the standard does not substitute for the proof required by the objective patent policy.

Infineon, 318 F.3d at 1104.

Because JEP 21-I was published after the SDRAM standard was approved; because disclosure of intellectual property was voluntary; because there is no evidence that Rambus's representative to JEDEC had actual knowledge of any patents or pending patents that would trigger the EIA/JEDEC patent policy; and because the presentations were not subject to a triggering event, Rambus was under no disclosure duty relating to the SDRAM standard.

ii. DDR-SDRAM

Formal consideration of the DDR-SDRAM standard did not begin until after Respondent withdrew from JEDEC. F. 968-82. Respondent attended its last JEDEC meeting on December 6, 1995 and formally withdrew from JEDEC by a letter dated June 17, 1996. F. 968. Although Respondent continued receiving information about JEDEC activities after it stopped attending meetings (F. 279-82), once its membership ended, Respondent was not obligated to disclose patent information. F. 782, 982.

Formal work on the DDR-SDRAM standard did not begin within JEDEC, at the earliest, until December 1996, when Fujitsu made the first showing of a DDR-SDRAM related proposal in JEDEC. F. 973-76. This is confirmed by an IBM presentation which lists as the first official DDR presentation at JEDEC a December 1996 presentation and by a Mitsubishi memorandum regarding the history of DDR-SDRAM that similarly relates that a proposal to JEDEC was made in December of 1996. F. 980, 981. It is not until March 1998 that the DDR-SDRAM standard was approved. F. 973-74. JEDEC Chairman Rhoden, in a "recap [of]

what had transpired with DDR," cites a "lot of private and independent work outside of JEDEC for most of 1996 (here is where we missed a good opportunity to start early)" and then lists December 1996 as the first JEDEC presentation. F. 973-74. The standard received approval from JEDEC's Board in August of 1999 and was published in June of 2000. F. 427-28.

Both the Federal Circuit and the District Court in the *Infineon* litigation found that Respondent had no duty to disclose regarding DDR-SDRAM because Rambus had withdrawn from JEDEC prior to formal consideration of the standard. 164 F. Supp.2d at 777; 318 F.3d at 1105. The District Court stated: "Infineon failed to prove that Rambus had a duty to disclose pending patents relating to DDR SDRAM because Rambus was not a member of JEDEC at the relevant time in which the DDR SDRAM standard was under consideration." 164 F. Supp.2d at 777.

The Federal Circuit agreed, finding that:

> the disclosure duty, as defined by the EIA/JEDEC policy, did not arise before legitimate proposals were directed to and formal consideration began on the DDR-SDRAM standard. None of the evidence relied on by Infineon (e.g., survey ballot, technology proposals on the SDRAM standard) provides substantial evidence for the implicit jury finding that Rambus had patents or applications 'related to' the DDR-SDRAM standard that should have been disclosed before the standard came under formal consideration.

Infineon, 318 F.3d at 1105.

In addition, the parties stipulated that as of January 1996, Rambus held no issued U.S. patents that were essential to the manufacture or use of any device manufactured in compliance

with any JEDEC standard. F. 939. Once Rambus withdrew from JEDEC, it was no longer subject to the EIA/JEDEC patent policy.

Complaint Counsel have offered insufficient evidence in support of their argument that Respondent violated the EIA/JEDEC disclosure duty with respect to the DDR SDRAM standard. The evidence presented at this trial clearly establishes that Respondent withdrew from JEDEC before any formal work on the DDR standard commenced. Thus, the conclusions shared by both the District Court and the Federal Circuit in *Infineon* on this question remain sound. As such, there is no basis to find a disclosure duty or violation of a duty by Respondent as it would pertain to the DDR SDRAM standard.

4. The Evidence Presented at Trial Does Not Provide a Factual Basis for Finding That Rambus Made Affirmative, Misleading Statements to JEDEC

Complaint Counsel argue that Rambus made "affirmative misleading statements calculated to quell any concerns or suspicions of JEDEC members as to the possibility that Rambus had patents or patent applications relevant to JEDEC's work." CCPHB at 72. In support of this argument, Complaint Counsel challenge Respondent's conduct in refusing to answer questions about its intellectual property on two occasions and Respondent's allegedly deceptive letter formalizing its withdrawal from JEDEC.

At Richard Crisp's first formal JC 42.3 subcommittee meeting as Rambus's JEDEC representative in May of 1992, Gordon Kelly, JC 42.3 committee chair, asked Crisp whether Rambus had patents or potential patents covering two bank design. F. 808, 811. Crisp shook his head indicating that he declined to comment. F. 808, 811. The evidence shows that JEDEC members understood that Crisp was declining to comment and not that he was making any indication about whether Rambus had obtained or intended to pursue patent protection of the two bank design. F. 812-17, 819, 857. For example, Kellogg testified that he considered Crisp's

conduct a "flag" because JEDEC members were "describing possible intellectual property concerns which may affect our decision process for synchronous DRAM," that "[t]hat is a concern," and that "[t]he lack of response by Rambus is also a concern." F. 825. Complaint Counsel did not present any evidence that Crisp was informed that his act of not commenting violated the JEDEC rules, as would have been expected at his first meeting if patent disclosure was required.

Despite Crisp's refusal to comment on Rambus's intellectual property, the evidence is compelling that JEDEC committee leaders and members were fully aware of Rambus's patents and applications with respect to features being considered for incorporation into JEDEC standards. As early as March 1992, Gordon Kelley had prepared a memorandum regarding Rambus's patents. F. 788. In April 1992, he prepared a "Rambus Assessment" along with two other IBM employees, the day after he attended a presentation by Rambus. F. 789, 791. The assessment noted "the risk is whether it [RDRAM] becomes a standard for the low-end bulk of DRAM bit volume." F. 793. The assessment further noted that "if Rambus fails to become a standard then it is business as usual for [IBM] and the SDRAM has a significant chance of being standard." F. 794. It is thus clear that Kelley was aware of Rambus technology and the prospects of its success in the spring of 1992. F. 786-806.

Similarly, Willi Meyer of Siemens (now Infineon) testified that in 1992 "we were absolutely sure that Rambus was trying to get patents." F. 806. Meyer also prepared a chart showing the "Pros" and "Cons" of "Rambus RDRAM," stating that 2-bank synchronous DRAM "may fall under Rambus patents." F. 803-06. Howard Sussman, the NEC representative, had reviewed Rambus's international patent application pursuant to the Patent Cooperation Treaty ("PCT application") and felt that many of the claims were barred by prior art. F. 810. Mark Kellog of IBM similarly noted, "Rambus International Patent . . . suspect claims won't hold." F. 870, 1524. Thus, Richard Crisp's refusal to

comment on Rambus patents at both the May 1992 and September 1995 JC 42.3 meetings not only raised concerns regarding the possible existence of Rambus intellectual property, but put members on notice, both expressly and implicitly, of Rambus's intent to seek broad coverage of its patents. F. 807-25, 842-57.

By an email dated June 13, 1995 to Hans Wiggers, the Hewlett-Packard representative, Crisp clearly warned that "the Ramlink/Synclink proposals will have a number of problems with Rambus intellectual property . . . *but I must caution you that there is a lot of material that is currently pending and we will not make any comment at all about it until it issues.*" F. 754 (emphasis supplied). In August 1995, Rambus again informed the SyncLink working group that its work might infringe Rambus's intellectual property. F. 853.

At the September 1995 JEDEC meeting, Crisp presented a written response to the questions about intellectual property that had been raised at the May 1995 meeting. F. 855. Rambus's statement, *published in full in the JEDEC minutes*, indicates in part:

> Rambus elects to not make a specific comment on our intellectual property position relative to the Synclink proposal. Our presence or silence at committee meetings does not constitute an endorsement of any proposal under the committee's consideration nor does it make any statement regarding potential infringement of Rambus intellectual property.

F. 855.

JEDEC members should have clearly understood from this statement that Rambus might have or might attempt to obtain patents covering technology utilized in JEDEC standards. Intel Corporation ("Intel") representative Sam Calvin testified that he understood that any silence by Rambus should not be taken as an

indication that Rambus did not have intellectual property relating to JEDEC's work. F. 857. Gordon Kelley testified regarding Crisp's refusal to comment in 1992 that Rambus's lack of comment was "unusual on the committee and is surprising" and that a "comment of no comment is notification to the committee that there should be a concern" about intellectual property issues. F. 819. The same logic would apply to Crisp's representation in 1995. Thus, again, the evidence does not support the contention that JEDEC was misled.

Rambus representatives attended their last JEDEC Meeting in December of 1995. F. 871. Rambus's separation from JEDEC was formalized on June 17, 1996, when Rambus sent a letter to JEDEC that stated that "Rambus plans to continue to license its proprietary technology on terms that are consistent with the business plan of Rambus . . . . We trust that you will understand that Rambus *reserves all rights regarding its intellectual property*." F. 871, 874, 968 (emphasis added). Rambus included with the letter a list of issued patents. F. 874. The list did not include the '327 patent. F. 875. The evidence is inconclusive regarding whether the '327 patent was left off of the list intentionally or inadvertently. F. 876.

In any event, JEDEC members were clearly aware of the technology invented by Rambus founders Farmwald and Horowitz as well as Rambus's business model which sought to protect and profit from theses inventions. *Infra* Section III.E.3. The evidence presented by Complaint Counsel is thus insufficient to provide a factual basis to find that Rambus affirmatively misled JEDEC.

5. Amendments to Claims to Broaden Patent Applications Were Not Improper

Complaint Counsel charge that Respondent's conduct constituted anticompetitive behavior and exclusionary conduct in that Respondent set out to amend and broaden its pending patent

applications for the specific purpose of covering technological features that were adopted or being considered for adoption in JEDEC's SDRAM standards, while deliberately keeping these patent applications secret from JEDEC. CCPTB at 6, 88. This argument fails for two reasons. First, as a matter of patent law, it was entirely legitimate for Respondent to seek claims covering technologies promoted by other JEDEC members that were originally disclosed in the '898 application. Second, as a matter of fact (discussed in F. 587-785 and the previous section of this analysis) there was no disclosure obligation under the JEDEC patent policy which attached to Rambus. As such, there can be no finding that Respondent, in violation of JEDEC rules, deliberately concealed proprietary technology from JEDEC that it was otherwise entitled to have.

The patent laws dictate that Rambus's patents could be based only on the "ideas" or inventions described in the original Farmwald-Horowitz patent application (the '898 application). Thus, under law, Rambus could not have "taken" ideas from JEDEC to be incorporated into its patent applications. The PTO's determination that Rambus's numerous divisional and continuation applications properly claim priority to the original '898 application (F. 168-78; *see Infineon*, 318 F.3d at 1084) cannot be second guessed. The patent laws make clear that Rambus was within its rights to protect the inventions disclosed in the '898 application that it saw being considered for use by JEDEC members.

The patent document which grants the patentee a right to exclude others . . . consists of two primary parts:

> (1) a written description of the invention, which may . . . include drawings, called the "specification," enabling those skilled in the art to practice the invention, and (2) claims which define or delimit the scope of the legal protection which

> the government grant gives the patent owner, the patent "monopoly."

General Foods Corp. v. Studiengesellschaft Kohle mbH, 972 F.2d 1272, 1274 (Fed. Cir. 1992). To obtain a patent claim the inventor must adequately set forth in the written description: (1) the invention, (2) the manner and process of making and using the invention, and (3) the best mode contemplated by the inventor of carrying out the invention. 35 U.S.C. § 112; *see also* 3-7 CHISUM ON PATENTS § 7.01 (2003).

The patent system recognizes that an inventor might not fully claim all the inventions nor the full scope of the individual inventions in an initial application. To allow the inventor to claim the full scope of the inventions disclosed in the application, patent law allows the inventor to amend its claims, to file continuation applications, or to file divisional applications. *See* 37 C.F.R. § 1.141(a); 35 U.S.C. § 121; *see also* 4-12 CHISUM ON PATENTS § 12.04, 13.03[2](2003). Here, the PTO determined that the '898 application covered multiple inventions. F. 169-71. The PTO issued an eleven way restriction requirement requiring Rambus to elect one invention to pursue in the '898 application. F. 171. Thereafter, Rambus filed numerous divisional and continuation applications based on the original '898 application. F. 172. As of April 2003, Rambus had filed a total of sixty-three continuation and divisional applications and has been issued at least forty-three patents. F. 174.

To maintain the same priority date as the original application, any amendment, continuation application, or divisional application must be supported by the disclosure in the original application. 35 U.S.C. §§ 112, 120, 121, 132. To be adequate, a written description must "convey with reasonable clarity to those skilled in the art that, as of the filing date sought, [the inventor] was in possession of the invention." *Vas-Cath, Inc. v. Mahurkar*, 935 F.2d 1555, 1563-64 (Fed. Cir. 1991). *See also Markman v.*

Westview Instruments, Inc., 52 F.3d 967, 986 (Fed. Cir. 1995) (*en banc*), *aff'd*, 517 U.S. 370 (1996).

To maintain the same priority date as the original application, neither an amendment to a continuation application nor a divisional application may add any "new matter." 35 U.S.C. § 132 ("No amendment shall introduce new matter into the disclosure of the invention."); 35 U.S.C. § 120 (giving benefit of original application filing date under certain circumstances); *Applied Materials, Inc. v. Advanced Semiconductor Materials Am., Inc.*, 98 F.3d 1563, 1579 (Fed. Cir. 1996) (Mayer, J., concurring) ("By definition, a continuation adds no new matter and is akin to an amendment of a pending application."); 35 U.S.C. § 121 (according original priority date to divisional application only if the divisional conforms to section 120). These requirements – that any amendment, continuation application, or divisional be supported by the original disclosure without any "new matter" – ensure that the inventor is limited to claiming only those inventions disclosed in the original application. *TurboCare Div. of Demag Delaval Turbomachinery Corp. v. General Elec. Co.*, 264 F.3d 1111, 1118 (Fed. Cir. 2001).

Thus, while the '898 application continues to be the progenitor of numerous patents, the PTO has determined that each and every claim contained in these new patents is supported by the original written description filed by Farmwald and Horowitz in 1990. F. 178. Consequently, each invention and the full scope of each invention claimed by Rambus was described in the written description of the '898 application (and therefore in the PCT application that became public in 1991).

Once an inventor has staked out his inventions in the written description of his application, the fact that someone uses one of the inventions in a competing product after the application has been filed but before the inventor claims that specific invention does not override the inventor's entitlement to claim the invention. As noted by the Federal Circuit:

> It should be made clear at the outset of the present discussion that there is nothing improper, illegal or inequitable in filing a patent application for the purpose of obtaining a right to exclude a known competitor's product from the market; nor is it in any manner improper to amend or insert claims intended to cover a competitor's product the applicant's attorney has learned about during the prosecution of a patent application.

Kingsdown Medical Consultants, Ltd. v. Hollister, Inc., 863 F.2d 867, 874 (Fed. Cir. 1988).

Further, the Federal Circuit has rejected the notion that amending a pending patent application to cover a competing product constitutes acting in "bad faith." *Multiform Desiccants, Inc. v. Medzam Ltd.*, 133 F.3d 1473, 1482 (Fed. Cir. 1998). In fact, amending a pending patent application to cover "a product containing a variant of the inventor's brainstorm" is "standard practice and has been for a long time." MERGES, MENELL & LEMLEY, INTELLECTUAL PROPERTY IN THE NEW TECHNOLOGICAL AGE 225 (2d ed. 2000).

These principles apply in the DRAM industry as they do in any other. In *Texas Instruments, Inc. v. U.S. Int'l Trade Comm'n*, 871 F.2d 1054 (Fed. Cir. 1989), the patentee, Texas Instruments, amended its pending patent claims to cover a DRAM device sold by a company called MOSTEK. *Id.* at 1064-65. Specifically, Texas Instruments broadened its pending claims by deleting certain claim limitations. *Id.* at 1065. The Federal Circuit held that the broadening of the claims to cover the competing DRAM was not improper. *Id.*

It was therefore legitimate for Rambus to seek claims covering technologies proposed at JEDEC that were originally disclosed in its '898 application. In amending its pending claims, Respondent

did not add new matter, and because it was under no disclosure duty, Respondent was not acting in bad faith or concealing secret patents from JEDEC. For the reasons stated herein, Complaint Counsel's claim that Respondent engaged in a pattern of anticompetitive acts and practices fails. In so holding, the Court next considers whether the challenged conduct was exclusionary in nature.

C. No Exclusionary Conduct

1. Exclusionary Conduct Defined

Exclusionary conduct is "'behavior that not only (1) tends to impair the opportunities of rivals, but also (2) either does not further competition on the merits or does so in an unnecessarily restrictive way.'" *Aspen Skiing*, 472 U.S. at 605 n.32 (quoting 3 P. Areeda & D. Turner, Antitrust Law 78 (1978)). "Generally, a finding of exclusionary conduct requires some sign that the monopolist engaged in behavior that – examined without reference to its effects on competitors – is economically irrational." *Stearns Airport Equipment Co., Inc. v. FMC Corp.*, 170 F.3d 518, 523 (5th Cir. 1999). *See also Aspen Skiing*, 472 U.S. at 608, 610-11 (conduct was exclusionary where defendant failed to offer "any efficiency justification whatever" for its pattern of conduct); *In re E.I. Du Pont de Nemours & Co.*, 96 F.T.C. 652, 738 (1980) (To determine whether conduct by monopolists is unreasonably exclusionary or if it constitutes legitimate competitive behavior, the courts have fashioned a variety of criteria such as whether the behavior amounted to ordinary marketing practices, whether it was profitable or economically rational, or whether it resulted in improved product performance.).

An example of conduct involving intellectual property that is not exclusionary, even though it adversely affects competitors, is where a firm develops a cost-saving technology, protects the technology through trade secrets or patents, and drives its rivals

out of business by being the low cost competitor. (Rapp, Tr. 9913). Not disclosing information about pending or future patent applications is rational and profit maximizing for a firm; it is also procompetitive for the same reasons that preserving trade secrets is procompetitive. (Rapp, Tr. 9918). This type of nondisclosure preserves incentives to innovate because innovation depends on the ability to control intellectual property. (Rapp, Tr. 9918-19). Exercising intellectual property rights to exclude competitors and protecting trade secrets from use by other companies are not, by law, exclusionary conduct. (Rapp, Tr. 9229-30). Similarly, exercising intellectual property rights to charge royalties that might raise a rival's costs is not exclusionary conduct. (Rapp, Tr. 9229).

2. Legitimate Business Justifications

"The key factor courts have analyzed in order to determine whether challenged conduct is or is not competition on the merits is the proffered business justification for the act." *Stearns Airport*, 170 F.3d at 522; *Concord Boat Corp. v. Brunswick Corp.*, 207 F.3d 1039, 1062 (8th Cir. 2000) (The proffered business justification is the most important factor in determining whether the challenged conduct is not competition on the merits.); *Taylor Pub'l Co. v. Jostens, Inc.*, 215 F.3d 465, 475 (5th Cir. 2000) ("To determine whether conduct is exclusionary, we look to the proffered business justification for the act."). "A defendant may avoid liability by showing a legitimate business justification for the conduct." *Multistate Legal Studies, Inc. v. Harcourt Brace Jovanovich*, 63 F.3d 1540, 1550 (10th Cir. 1995). *See also Du Pont*, 729 F.2d at 140 ("[I]n the absence of proof of a violation of the antitrust laws or evidence of collusive, coercive, predatory, or exclusionary conduct, business practices are not 'unfair' in violation of § 5 unless those practices either have an anticompetitive purpose or cannot be supported by an independent legitimate reason.").

Legitimate business justifications or "normal business purpose[s]" (*Aspen Skiing*, 472 U.S. at 608-10), include protecting trade secrets and proprietary information. *Technical Resource Servs. v. Dornier Med. Sys., Inc.*, 134 F.3d 1458, 1467 (11th Cir. 1998). *See also In re Indep. Serv. Orgs. Antitrust Litig.*, 203 F.3d 1322, 1329 (Fed. Cir. 2000) (excluding others from use of copyrighted work is a "presumptively valid business justification for any immediate harm to consumers"); *Berkey Photo, Inc. v. Eastman Kodak Co.*, 603 F.2d 263, 281-82 (2d Cir. 1979) ("a firm may normally keep its innovations secret from its rivals as long as it wishes"). Where there is a business justification, the challenged conduct is not exclusionary even if "one reason for [defendant's conduct] was to disadvantage the competition." *Universal Analytics, Inc. v. MacNeal-Schwendler Corp.*, 914 F.2d 1256, 1259 (9th Cir. 1990). It is the defendant's burden to demonstrate that its business justification is supported by facts. *See Microsoft*, 253 F.3d at 59, 66 (Microsoft's failure to offer procompetitive justification for certain conduct led to conclusion it was exclusionary).

Respondent has demonstrated that there were legitimate business justifications for the conduct challenged by Complaint Counsel. F. 1064-87. Rambus believed that if it revealed its patent applications, other companies could file interference actions and that, in other countries where the rules are first to file, someone could file a claim before Rambus did. F. 1064. A contemporaneous document shows that Rambus decided that it could not be expected to talk about potential infringement for patents that had not issued both from the perspective of not knowing what would wind up being acceptable to the examiner and from the perspective of not disclosing its trade secrets earlier than necessary. F. 1065.

The protection of trade secrets is a valid business justification for not disclosing information regarding pending patent applications and intentions to file applications or to amend pending claims in the future. F. 1076. Disclosure of trade secrets,

including pending patent applications or intentions to file or amend future applications, even after a parent patent application becomes public, may: (1) jeopardize the issuance of pending claims by enabling competitors to file patent interferences or to race to be first-to-file in certain foreign jurisdictions; and (2) result in a loss of competitive advantage by informing competitors of the firm's research and development focus or by inducing competitors to begin work around efforts earlier. F. 1078-87. Even after the '898 application had been disclosed (in the form of the PCT application), Rambus still had trade secrets (additional pending applications and intentions to file additional applications) that it could legitimately protect from disclosure. F. 1080. Rambus's keeping information about its pending or future patent applications confidential did not impose on Rambus costs or risks that were compensable only by excluding rivals and thereby gaining market power. F. 1086. These facts demonstrate that Respondent's conduct, in maintaining the confidentiality of the proprietary information contained in its patent applications, clearly related to a legitimate and normal business purpose. The presence of these legitimate business justifications, that were not done in an unnecessarily restrictive way, precludes a finding of exclusionary conduct.

3. Conduct Before Standard Setting Organizations

Complaint Counsel further argue that Respondent's bad-faith, deceptive acts to a standard setting organization constitute exclusionary conduct. CCPHB at 19. This argument is not convincing for three reasons. First, as set forth above, Complaint Counsel did not prove that JEDEC had a clear and unambiguous requirement that its members disclose patents or patent applications. *Supra* Section III.B.3. Second, the legitimate business justifications of a company not disclosing information regarding its pending patent applications or its intentions to file future patent applications, regardless of what standards are developed, are not altered by mere participation in a standard setting organization. F. 1087. Third, Complaint Counsel's legal

support for their proposition is clearly distinguishable from the facts of this case.

First, a cornerstone of any standard setting organization is a clearly stated and clearly *understood* intellectual property policy. *See Amicus* Brief of Consumers Electronics Association, *et al.*, On Petition For a Writ of Certiorari to the United States Supreme Court, *Infineon Technologies, et al., v. Rambus, Inc.*, No. 03-37, Attachment 4 to CCPHB at 3 (emphasis added). EIA/JEDEC's patent policy did not meet this standard and the Court will not rewrite the patent policy to impute "requirements" that were not within its actual scope. *See Infineon*, 318 F.3d at 1098. As patent disclosure policies usually vary by organization, each reflects the collective judgment of the organization's participants as to what disclosure requirements best serve the purposes of the group. *See Amicus* Brief of Commonwealth of Virginia, *et al.*, On Petition For Writ of Certiorari To United States Supreme Court, *Infineon Technologies AG, et al. v. Rambus, Inc.*, No. 03-37, Attachment 5 to CCPHB at 7. Any such requirements, however, must be clearly and unequivocally articulated. Here, they were not.

The EIA/JEDEC patent policy has been shown to be a loosely defined amalgam of confusing, contradictory documents and presentations. It failed to clearly define members' rights, or more importantly, their obligations. *See* F. 587-785. It bound participants with actual knowledge of intellectual property, but did not require the participants to check for intellectual property within their companies. F. 778-80. Although it sought assurance that members would license patents at RAND rates, it did not always take steps to insure that such assurances could or would be made. It did not maintain a complete patent tracking list and responded inconsistently when members failed to disclose intellectual property. F. 666-69. *Compare* F. 691-700 *with* F. 686-690.

As to the second point, an open standards committee, to function effectively, needs to be able to assure member companies

that legitimate business justifications for protecting innovative, proprietary information will not be undermined by inconsistent, inartfully drafted and practiced disclosure policies. To hold otherwise would have a chilling effect on procompetitive participation in such bodies and in the marketplace generally. As such, Rambus's mere membership in such an organization, without more, cannot form the basis for excluding its legitimate right to protect its trade secrets from disclosure.

Finally, as to the third point, Complaint Counsel again rely on the consent decree entered in *Dell*, 121 F.T.C. 616 and on *Indian Head*, 817 F.2d 938. As noted above, the *Dell* consent decree provides no precedential value. The facts in *Indian Head* are dramatically different from the circumstances presented here. In *Indian Head*, defendant conspired with other steel companies to exclude the plaintiff's competing plastic products from standards set by the organization. 817 F.2d at 497. The conduct was plainly the kind of egregious unlawful activity that has traditionally concerned antitrust courts about standard setting bodies – agreements among some or all members acting in cartel-like fashion to exclude rival technologies.

On appeal from the Second Circuit, the Supreme Court in *Allied Tube* found that defendant "did not violate any rules of the Association" but "nonetheless did 'subvert' the consensus standard-making process of the Association," and concluded that "[t]he antitrust validity of these efforts is not established, without more, by petitioner's literal compliance with the rules." *Allied Tube*, 486 U.S. at 498.

Allied Tube does not compel a finding that Rambus's conduct before JEDEC constitutes exclusionary conduct. Here, Rambus did not at any time encourage JEDEC to promote or adopt any feature or technology for inclusion in the SDRAM standard. When asked on two occasions at JEDEC meetings if it would care to comment about its intellectual property rights, it merely declined to do so. F. 809, 855. It did not lie about its patent rights

or its intention to assert them. It was not even allowed to present its technology for standardization. F. 824-25. By contrast, in *Indian Head*, defendant packed the annual meeting with newly registered members, by arranging and paying for people to join the industry and register as voting members, and instructed its personnel how to vote. 817 F.2d at 947. The steel interest's recruitment of 230 members for purposes of casting a single vote gave it a disproportionate voice, inconsistent with the concept of "consensus" standard making. *Id.* Respondent's conduct, under the facts established in this case, does not rise to the level found to constitute exclusionary conduct in *Allied Tube*.

4. Violations of Extrinsic Duties or Deception Affecting Consumers Not Exclusionary Conduct

Complaint Counsel also argue that exclusionary conduct includes conduct that is improper for reasons extrinsic to the antitrust laws. CCPHB at 89. Complaint Counsel argue that Respondent's conduct was exclusionary because it amounted to "deception" or violated "extrinsic duties," such as the duty of good faith and duty to disclose relevant patent information established by JEDEC's rules. CCPHRB at 67. This argument also fails. First, as set forth in Section III.B.3., *supra*, Complaint Counsel have not proven that Respondent's conduct constituted deception or violated any clear duty of good faith or duty to disclose, whether established by open standards, JEDEC's rules, or otherwise. Second, case law establishes that exclusionary conduct is not determined by liability "in tort or contract law, under theories of equitable or promissory estoppel or implied contract . . . or by analogy to the common law tort" rules. *Olympia Equipment Leasing Co. v. Western Union Tel. Co.*, 797 F.2d 370, 376 (7th Cir. 1986). Rather, as the Commission has acknowledged in an amicus brief, exclusionary conduct is an antitrust concept. Brief for the United States and the Federal Trade Commission as *Amicus Curiae* on Petition for a Writ of Certiorari, *Verizon Communications, Inc. v. Trinko*, No. 02-682, at 13 (December 2002) http://www.usdoj.gov/osg/briefs/2002/2pet/5ami/2002-

0682.pet.ami.pdf ("Conduct is 'exclusionary' or 'predatory' in antitrust jurisprudence if the conduct would not make economic sense for the defendant but for its elimination or softening of competition.") (citation omitted). Thus, exclusionary conduct should be analyzed using antitrust principles.

Complaint Counsel argue that "'where conduct contributes to establishing or maintaining monopoly power, a court will be especially likely to find that conduct predatory or anticompetitive if it is *also improper* for reasons extrinsic to the antitrust laws [listing "false advertising" and "product disparagement" as two examples].'" CCPHB at 89 (quoting ABA SECTION OF ANTITRUST LAW, ANTITRUST LAW DEVELOPMENTS at 247-49 (5th ed. 2002)) (emphasis added). Complaint Counsel's only support for this proposition, the ABA handbook, is not persuasive legal authority and does not support Complaint Counsel's position. By its terms, it refers only to conduct that is improper in an antitrust sense and is "*also* improper" for extrinsic reasons. Thus, Complaint Counsel have provided no basis to avoid traditional legal requirements for proving exclusionary conduct.

Moreover, courts have repeatedly held that a violation of an extrinsic rule, statute, or ethic is not itself exclusionary conduct. *E.g.*, *Olympia Equipment*, 797 F.2d at 376; *Goldwasser v. Ameritech Corp.*, 222 F.3d 390, 399-401 (7th Cir. 2000) (plaintiff must state "freestanding antitrust claim" and cannot base its antitrust claim simply on violations of the 1996 Telecommunications Act. "It would be undesirable here to assume that a violation of the 1996 Act requirement automatically counts as exclusionary behavior for purposes of Sherman Act § 2."); *Bucher v. Shumway*, 452 F. Supp. 1288, 1291 (S.D.N.Y. 1978) (no antitrust liability for violation of laws preventing "deception or overreaching" in the securities markets).

Further, a breach of a duty of good faith and fair dealing in itself does not constitute exclusionary conduct. In *Conoco, Inc. v. Inman Oil Co.*, 774 F.2d 895 (8th Cir. 1985), a distributor of

petroleum products brought suit against its franchisor alleging that the franchisor's low bidding for contracts that the distributor was also seeking constituted an attempt to monopolize and a breach of the implied obligation of good faith and fair dealing between the parties. While holding that bidding against its franchisee did breach the franchisor's implied obligation of good faith and fair dealing, the Eighth Circuit held that the conduct was not exclusionary because the franchisor had a legitimate business reason unrelated to the elimination of competitors – obtaining a new customer. *Id.* at 905-06, 908-09.

Complaint Counsel also argue that deceptive and misleading conduct that deprives consumers of information constitutes exclusionary conduct. CCPHRB at 67-68 (citing *Microsoft*, 253 F.3d at 76-77; *44 Liquormart, Inc. v. Rhode Island*, 517 U.S. 484, 503 (1996); *Conwood Co. v. United States Tobacco Co.*, 290 F.3d 768 (6th Cir. 2002), *cert. denied*, 123 S. Ct. 876 (2003); *Du Pont*, 729 F.2d at 137; *National Ass'n of Pharm. Mfrs. v. Ayerst Labs.*, 850 F.2d 904, 916 (2d Cir. 1988); *Caribbean Broadcasting Sys. v. Cable & Wireless PLC*, 148 F.3d 1080, 1087 (D.C. Cir. 1998). However, Complaint Counsel's economic expert, Professor McAfee, admitted that a misrepresentation, even if it has an impact on competition, is not always exclusionary. *See* F. 1088-89. Further, none of the cases relied upon by Complaint Counsel compel a finding that Respondent's conduct here, alleged misrepresentations through omission, constitutes exclusionary conduct.

In the majority of the cases relied upon by Complaint Counsel, the conduct at issue went far beyond the conduct Respondent is alleged to have engaged in. In *Microsoft*, defendant was found to have engaged in exclusionary conduct based not solely on its misleading statements regarding the capabilities of its Java development application, but also based on designing a Java Virtual Machine that was incompatible with the one developed by Sun, entering into contracts requiring major independent software vendors to promote Microsoft's Java Virtual Machine exclusively,

and coercing Intel to stop aiding Sun in improving the Java technologies. 253 F.3d at 74. In *Conwood*, the conduct found to be exclusionary was defendant's pervasive practice of destroying competitor's racks and point of service materials and reducing the number of competitor's facings through exclusive agreements with and misrepresentations to retailers. 290 F.3d at 768. In *Caribbean Broadcasting Sys.*, defendants' fraudulent misrepresentations to advertisers and sham objections to a government licensing agency in order to defeat the application of a potential competitor were found to constitute anticompetitive conduct. 148 F.3d at 1087.

The court in *National Ass'n of Pharm. Mfrs.* did not reach the question of whether deception amounts to exclusionary conduct. 850 F.2d at 916-17. There, the Court of Appeals reversed an order dismissing the complaint and held that whether the publication of a letter to pharmacists alleged to have disparaged a competitor's drug stated a claim under Section 2 of the Sherman Act required an analysis of several factors – whether the representations were clearly false, clearly material, clearly likely to induce reasonable reliance, made to buyers without knowledge of the subject matter, continued for prolonged periods, and not readily susceptible of neutralization or other offset by rivals – and could not be adequately evaluated until the discovery process had moved forward. *Id.*

Other cases relied upon by Complaint Counsel do not hold that deception amounts to exclusionary conduct. *44 Liquormart* does not even address anticompetitive conduct. In *44 Liquormart*, Rhode Island's statute banning price advertising on liquor was found to constitute a blanket prohibition against truthful, nonmisleading speech about a lawful product and was held to abridge speech in violation of the First Amendment of the Constitution. 517 U.S. at 504, 516. In *Du Pont*, the Court of Appeals for the Second Circuit did not hold that deceitful conduct amounts to exclusionary conduct. Instead, in the language quoted by Complaint Counsel, the Second Circuit noted that "[i]n

prosecuting violations of the spirit of the antitrust laws, the Commission has, with one or two exceptions, confined itself to attacking collusive, predatory, restrictive, or deceitful conduct that substantially lessens competition." 729 F.2d at 137.

Thus, the cases relied upon by Complaint Counsel do not support a finding of exclusionary conduct from the facts established in this case. "Antitrust law is rife with . . . examples of what competitors find to be disreputable business practices that do not qualify as predatory behavior." *Taylor Publ'g Co.*, 216 F.3d at 476. To prove monopolization, even if JEDEC's rules were violated, Complaint Counsel would have to demonstrate that Rambus's conduct was exclusionary within the meaning of the antitrust laws – i.e., that it lacked a legitimate business justification. Complaint Counsel have failed to do so. Thus, exclusionary conduct, an element of Counts I, II, and III, has not been proved. Having so held, the analysis turns next to the issue of intent.

D. No Intent

1. Intent Defined

The Supreme Court, in *Aspen Skiing*, characterized intent as "merely relevant to the question whether the challenged conduct is fairly characterized as 'exclusionary' or 'anticompetitive'" in a monopolization claim. 472 U.S. at 602. The *Microsoft* court held: "in considering whether the monopolist's conduct on balance harms competition and is therefore condemned as exclusionary for purposes of § 2, our focus is upon the effect of that conduct, not upon the intent behind it. Evidence of the intent behind the conduct of a monopolist is relevant only to the extent it helps us understand the likely effect of the monopolist's conduct." *Microsoft*, 253 F.3d at 59 (citing *Chicago Bd. of Trade v. United States*, 246 U.S. 231, 238 (1918) ("knowledge of intent may help the court to interpret facts and to predict consequences"); *Aspen Skiing*, 472 U.S. at 603. To the extent that intent is an element for

proving the violations alleged, courts have described varying degrees of the level of intent required.

Count I, monopolization, has as one of its elements, "the *willful* acquisition . . . of [monopoly] power, as distinguished from growth or development as a consequence of a superior product, business acumen, or historic accident." *Grinnell*, 384 U.S. at 570-71 (emphasis added). "The willfulness element certainly requires proof of intent." *United States Football League*, 842 F.2d at 1359 (citing *Aspen*, 472 U.S. at 602 n.28). "Under § 2, intent to obtain a monopoly is unlawful only where an entity seeks to maintain or achieve monopoly power by anti-competitive means." *Endsley v. City of Chicago*, 230 F.3d 276, 283 (7th Cir. 2000) ("By intent we do not mean intent to obtain a monopoly or to capture an ongoing increase in market share. This of course is the aim of every business endeavor.").

Count II, attempt to monopolize, requires proof of a "specific intent" to accomplish the forbidden objectives; that is – "'an intent which goes beyond the mere intent to do the act.'" *Aspen Skiing*, 472 U.S. at 602 (quoting *United States v. Aluminum Co. of America*, 148 F.2d 416, 432 (2d Cir. 1945). Specific intent entails the intent to destroy competition, control prices, or build monopoly. *Times-Picayune Publ'g Co. v. United States*, 345 U.S. 594, 626 (1953); *McGlinchy v. Shell Chem. Co.*, 845 F.2d 802, 811 (9th Cir. 1988).

Count III, unfair methods of competition, also includes an inquiry into intent. *Du Pont*, 729 F.2d at 139. In the consent decree in *Dell*, the Commission expressly stated that its "order should not be read to create a general rule that inadvertence in the standard setting process provides a basis for enforcement action." *Dell*, 121 F.T.C. at 626. In other words, intent to mislead was an implicit element of the Commission's cause of action.

The intent necessary to support Counts I, II, or III – an intent to gain monopoly through anticompetitive conduct – must be

distinguished from an intent to achieve market position through lawful competition:

> The "intent" to achieve or maintain a monopoly is no more unlawful than the possession of a monopoly. Indeed, the goal of any profit-maximizing firm is to obtain a monopoly by capturing an ever increasing share of the market. Virtually all business behavior is designed to enable firms to raise their prices above the level that would exist in a perfectly competitive market. Economic rent – the profit earned in excess of the return a perfectly competitive market would yield – provides the incentive for firms to engage in and assume the risk of business activity. Monopolies achieved through superior skill are no less intentional than those achieved by anticompetitive means . . . . so the intent relevant to a § 2 Sherman Act claim is only the intent to maintain or achieve monopoly power by anti-competitive means.

Illinois, ex rel. Burris v. Panhandle E. Pipe Line Co., 935 F.2d 1469, 1481 (7th Cir. 1991).

2. Complaint Counsel Have Not Demonstrated That Respondent Intended to Mislead or Deceive JEDEC

Here, the anticompetitive conduct alleged by Complaint Counsel is that Respondent intentionally sought to mislead JEDEC through bad faith, deceptive conduct. Complaint Counsel must therefore prove that Rambus intended through its actions or omissions to mislead or deceive JEDEC by knowingly violating JEDEC rules or clear policies. *Cf. Pence v. United States*, 316 U.S. 332, 337 (1942) (for federal common law fraud claim, plaintiff must show that representation was made with knowledge of its falsity and with intent to deceive); *MCI Communications Corp. v. American Tel. & Tel. Co.*, 708 F.2d 1081, 1129 (7th Cir.

1983) (holding that a representation about products must be "knowingly false or misleading before it can amount to an exclusionary practice"); *ILC Peripherals Leasing Corp. v. International Business Machines Corp.*, 458 F. Supp. 423, 442 (N.D. Cal. 1978), *aff'd per curiam sub nom. Memorex Corp. v. IBM Corp.*, 636 F.2d 1188 (9th Cir. 1980) (granting directed verdict on monopolization and attempted monopolization claims based on allegedly misleading statements where there was "nothing knowingly false" about the representations).

The record evidence in this case does not prove that Respondent intentionally misled JEDEC or intentionally violated its rules. There is no direct evidence that Respondent misappropriated any information from JEDEC that it was not otherwise entitled to receive. Rambus, like other members, began attending JEDEC meetings, in part, to learn what the competition was working on. F. 914. Gordon Kelley, IBM JEDEC representative and JC 42.3 Chairman, along with Siemens JEDEC representative Willi Meyer, monitored JEDEC activities and reported to a joint DRAM development team that they had created expressly for that same purpose. F. 915.

Gordon Kelley testified that he did not feel "that the *use of JEDEC confidential information was an abuse as long as the people using the information were members*." F. 916 (emphasis supplied). It is also clear that membership in JEDEC entitled companies, *inter alia*, to receive minutes from JEDEC meetings, which record the key decisions that are made during the standard development process, including motions and votes. F. 255-56. The minutes were kept as a chronological statement of the events and occurrences at the meetings, including presentations on technological proposals. F. 256. The minutes of JC 42.3 meetings were also publicly available. F. 278. Thus, Rambus did not intentionally or secretly acquire any information from JEDEC that other member companies did not also have readily available.

Contrary to Complaint Counsel's assertions, the record shows numerous occasions when Rambus intentionally *disclosed* its proprietary RDRAM technology to DRAM manufacturers and systems companies. *E.g.*, F. 63, 102, 161. Apart from the early press events in 1992 and the numerous articles, marketing brochures and technical descriptions published on the subject, Rambus described its inventions through not only the '898 application, but also the PCT application, which was publicly available as of October 31, 1991. F. 97-219. The PCT application is identical in all material respects to the '898 application. F. 183-85. These descriptions continued with release of the '703 patent on September 7, 1993. F. 179-82. An analysis of any or all of these descriptions and the claims contained therein, should have raised concerns within the industry that Rambus might be able to obtain patents over the four technologies in issue.

Further evidence of Rambus's lack of intent to mislead or deceive JEDEC members is found in its meetings in October 1995 with several DRAM manufacturers in which Rambus expressly warned that it had or might obtain intellectual property rights that apply to SyncLink and new SDRAMs. F. 454-56. During this time, Rambus informed Intel that it did not see how future memory chips could meet performance goals without using some or all of Rambus's inventions. F. 863.

The record on this issue is conclusive. There was no duty under JEDEC rules that required Respondent to disclose its intellectual property. There is no evidence that Respondent acquired or intentionally misappropriated confidential JEDEC information that it was not otherwise entitled to have. There is no evidence that it ever made a knowingly false statement to JEDEC or member companies regarding its patent position. Given the widespread knowledge of Rambus's intellectual property in the DRAM industry, and Rambus's ongoing efforts to promote its technologies, including warning companies of possible infringement, there are no actions or omissions on behalf of Rambus which constitute an intent to mislead or deceive by

knowingly violating a JEDEC disclosure rule. Complaint Counsel's argument on this issue thus fails for lack of proof.

3. No Inference of Intent

Complaint Counsel alternatively argue that the requisite intent can, nevertheless, "be inferred from anticompetitive conduct." (CCPHB at 90 (citing *M&M Medical Supplies & Service, Inc. v. Pleasant Valley Hosp., Inc.*, 981 F.2d 160, 166 (4th Cir. 1993))). But that is true only if the conduct is clearly exclusionary. *Drinkwine v. Federated Publications, Inc.*, 780 F.2d 735, 740 (9th Cir. 1985) (where conduct was not "clearly threatening to competition or clearly exclusionary," specific intent element was missing). *See Tops Mkts., Inc. v. Quality Mkts., Inc.*, 142 F.3d 90, 101 (2d Cir. 1998) (a fact finder could infer intent from conduct that "was not motivated by a valid business justification"); *Thurman Industries, Inc. v. Pay 'N Pak Stores, Inc.*, 875 F.2d 1369, 1378 (9th Cir. 1989) (specific intent may be inferred by anticompetitive conduct only if the conduct is predatory or clearly in restraint of competition such as a *per se* violation under Section 1). Complaint Counsel have not shown that Respondent's conduct rises to such level. Under these facts, intent, having not been demonstrated, will not be inferred.

4. Other Factors Demonstrating That The Intent Element Is Not Met

A finding that Respondent had legitimate business justifications for not disclosing its patent claims, in addition to assessing whether conduct is exclusionary, can also preclude a finding of intent. *Technical Resource Services*, 134 F.3d at 1466-67 ("A fair and reasonable reading of the jury's verdict is that the jury chose to credit some or all of [defendant's] business justifications, and consequently concluded that [defendant] did not willfully maintain its monopoly and did not have the specific intent to achieve monopoly."); *Byars v. Bluff City News Co., Inc.*, 609 F.2d 843, 862 n.53 (6th Cir. 1980) ("valid business purpose

can offset a finding of monopolist intent"). Moreover, actions "predominately motivated by legitimate business aims . . . cannot bear out the specific intent essential to sustain an attempt to monopolize under § 2." *Times-Picayune*, 345 U.S. at 626. As set forth in Section III.C.3, *supra*, Respondent has demonstrated that its actions were not intentionally misleading or deceptive, but were, in fact, predominately motivated by legitimate business aims.

In addition, a finding that Respondent's acquisition of monopoly power in the relevant markets is attributable to its development of superior products defeats a finding of willful monopolization under the *Grinnell* standard. As set forth in Findings 1128-1402 and summarized below in Section III.F.2., JEDEC considered alternatives to the Rambus technologies, but rejected these alternatives as inferior. In addition, as described in Findings 1056-63 and summarized below in Section III.F.3., Rambus's technologies were utilized by the industry because of Intel's decision to incorporate RDRAM in its microprocessors. Because Respondent has demonstrated that its acquisition of monopoly power is a consequence of the market demand for Respondent's superior products, the intent element has not been satisfied. Having so held, the analysis turns next to the issue of causation.

E. No Causation

1. Causation Defined

"To establish a monopolization claim, the plaintiff must demonstrate that the defendant in fact acquired monopoly power *as a result* of unlawful conduct." *Association for Intercollegiate Athletics for Women v. N.C.A.A.*, 735 F.2d 577, 584 and 586 (D.C. Cir. 1984) (emphasis added); *Trans Sport*, 964 F.2d at 188 (To sustain a § 2 claim, "requires proof that the defendant willfully acquired or maintained its power, thereby *causing* unreasonable 'exclusionary,' or 'anticompetitive' effects.") (emphasis added)

(citations omitted). *See also Taylor*, 216 F.3d at 484 (§ 2 claim failed because plaintiff failed to show that its injuries were caused by defendant's conduct); *Concord Boat*, 207 F.3d at 1063 (§ 2 claim failed because plaintiff failed to establish antitrust injury or causation). In an attempted monopolization case, "a violation will only be found where there is a causal link between the anticompetitive behavior and the dangerous probability of success." *Ashkanazy v. I. Rokeach & Sons, Inc.*, 757 F. Supp. 1527, 1540 (N.D. Ill. 1991).

Causation is also an element of a cause of action for unfair methods of competition in violation of Section 5 of the FTC Act. *Du Pont*, 729 F.2d at 141 (Commission's order vacated where the record did not "contain substantial evidence . . . showing a causal connection between the challenged practices and market prices"); *In re Boise Cascade Corp.*, 113 F.T.C. 956, 993 (1990) (requiring "causal connection" between price discrimination and alleged resulting injury). *See also In re Ethyl Corp.*, 101 F.T.C. 425, 598 (1983) (Section 5 prohibits only conduct that leads to an undesired result (e.g., sustained supracompetitive prices) and violates the basic legislative goals of the Sherman Act.).

Antitrust cases based on subversion of a standard setting process also require the causal link to be proved. In *Indian Head*, the Court of Appeals found that defendant's behavior caused antitrust injury. 817 F.2d at 945. In *Clamp-All Corp.*, plaintiff's antitrust claim failed where there was no "concrete evidence that the submission of [defendant's] proposal caused (or even influenced) [the standard setting organization's] decision not to adopt any standard." *Clamp-All Corp. v. Cast Iron Soil Pipe Inst.*, 851 F.2d 478, 489 (1st Cir. 1988). In *Townshend*, the monopolization charge failed where plaintiff had "not asserted that the [standard setting organization] could have adopted a V.90 standard which did not encompass [defendant's] technology." *Townshend*, 2000 U.S. Dist. LEXIS 5070 at *33. Thus, the courts require causation – the showing of a causal link between the standard setting conduct and the adoption of a standard that

infringed the wrongdoer's patent. The court in *Townshend* distinguished the facts before it from those leading to the consent decree in *Dell*, stating that in *Dell*, the standards setting body was choosing among options, and there was a possibility that it could have adopted a standard which did not incorporate Dell's patent. *Id.* In the statement accompanying the consent decree, the Commission demonstrated the causal link. "[H]ad [the standard setting organization] known of the Dell patent, it could have chosen an equally effective, non-proprietary standard." *Dell*, 121 F.T.C. at 624 n.2. In contrast to the facts described in *Dell*, as discussed *infra* Section III.F.2, the facts here do not establish that JEDEC could or would have chosen an equally effective, non-proprietary standard.

2. No Causal Link Between JEDEC Standardization and Respondent's Acquisition of Monopoly Power

a. Rambus Did Not Acquire Monopoly Power by Virtue of JEDEC's Standard Setting

Although Complaint Counsel argue that Respondent acquired its monopoly power because its technologies were incorporated in the JEDEC standards, the evidence demonstrates that DRAM standards succeed, even if not selected by JEDEC, and fail, even if chosen by JEDEC. F. 1039, 1041. The network effects in the DRAM industry are weak, thus different DRAM standards can coexist in the market. F. 1037-38. Standardization by JEDEC is not necessary for marketplace success. F. 1039. For example, Samsung brought technology to JEDEC for standardization, but JEDEC declined to adopt it. Samsung produced the product anyway and it became a high volume DRAM product. F. 1039. Similarly, reduced latency DRAM ("RLDRAM") was developed and produced by Infineon and Micron with little or no involvement by JEDEC. F. 1040. Standardization by JEDEC is also sometimes insufficient to ensure market success. For example, JEDEC standardized Burst EDO, yet it failed in the marketplace. F. 1041.

The publication of JEDEC's SDRAM standard was insufficient to ensure market success or even interoperability. F. 1043. Prompted by these incompatibilities, Intel – not JEDEC – developed the "PC SDRAM" standard in 1996. F. 1044. The Intel PC SDRAM specification set forth what would become the industry specification for PC100 SDRAM. F. 1045. The PC133 SDRAM standard was developed by DRAM manufacturers and Personal Computer ("PC") Original Equipment Manufacturers ("OEMs") and was later incorporated into the Intel PC SDRAM standard. F. 1047. Intel's adding of the PC SDRAM standard specifications demonstrates that there are powerful forces in the DRAM industry that affect DRAM standards. F. 1048. Formal standard setting is therefore not the only way in which an iteration of DRAM can become prominent.

Rambus did not obtain additional market power due to any alleged failure to disclose its intellectual property interests before standardization by JEDEC. Standardization of the Rambus technologies by JEDEC did not reduce the substitution possibilities of alternatives, and Rambus's market power was unchanged by formal standard setting by JEDEC. *See* F. 1051. In addition, Rambus did not obtain or retain any additional market power due to any alleged failure to disclose its intellectual property interests after standardization by JEDEC (i.e., *ex post*) because, even after standardization, switching costs would not have prevented a shift to an available technology that was as good or better than Rambus's technology. F. 1645-65. Thus, Respondent's acquisition of monopoly power is not attributable to the inclusion of its technology in JEDEC standards.

b. Rambus Acquired Monopoly Power as a Result of its Superior Technology and Intel's Choice of its Technology

Intel's choice of Rambus's proprietary DRAM ("RDRAM") conferred monopoly power. F. 1056-63. Intel played a significant

role in selecting among future memory architectures. Intel built both microprocessors and chipsets that connected the microprocessors to the system main memory. Intel controlled eighty percent of the market for microprocessors used in personal computers. F. 1060. Intel saw a growing performance gap in the mid-1990's between central processing unit ("CPU") performance and DRAM performance. F. 1056. After examining the alternatives for a year, Intel chose RDRAM to be its next generation DRAM technology. F. 1058. Intel chose RDRAM because of the need for higher bandwidth for use with faster CPUs and the desire to satisfy memory needs driven by more I/O demands and new applications. F. 1060.

Intel's choice of RDRAM was significant. Representatives of Advanced Micro Devices ("AMD"), Intel's competitor in the microprocessor market, explained that, in the late 1990's, AMD believed RDRAM would become the next volume memory product and a *de facto* standard because it had been chosen by Intel. "Given that . . . Intel . . . owns 80% of the market . . . our customers were saying . . . Rambus, it's a revolutionary change . . . but, you know, that's the way industry is going, that's the way we're going to go, and Rambus is it." F. 1060. "[Intel] drove the volume, and if the volume DRAM was Rambus that would become the commodity part if the indications were most of the DRAMS in the world were going to be Rambus DRAM's, we better be compatible with them." F. 1061.

Intel's selection of RDRAM was also significant to the PC OEMs. F. 1062. A representative of Compaq explained Compaq's sentiment in 1998 that "Rambus is the clear next generation memory" as based on the fact that Intel had told Compaq that Intel was going to produce chip sets for RDRAM. F. 1063. This is significant because ninety percent of Compaq's PC applications used Intel chipsets. F. 1063. Thus, it was Intel's selection of Rambus's superior technologies that created market power. This conclusion is strongly supported by evidence of the extraordinary reaction and resulting conduct of certain DRAM manufacturers to

Intel's announcement in 1996 that it would exclusively support RDRAM as its next generation of main memory. See F. 437-586.

For these reasons, and, as discussed in a following section, because Respondent's technologies were superior to any proposed alternative, Complaint Counsel have not demonstrated that Respondent acquired monopoly power as a result of unlawful conduct. The analysis continues with an examination of the issue of reliance.

3. No Reasonable Reliance by JEDEC

Antitrust cases based on misrepresentations require evidence of reliance. In a monopolization case based on a patent allegedly procured by fraud on the PTO, the plaintiff must make a "clear showing of reliance, i.e., that the patent would not have issued but for the misrepresentation or omission" that "cause[d] the PTO to grant an invalid patent." *Nobelpharma AB v. Implant Innovations, Inc.*, 141 F.3d at 1070-71. To prove that false and misleading advertising or defamation constitutes exclusionary conduct requires proof that consumers are clearly likely to reasonably rely on the misrepresentations. *American Professional Testing Serv. v. Harcourt Brace Jovanovich Legal & Professional Publ'g,* 108 F.3d 1147, 1152 (9th Cir. 1997); *National Ass'n of Pharm. Mfrs. v. Ayerst Labs.*, 850 F.2d 904, 916 (2d Cir. 1988).

To the extent that Complaint Counsel's Section 5 cause of action is based upon a breach of a duty to disclose, if any duty existed and if Respondent had breached any such duty, Complaint Counsel would still have to demonstrate that JEDEC members relied upon Respondent's omissions or misrepresentations and that such reliance was reasonable. A plaintiff making similar allegations in support of a fraud claim would have to prove that JEDEC and its members acted in reliance on Rambus's alleged failure to disclose. *See Alicke v. MCI Communications Corp.*, 111 F.3d 909, 912 (D.C. Cir. 1997) (federal common law fraud and unfair trade practice); *Bank of Montreal v. Signet Bank*, 193 F.3d

818, 827 (4th Cir. 1999) (under Virginia law, fraud by omission requires a showing that the accused knew "the other party [was] acting upon the assumption that the [concealed] fact does not exist") (internal quotation marks omitted).

In addition, Complaint Counsel bear the burden of proving that such reliance is reasonable. "The 'justifiable reliance' requirement ensures that a causal connection exists between the misrepresentation and the plaintiff's injury." *Grubb v. Federal Deposit Ins. Corp.*, 868 F.2d 1151, 1162 (10th Cir. 1989). Where a party had information available that put him on notice that the representations could not be trusted, reliance on those representations is not reasonable. *See, e.g., Hershey v. Donaldson, Lufkin & Jenrette Sec. Corp.*, 317 F.3d 16, 25 (1st Cir. 2003). Moreover, where a plaintiff has made an investigation, even a partial investigation, reliance on the misrepresentation is not reasonable. *See, e.g., Bank of Montreal*, 193 F.3d at 827.

The record evidence shows that members of JEDEC did not rely on any omission by Rambus and that, if they had, such reliance would not have been reasonable. As set forth in Findings of Fact F. 58-219 and 786-901, and summarized below, JEDEC and its members were well aware that Rambus was seeking broad patent protection for its inventions and knew that Rambus might obtain patent claims covering features being considered for standardization.

As noted in Section III.D.2., the DRAM industry was well aware of Rambus's inventions. The DRAM industry was also aware of Rambus's business model and witnesses testified that they understood that Rambus would seek broad patent protection of its inventions. F. 164; *see* F. 808, 877-901. The technologies had been first disclosed in 1989-90 when Drs. Farmwald and Horowitz made visits to many DRAM manufacturers (including Texas Instruments, IBM, Toshiba, Fujitsu, Mitsubishi, NEC, Matsushita, Micron and Siemens) and systems companies (including Sun Microsystems, Motorola, Apple, SGI and Tandem)

to try to convince them about the benefits of their approach and to get feedback from them. F. 102-04. In the 1990-91 period, Dr. Horowitz prepared detailed technical descriptions of the Rambus technology for use with customers and potential customers to convince them of the merits of Rambus technology and to help them build it. F. 110-21. A still later Rambus technical description was released on April 1, 1991 which was a more complete version with many more technical details. F. 130-34. Rambus subsequently entered into non-disclosure agreements to protect its proprietary technology. F. 63, 159-66.

On March 9, 1992, Rambus held simultaneous events in the Silicon Valley and in Tokyo to publicly announce its technology and business plan. F. 135. Rambus produced and distributed its first marketing brochure about Rambus technology which disclosed the four features of Rambus technology at issue here. F. 149-53. In connection with the public announcement of Rambus's technology and business plan in March 1992, Rambus provided information to the press regarding Rambus's inventions, and numerous articles about Rambus appeared. F. 144. Many of these articles contained a significant amount of technical detail. For example, an article entitled "Rambus Unveils Revolutionary Memory Interface" in the March 4, 1992 Microprocessor Report describes Rambus's technology in some depth and describes three of the four features of Rambus technology at issue here, as well as aspects of the fourth. F. 145-48. In addition, The Journal of Solid State Circuits, the most widely read journal for circuit designers, published a paper about the Toshiba 4.5 megabit Rambus DRAM. F. 158.

Indeed, the evidence shows that members of JEDEC were also aware of the technologies invented by Rambus. As noted in Section III.B.4, G. Kelley, IBM representative and JC 42.3 subcommittee chair, prepared a "Rambus Assessment" from which it is clear that he was aware of Rambus technology and the possibility that Rambus might assert some intellectual property claims over SDRAM. F. 791-95. On this point, Siemens JEDEC

representative Willi Meyer observed: "IBM is still keeping its eye on [Rambus] . . . . IBM is seriously considering to preemptively obtain a license as soon as possible." F. 797.

As a result of the May 1992 episode, when Crisp declined to comment on whether Rambus had patents or potential patents (F. 819), in a June 1992 follow-up meeting presentation, Gordon Kelley specifically noted "Patent Problems? (Motorola/Rambus)." F. 831. At this same meeting, Sussman of NEC stated that he had reviewed Rambus's PCT application and noted that nothing in the application "related to the work ongoing at JEDEC." F. 810, 828. There was additional discussion of the PCT application at the September 1993 meeting, including comments that the claims were barred by prior art; copies of the application were offered to the members of JEDEC. F. 836-41.

During this period, DRAM manufacturers and members of JEDEC were actively following and continuing to investigate Rambus's patent portfolio. Siemens's representative Meyer testified he obtained the serial number for Rambus's WIPO application and "sent it back to the [Siemens] patent department" for analysis. F. 840. Thereafter, in March 1994, Meyer, in a clearly foreboding comment, noted: "[a]ll computers will (have to be) built like this someday, but hopefully without royalties to Rambus." F. 841.

In 1995, Rambus informed LG Semiconductor, Samsung, NEC, OKI, Intel and Micron Technologies that SDRAMs might infringe on Rambus's patents. F. 859-63. Micron's concern about Rambus's intellectual property was evident in 1995 and 1996, when executive Jeff Mailloux sent a memorandum entitled, "Rambus Inc. Patents" to several Micron employees, including JEDEC representative Terry Walther, attaching abstracts of Rambus patents for an analysis of "both the quality (is there prior art?) and the breadth (apply to more than just RAMBUS?"). F. 864. Mailloux subsequently advised Micron CEO Steve Appleton in December 1996, that "from our research, we think many

Rambus patents read on prior art or other patents." F. 878. At the same time, Mitshubishi's Japanese patent department was reviewing Rambus intellectual property for any prior art. F. 865.

After Rambus withdrew from JEDEC in June 1996, JEDEC members continued to engage in continuing discussions about Rambus intellectual property. F. 877-901. By 1997, numerous emails by Micron employees suggest ongoing concerns with Rambus patents. F. 884-96. By March 1997, Terry Lee of Micron agreed that he thought that Rambus might have intellectual property claims relating not just to RDRAMs but to the work of the JEDEC JC 42.3 committee as well. F. 808.

Similarly, the SyncLink Consortium was well aware that their work could or would violate the claims in Rambus's pending patent applications if those applications issued as patents. For example, a September 1995 trip report by Motorola JEDEC representative Mark Farley stated that "SyncLink told Motorola confidentially that there were very likely patents violated by their proposal." F. 856. The January 1996 SyncLink Consortium meeting minutes state that "Rambus says their patents may cover our SyncLink approach even though our method came out of early RamLink work." F. 866. Dr. Gustavson determined that Rambus's pending European patent applications covered everything that the Ramlink and SyncLink groups were doing, but concluded that the applications would never issue. F. 867. Crisp's May 1997 email reports that a VIA Technologies executive had said that "he thinks that SyncLink is going to be stepping all over Rambus patents." F. 898. The January 1997 SyncLink Consortium meeting minutes show a desire to "collect information relevant to prior art and Rambus filings," because of a concern that "Rambus will sue individual companies" for patent infringement." F. 899. Many of the SyncLink Consortium and IEEE members were also members of JEDEC. *See* F. 438, 464; *see also* Respondent's Submission Regarding Company Attendance at SyncLink and JEDEC 42.3 Meetings, filed October 28, 2003.

This evidence, along with the Findings of Fact regarding the response of certain individuals in the DRAM industry to Intel's decision to adopt RDRAM for its desktop memory architecture, demonstrates that members of JEDEC investigated Rambus's intellectual property, dismissed it as a collection of prior art despite Rambus's warnings that it would enforce its patents, and made the strategic decision to introduce the claimed Rambus technology into the JEDEC standards. On these facts, there can remain little doubt that JEDEC, if not the majority of the DRAM industry, was on notice and fully aware of Rambus's patent portfolio, and therefore could not have reasonably relied on any alleged misrepresentation or omission by Respondent in failing to disclose such technology to JEDEC.

4. No Inference of Causation

Complaint Counsel acknowledge that "there must be a causal link between the conduct at issue and the acquisition of monopoly power." CCPHB at 107 (citing T. Muris, *The FTC And The Law Of Monopolization*, 67 ANTITRUST L.J. 693, 694 (2000)). However, Complaint Counsel assert that they do not have to prove a causal link; rather, they urge, causation can be inferred from the allegedly anticompetitive conduct itself. CCPHB at 107-08. For this proposition, Complaint Counsel rely on the statement by the Court of Appeals in the *Microsoft* case that "courts will infer 'causation'" from conduct that "'reasonably appear[s] capable of making a significant contribution to . . . monopoly power.'" CCPHB at 107 (quoting *Microsoft Corp.*, 253 F.3d at 79). However, *Microsoft* does not support Complaint Counsel's proposition on the facts presented in the instant case.

In *Microsoft*, the government proved the first basic element of causation: that Microsoft had engaged in a widespread pattern of anticompetitive and exclusionary conduct that had the purpose and effect of denying rival Netscape access to the most effective means of distribution which made it impossible for Netscape to compete effectively against Microsoft. *Microsoft*, 253 F.3d at 58,

64-67, 78; *United States v. Microsoft Corp.*, 87 F. Supp. 2d 30, 39 (D.D.C. 2000), *aff'd in relevant part*, 253 F.3d 34 (D.C. Cir. 2001). The court found, that, but for that conduct, Netscape might have flourished as an internet browser in competition with Microsoft's Internet Explorer browser and that a successful Netscape browser might have served as a middleware platform that would have stimulated entry into the desktop operating system market and thus eroded Microsoft's monopoly there. *Microsoft*, 253 F.3d at 79; 87 F. Supp. 2d at 38-39. The court also found that Microsoft's success in crippling Netscape by its exclusionary conduct made it impossible for the court to determine directly whether these other subsequent events would have occurred. *Microsoft*, 253 F.3d at 79. Under those circumstances, the court said that, for purposes of determining liability, it would infer that Microsoft's exclusionary conduct had the required effect on competition. *Id.* at 78-79.

The facts of this case are distinguishable on two grounds. First, while, in *Microsoft*, the government *proved* that Microsoft's conduct had the alleged effect on Netscape, Complaint Counsel, in this case, want to *infer* that first step of causation (i.e., that JEDEC would have adopted a different standard). *See* CCPHB at 107. Second, the subsequent events alleged by the government in the *Microsoft* case – the development of Netscape into a middleware platform and the resulting new entry into the operating system market – had no historical precedents, and Microsoft's conduct made it impossible for the court to know whether that unprecedented chain of events would have ensued if Microsoft had not excluded Netscape from the effective means of distribution. 253 F.3d at 78-79.

Here, by contrast, there is substantial experience with the events alleged by Complaint Counsel. The evidence clearly demonstrates that Complaint Counsel have failed to prove the required "causal link" between the challenged conduct and Respondent's market power. Short of such proof, nothing in *Microsoft* allows causation to be inferred by the Court. Thus,

causation, an element of Counts I, II, and III, has not been proved. Having so held, the analysis proceeds to the issue of anticompetitive effects.

F. No Anticompetitive Effects

1. Anticompetitive Effects Defined

"To sustain a § 2 claim, the plaintiff must prove not only that the defendant had the power to monopolize, but also that it willfully acquired or maintained its power, thereby causing unreasonable 'exclusionary,' or 'anticompetitive' effects." *Trans Sport*, 964 F.2d at 188 (internal citations omitted). "[T]o be condemned as exclusionary, a monopolist's act must have an 'anticompetitive effect.' That is, it must harm the competitive process and thereby harm consumers." *Microsoft*, 253 F.3d 58. "[T]he plaintiff, on whom the burden of proof of course rests must demonstrate that the monopolist's conduct indeed has the requisite anticompetitive effect." *Id. See also* Muris, 67 ANTITRUST L.J. at 695 ("exclusionary conduct can be condemned as monopolistic only after a full analysis, including consideration of whether the practice in fact has an anticompetitive impact").

In an attempted monopolization case, while actual effects are not necessary, courts must find threatened anticompetitive effects. *Taylor Publ'g Co.*, 216 F.3d at 474 ("in an attempt case we focus on the harm that potentially might have been caused by the conduct in light of the state of the market").

Effects must also be proved to support a cause of action for unfair methods of competition in violation of Section 5 of the FTC Act. *See Atlantic Refining*, 381 U.S. at 370 (Supreme Court upheld Commission's cease and desist order, noting "[i]t is beyond question that *the effect* on commerce was not insubstantial."); *Boise Cascade Corp. v. FTC*, 637 F.2d 573, 582 (9th Cir. 1980) (absence of evidence reflecting an anticompetitive effect rendered Commission order unenforceable). *See also In re*

Ethyl, 101 F.T.C. at 598 (application of Section 5 requires careful review of the facts to insure there is persuasive evidence of effects); *In re General Motors Corp.*, 103 F.T.C. 641, 701 (1984) (declining to find violation of Section 5 where there had been no demonstration of an anticompetitive impact).

Complaint Counsel assert that the anticompetitive effects in this case are substantial costs on DRAM makers, including but not limited to the costs of the anticompetitive and discriminatory royalties that Respondent has charged. CCPHB at 14. Complaint Counsel further assert that Respondent's conduct threatens to lead to increases in prices in SDRAM and DDR SDRAM devices, disrupt JEDEC's ability to develop timely DRAM industry standards, impose additional costs on DRAM makers, who may be forced to expend resources in developing and implementing alternative standards that avoid Respondent's patents, and discourage industry participation in standards organizations, while at the same time discouraging reliance upon standards developed by such organizations. CCPHB at 14.

However, as described above, Complaint Counsel have not proved that Respondent acquired its market power through anticompetitive conduct, as distinguished from Respondent's development of superior technologies. Further, as set forth below, Complaint Counsel have not demonstrated that JEDEC would have chosen different standards had Respondent made the disclosures Complaint Counsel allege should have been made. In addition, Complaint Counsel did not prove that Respondent's conduct resulted in higher prices to consumers. Thus, Complaint Counsel have not demonstrated that Respondent's conduct resulted in any anticompetitive effects.

2. Complaint Counsel Have Not Demonstrated That There Were Viable Alternatives to Rambus Technologies

Complaint Counsel have not proved that if Respondent had made additional disclosures, JEDEC could or would have adopted any viable alternatives to the Rambus technologies. F. 1128-1402. Complaint Counsel state that they do not bear the burden of showing that the proposed alternative technologies were non-infringing. CCPHRB at 56. Complaint Counsel suggest that, instead, the burden rests upon Respondent, as the patent holder, to show the absence of non-infringing alternatives. CCPHRB at 57, citing, among other authorities, *Nutrinova Nutrition Specialties and Food Ingredients GMBH v. International Trade Comm'n*, 224 F.3d 1356, 1359 (Fed. Cir. 2000) ("As a general proposition, the law places the burden of proving infringement on the patentee who alleges it."). It is true that in patent infringement suits, the burden rests upon the patent holder to show that the party alleged to have infringed did infringe. *See, e.g.*, *Carroll Touch, Inc. v. Electro Mechanical Systems, Inc.*, 15 F.3d 1573, 1578 (Fed. Cir. 1993). However, Complaint Counsel, as the proponent of the factual proposition that JEDEC could have chosen alternatives, has the burden of proof thereto. *See* 16 C.F.R. § 3.43(a). A recent decision by the Commission is instructive on this issue.

In *In re Schering-Plough*, perhaps the most important issue in the underlying patent litigation between Schering Plough and Upsher-Smith, which resulted in a settlement agreement found by the Commission to be anticompetitive, was whether the product made by Upsher, the generic manufacturer, infringed on Schering's branded, patented product. *In re Schering Plough Corp.*, 2003 FTC LEXIS 187, *69-70 (2003). The Commission held: "We cannot assume that Schering had a right to exclude Upsher's generic competition for the life of the patent any more than we can assume that Upsher had the right to enter earlier." *Id.* In so holding, the Commission thus *refused to assume* that an alleged infringer's product did not infringe. Yet this is precisely

what Complaint Counsel seek here: an assumption by the Court that the alternatives to Rambus's technologies considered by JEDEC and proposed by Complaint Counsel's technical expert did not infringe. In this case, which is *not* a patent infringement suit, such an assumption, in lieu of demonstrable proof by the proponent, is unwarranted.

In addition, it is not sufficient for Complaint Counsel to simply assert that alternatives were available, acceptable, and noninfringing. "Mere speculation or conclusory assertions will not suffice"; rather, there must be "concrete factual findings" sufficient to support an inference that acceptable alternatives were available. *Grain Processing Corp. v. American Maize-Products Co.*, 185 F.3d 1341, 1353 (Fed. Cir. 1999). *See also Du Pont*, 729 F.2d at 141-42 (finding insufficient the testimony of complaint counsel's expert that the market would have operated differently absent these practices without estimating the extent of that difference). Whether Complaint Counsel established that viable alternatives were available with respect to the disputed Rambus technologies follows.

a. Programmable CAS Latency

Complaint Counsel, through the testimony of their technical expert, Professor Jacob, did not demonstrate that there were viable alternatives to programmable CAS latency in SDRAMs and DDR SDRAMs because the evidence presented shows that the use of fixed CAS latency parts would have required multiple fixed CAS latency parts, leading to higher costs and logistical difficulties for DRAM manufacturers and users. F. 1136-64. Programming CAS latency with fuses, as with the fixed CAS latency alternative, would have required multiple parts with different CAS latencies, leading to higher costs and logistical difficulties for DRAM manufacturers and users. F. 1165-77. Scaling CAS latency with clock frequency would have resulted in higher costs and, upon a formal infringement analysis, might be found to infringe Rambus's patents. F. 1178-86. Using dedicated pins on the

DRAM to select CAS latency would be more expensive and less reliable. F. 1187-1200. Identifying CAS latency in the read command would still require storing latency information in a programmable register like the mode register in SDRAMs. F. 1201-06. Staying with asynchronous technology was not a viable alternative because asynchronous technology was not capable of achieving the performance necessary for high speed operation. F. 1207-14.

b. Programmable Burst Length

Complaint Counsel, through the testimony of Professor Jacob, did not demonstrate that there were viable alternatives to programmable burst length in SDRAMs and DDR SDRAMs because the evidence presented shows that the use of fixed burst length parts would have required multiple fixed burst length parts, leading to higher costs and logistical difficulties for DRAM manufacturers and users. Setting burst length with fuses would have required multiple parts with different burst lengths, leading to higher costs and logistical difficulties for DRAM manufacturers and users. F. 1216-30. Using dedicated pins on the DRAM to identify burst length would be significantly more expensive and, upon a formal infringement analysis, might be found to infringe Rambus's patents. F. 1239-45. Using dedicated pins to explicitly identify burst length in the read command, upon a formal infringement analysis, might also be found to violate Rambus patents. F. 1246-47. Using a burst terminate command would result in significantly lower performance. F. 1248-56. Using a CAS pulse to control data output would lead to cost, testing and performance problems. F. 1257-59.

c. Dual-edge Clocking

Complaint Counsel, through their expert's testimony, did not demonstrate that there were viable alternatives to dual-edge clocking in DDR SDRAMs because the evidence presented shows that interleaving on-chip banks suffer from performance and cost

disadvantages and, upon a formal infringement analysis, might be found to infringe Rambus patents. F. 1281-91. Interleaving on-module ranks would be significantly more expensive, have performance problems, and provide less flexibility than dual-edge clocking and would not be available for all applications. F. 1292-1305. Increasing the number of pins on the DRAM would be significantly more expensive, in addition to having performance problems. F. 1306-16. Increasing the number of pins per module would be significantly more expensive and would be unavailable in certain applications. F. 1317-21. Doubling the clock frequency would be significantly more expensive, in addition to being difficult to implement and having performance problems. F. 1322-35. Using simultaneous bidirectional I/O drivers would be very expensive and difficult, if not impossible, to implement and would not provide the performance of dual-edge clocking. F. 1336-41. Toggle mode would be significantly more expensive and could not achieve the performance of DDR SDRAMs with dual-edge clocking. F. 1342-49.

d. On-Chip DLL

Complaint Counsel, through Professor Jacob's testimony, did not demonstrate that there were viable alternatives to on-chip delay locked loop ("DLL") in DDR SDRAMs because the evidence presented shows that putting a DLL on the memory controller would not be sufficient for high speed performance. F. 1358-60. Putting a DLL on the module would be significantly more expensive and difficult to implement. F. 1361-69. Using a vernier method would not be sufficient for high speed performance and, upon a formal infringement analysis, might be found to infringe patents. F. 1370-77. Using more DRAM pins and not clock frequency is the same as the alternative proposed of using more pins per DRAM rather than using dual-edge clocking and thus suffers from the same infirmities and the same performance and cost disadvantages. F. 1378-80. Relying on the DQS data strobe would not be sufficient for high speed performance. F. 1381-84. Read clocks would have required

relying on a strobe and would have still required a DLL. F. 1385-87.

In drawing these conclusions, the Court notes Professor Jacob's lack of experience in DRAM circuit design. Aside from reviewing some DRAM data sheets, Professor Jacob had no particular DRAM-related experience in the mid-1990's. F. 1128. By contrast, Respondent's technical experts, Dr. Soderman and Michael Geilhufe, have a combined sixty years of experience in the DRAM and semiconductor industries involving the design of DRAMs, as well as various other types of integrated circuits. F. 1129-30. Their testimony effectively rebutted the conclusions put forth by Professor Jacob with respect to the issue of viable alternatives. F. 1128-34. Moreover, in considering Professor Jacob's testimony, the Court notes that his methodology failed, *inter alia*, to employ software simulation to model the performance of the alternatives that he proposed; failed to provide sufficient detail to enable an actual circuit design for the proposed alternatives; and failed to do any investigation to determine whether the proposed alternatives were covered by patents held by Rambus or others. F. 1128-34. Having so concluded, the Court next considers the economic evidence presented in this case.

3. Analysis of the Economic Evidence

a. The Methodology Used by Complaint Counsel's Economic Expert Is Flawed

At trial, Complaint Counsel's economic expert, Professor McAfee, testified that he believed that equal or superior alternatives were excluded by Rambus's alleged conduct. F. 1096. However, Professor McAfee's definition of "equal or superior" is flawed, as it does not stand up to the rigors of traditional economic analysis. F. 1096. To determine whether equal or superior alternatives were excluded, Professor McAfee evaluated whether alternatives were "commercially viable." F. 1096-98. According to Professor McAfee, an alternative was

"commercially viable" if it constrained the price of Rambus's technologies. F. 1098. But defined that way, the concept of "commercially viable" does not mean that the technology is "equal or superior," as even weak substitutes can constrain the price of a technology. F. 1098. Further, when determining whether an alternative was price constraining, Professor McAfee did not consider the price level required before the alternatives would actually constrain the price. F. 1099. Thus, even if alternatives were "price constraining" with respect to Rambus's technologies, that does not make them a viable alternative that would have been chosen by JEDEC. F. 1098, 1483. A technology that is price constraining is not the same as an economic substitute. F. 1483. An economic substitute must be equivalent in terms of cost-performance features. F. 1483. What is important to compare is the overall attractiveness of the alternatives on a quality/cost-adjusted basis. F. 1483-84. Although he claimed that his methodology was "parallel" to standard economic tests, Professor McAfee admitted that he was aware of no economic literature that describes the use of a "commercial viability" test to determine market substitutability of alternatives. F. 1097.

Rather than examining the actual cost differences between the Rambus technologies and the proposed alternatives, Professor McAfee opined that he had considered an amalgam of factors and determined that certain alternatives were "commercially viable" based on the information he analyzed. F. 1091, 1106. The information upon which Professor McAfee tied his notion of commercial viability included the subjective perceptions of JEDEC members at the time, regardless of whether those perceptions were ultimately correct. F. 1100. While this factor may speak to whether JEDEC would have selected a technology, it does not go to whether an alternative is equal or superior in objective terms. F. 1103. Further, while Professor McAfee testified that it was likely that at least one of the technologies he deemed to be a commercially viable alternative to Rambus's technology was equally efficient or superior to Rambus's

technology, he could not identify any such technology as equal or superior. F. 1107.

In addition, several economic assumptions made by Professor McAfee, when measured against the Court's findings on the evidence, undermine the stated opinions that rely on those assumptions. For example, Professor McAfee admitted that the only "candidate purpose" he considered for Rambus's decision to withhold patent information from JEDEC was monopolization, i.e., McAfee did not consider other purposes, such as the protection of trade secrets, that might have led Rambus to take the risk that McAfee identified. F. 1071. In addition, Professor McAfee erroneously judged patented technologies to be "hobbling" because he believed, contrary to the evidence, that JEDEC rules put a "penalty" on technologies that were covered by intellectual property. F. 1101. He thus regarded patented technologies, such as Rambus's, as inferior based on the presence of intellectual property issues without regard to the level of royalties sought for the technology. F. 1101.

Similarly, Professor McAfee relied on his notion of "satisficing" to conclude, in effect, that the term "equal" included technologies that were inferior to Rambus's technologies. F. 1105. Professor McAfee defined satisficing as refering to the process by which an organization like JEDEC will choose an adequate solution to a problem it faces rather than expending the effort to find the perfect solution. F. 1105. However, the conclusion that JEDEC would have adopted Rambus's technologies in SDRAM and DDR once it received a RAND assurance from Rambus is not undermined by the possibility that JEDEC might have been satisficing. F. 1485. If JEDEC had avoided patented technologies in favor of alternative technologies without a lot of analysis, it would not have been satisficing; such conduct is merely biased behavior. F. 1485. If JEDEC were satisficing, it would be willing to go forward with patented technology upon the receipt of a RAND letter. F. 1485.

Professor McAfee based his analysis that Rambus's conduct was exclusionary on several mistaken assumptions, including the assumption that Rambus's conduct constituted a violation of a JEDEC rule or process and that Rambus had made misrepresentations to JEDEC. F. 1110-18. McAfee further assumed that Rambus knowingly took a risk that it might lose the ability to enforce its patents by not disclosing patent interests, but conceded that Rambus would have understood that Rambus's enforcement of its patents, once they issued, would have triggered an inquiry into whether Rambus should have disclosed its patents. F. 1108-09. Professor McAfee admitted that exclusion of inferior products from the market is not exclusionary in an economic sense. F. 1088.

Professor McAfee further admitted that he had done no analysis to determine the economic efficiency of JEDEC's rules or whether they advanced the interests of antitrust law. F. 1120-21. Professor McAfee admitted that JEDEC's disclosure rules do little to mitigate risk of hold up because the disclosure obligation applies only to the knowledge of the representative at the meeting, rather than that of the member company. F. 1126. Professor McAfee further admitted that it is plausible with his assumptions that if Rambus never joined JEDEC, JEDEC would still have selected the four Rambus technologies for inclusion in its standards. *See* F. 1127.

b. In the "But/For" World, JEDEC Would Not Have Rejected the Rambus Technologies Even if Alternatives Did Exist and Rambus Had Made the Additional Disclosures

Professor Teece's testimony on this issue is highly persuasive. Professor Teece is a chaired professor in the School of Business at the University of California at Berkeley. F. 1404. He is also the Director of the Institute for Management, Innovation, and Organization at the University of California at Berkeley. F. 1404. Professor Teece's specialization within the field of industrial

organization is in technology policy and particularly antitrust policy as it relates to high technology industries. F. 1408. He also has substantial expertise in the area of the economics of standard setting. F. 1409.

The "but/for" world may be analyzed by the use of a decision tree, which is a device commonly used in economics to understand the different possible scenarios and outcomes in a "but/for" world. F. 1411. In this case, the decision tree starts with the assumption that Rambus made the additional disclosures that Complaint Counsel allege Rambus should have made. F. 1412. Had Rambus made these additional disclosures, JEDEC would have had a choice; it could either proceed without seeking a RAND letter from Rambus, or it could ask Rambus to provide a RAND letter. F. 1412. If JEDEC had asked for a RAND letter, Rambus would have to decide whether to give a RAND letter. F. 1412. If Rambus agreed to give a RAND letter, JEDEC members would (as a theoretical matter) have sought to negotiate licenses from Rambus before the standard was adopted and before any relevant patents issued (*ex ante*) or it could have proceeded without such negotiations. F. 1412. If there were no *ex ante* negotiations, JEDEC could have adopted the standards incorporating Rambus's technologies or it could have adopted different standards. F. 1412. Had JEDEC adopted the same standards as it actually adopted, the same outcome would have occurred in the but/for world as in the actual world. F. 1413.

An economic analysis shows that there are a number of considerations that suggest that JEDEC might not have sought a RAND assurance from Rambus even if Rambus had made the disclosures. First, JEDEC might have perceived that Rambus was trying to derail the standard setting process by gaming the system. F. 1414-1415. Second, JEDEC might not have asked for a RAND letter because members might have believed that Rambus would not obtain patents (because of invalidity based on prior art) that would cover products consistent with the JEDEC standard. F. 1416. Third, JEDEC might not have asked for a RAND letter

from Rambus because, in the real world, JEDEC did not seek, and to this day has not sought, a RAND assurance from Rambus regarding SDRAM, DDR or DDR2, despite JEDEC's knowledge of and concerns about Rambus's patent coverage. F. 1417. Litigation between Rambus and various DRAM manufacturers would not explain JEDEC's failure to seek RAND assurances from Rambus. F. 1418. JEDEC had previously sought RAND assurances from Texas Instruments regarding the Quad-CAS technology even though Texas Instruments was in litigation with Micron at the time. F. 1418.

Had Rambus made the additional disclosures that Complaint Counsel contend it should have made and had JEDEC not sought a RAND letter, economic analysis shows that JEDEC would have adopted the same standards that it did in the real world – the standards incorporating Rambus's technologies. F. 1419. Complaint Counsel's expert, Professor McAfee conceded that in such a case, "it would lead to the same outcome as the actual world." F. 1419.

The economic evidence further shows that had JEDEC sought a RAND assurance, it still would have adopted Rambus's technologies. F. 1435-85. First, Professor Teece concluded that, with respect to the RAND requirement of making licenses available to all interested parties, the evidence shows that a patent holder would agree to such a provision, as it ensures that it would likely receive royalties that it otherwise would not receive if it selectively decided to whom it would license. F. 1437. The second provision of the RAND assurance, that the licensor agrees to license on reasonable terms, provides an economic incentive to the patent holder as patentees are assured that royalties are not unreasonable, thereby making them more likely to adopt the technology. F. 1438. The third requirement of the RAND assurance, that the license be demonstrably free of any unfair discrimination, is also attractive to the patent holder because it makes it more likely that licensees will adopt the patented technology. F. 1440. Thus, economic analysis leads to the

conclusion that if JEDEC had asked Rambus to provide a RAND letter, Rambus would have provided such a commitment. F. 1442.

The economic analysis also shows that it is unlikely that there would have been any *ex ante* negotiations. F. 1452-63. Professor McAfee testified that once Rambus issued a RAND letter, JEDEC members would have an incentive to engage in *ex ante* negotiations, i.e., to negotiate with Rambus prior to the adoption of Rambus's technologies into the SDRAM and DDR standards. F. 1452. He further concluded that if any one firm engaged in *ex ante* negotiations with Rambus, that firm would "report" the royalty rates back to other JEDEC members. F. 1452. This conclusion, however, failed to take into account all relevant factors that go into such a decision, including the fact that any such licensing agreements would be done under confidentiality agreements. F. 1452.

Moreover, Complaint Counsel's expert's conclusion is undermined by the fact that there is no evidence of *ex ante* negotiations for naked licenses for patent applications outside of the DRAM industry. F. 1453. The rationale for the absence of negotiations before patents issue is that patent application "rights" have not matured into issued patents and the parties cannot know for what they are bargaining. F. 1454. There is great uncertainty in negotiating such rights because patent applications, during the course of prosecution, often undergo changes – claims get amended, get withdrawn or abandoned – and it is impossible to know what claims will ultimately issue. F. 1454. Because of this uncertainty, negotiations before patents issue are extraordinary complex and costly, and in the real world, firms do not engage in this type of negotiations with any frequency. F. 1455.

The economic evidence thus shows that JEDEC would have adopted Rambus's technologies with a RAND assurance. The record has also demonstrated that the alternatives to Rambus's technologies were inferior in cost performance terms, despite Rambus's royalties. F. 1464. Moreover, JEDEC has repeatedly

demonstrated a willingness to adopt patented technologies, and it would likely do the so again with Rambus's technologies. F. 1466-82. For example, during the period when Rambus attended JEDEC, Desi Rhoden could not recall any incident of a JEDEC committee seeking an alternative technology after a JEDEC member disclosed a relevant patent or application and the member announced it would license on RAND terms. F. 1468. Similarly, Gordon Kelley, a long time chair of JC 42.3 testified that, while he could not recall any instances in which JEDEC pursued alternatives to what the committee thought was a best alternative after receiving a RAND commitment, he did recall some instances in which JEDEC dropped all consideration of alternatives after receiving a RAND assurance. F. 1467.

c. JEDEC's "Revealed Preference" For Rambus's Technologies

Finally, the theory of "revealed preference" shows that JEDEC preferred Rambus's technologies. F. 1465. The theory of revealed preference holds that one draws inferences about people's preferences by observing their choices. F. 1486-87. According to this theory, the choices of JEDEC and DRAM manufacturers to use the Rambus technologies when there were opportunities to use other technologies shows that the Rambus technologies were superior to any alternatives in cost performance terms. F. 1488.

In the real world, JEDEC revealed its preferences by selecting Rambus technologies over all others. For SDRAM, JEDEC selected two Rambus technologies – programmable CAS latency and programmable burst length – over all available alternatives. F. 1489. For DDR, JEDEC selected four Rambus technologies – programmable CAS latency, programmable burst length, dual-edge clocking, and on-chip PLL/DLL – over all available alternatives. F. 1491.

For both the SDRAM and DDR standards, JEDEC considered and rejected several alternatives that Complaint Counsel now assert JEDEC could have adopted in lieu of the Rambus technologies. F. 1489-91. Even with respect to the DDR2 standard development by JEDEC in 2000 and 2001, such work was done with full knowledge of Rambus's patents and demands for royalties. F. 1494-97. Meeting minutes of the Future DRAM Task Group show that JEDEC considered entirely different architectures for the next generation DRAM, but ultimately adopted Rambus technologies. F. 1493, 1502-04, 1584. Thus, according to the theory of revealed preference, the choices of JEDEC and DRAM manufacturers to use the Rambus technologies where there were opportunities to use other technologies, demonstrates that the technologies were superior to any alternatives in cost/performance terms. F. 1486-1518. As stated by Gordon Kelly, JEDEC considered the available technologies and selected what was considered the best. F. 1489.

Thus, neither the technical nor the economic evidence supports Complaint Counsel's argument that there were viable alternatives to the four technologies of Rambus. The evidence further shows that even if Respondent had made additional disclosures, rational DRAM manufacturers and a rational JEDEC would have selected Rambus's technologies because the proposed alternatives were inferior. F. 1464. The evidence also shows that JEDEC might not have sought a RAND assurance from Rambus, but if it had, Rambus would have given it and it is unlikely that there would have been any *ex ante* negotiations. F. 1435-63. Having so concluded, Respondent's conduct before JEDEC with respect to nondisclosure of its patents and patent applications did not cause JEDEC to adopt these technologies into its SDRAM and DDR standards.

4. Complaint Counsel Have Not Demonstrated That Rambus's Conduct Resulted in Higher Prices to Consumers

In *Indian Head*, defendant was found to have violated the integrity of the standard setting organization's procedures for the sole purpose of achieving an *anticompetitive result* – the exclusion of PVC conduit from the marketplace. 817 F.2d at 947. The jury in that case had found that as a proximate result of defendant's restraint of trade, plaintiff lost $3.8 million in profits. *Id.* at 939. Thus, anticompetitive effects were proven. *See also Allied Tube*, 486 U.S. at 509-10 (no *Noerr* immunity from any antitrust liability flowing from the *effect* the standard has of its own force in the marketplace). Here, the evidence shows that competition has not been adversely affected by Rambus's alleged failure to disclose. It is worth noting on this issue that Complaint Counsel's expert, Professor McAfee, admitted that the alleged conduct of Rambus has had no impact on DRAM prices, no effect on consumers, and no effect on the final PC market as of the time of trial (over three and one-half years after Rambus began asserting its patents). F. 1053. Complaint Counsel have not demonstrated any anticompetitive result because Complaint Counsel have not shown consumer harm or that Respondent's royalty rates were anything but reasonable and nondiscriminatory.

a. Rambus's Royalty Rates Are Reasonable

The next question before the Court is, if Rambus had made additional disclosures, would JEDEC members pay the same royalties as they currently do. John Kelly, EIA's President and General Counsel, testified that EIA does not get involved in the determination of whether rates are reasonable and nondiscriminatory. F. 1542. Rather, such questions are left to negotiation by the parties or market forces or are resolved by the courts. F. 603, 1542. Robert Goodwin of Kentron testified that he understood a reasonable rate to be what the market will agree to pay. F. 1544. Similarly, Desi Rhoden testified that what were "fair

and reasonable" licensing terms were left to the courts. F. 1545. A review of the evidence demonstrates that Rambus's royalties are comparable to other licensing rates in the industry and thus are reasonable under the JEDEC rules.

Rambus's royalty rate for its SDRAM licenses is 0.75%. F. 1546. Its royalty rate for DDR licenses in most cases is 3.5%. F. 1546. By way of comparison, the IBM Worldwide Licensing policy sets forth royalty rates from one to five percent of selling price, depending on the category of patent. F. 1548. There is no evidence that the rates contained in IBM's Licensing Policy are unreasonable. F. 1549.

Professor Teece's testimony on this issue is, again, highly persuasive. Professor Teece is a preeminent authority in licensing and cross-licensing in the semiconductor industry. Based on a review of rates charged by IBM, AMD, Kentron, and others, Professor Teece concluded that Rambus's royalty rates were reasonable. F. 1558. The industry rates he stated, cluster around four to five percent. F. 1558. The Rambus SDRAM royalty rate of 0.75% is at the low end of what comparable technologies command. F. 1558. Rambus's DDR royalty rate is near the low end of the middle of comparable rates. F. 1558. This is consistent with Rambus's 1992 business plan which recognized that its royalty rates were in line with semiconductor "traditional royalty levels of 1-5%." F. 1557.

Professor Teece also noted that the industry rates used in this comparison underestimated actual rates because the semiconductor industry rates tend to reflect balancing payments on cross-licenses rather than rates for a straight license like Rambus's. F. 1559. A company can get economic value from internally developed patented technology because it gives the company a benefit in cross-licensing negotiations. F. 1560.

The evidence shows that Rambus's royalty rates were agreed to in arms-length negotiations with major industry players. F.

1561. Complaint Counsel's expert admitted that he had no expertise in how to determine a reasonable royalty rate and Complaint Counsel failed to introduce any evidence to rebut Respondent's showing that its royalty rates were reasonable. F. 1566.

b. Rambus's Royalty Rates Are Non-discriminatory

Professor Teece testified that discrimination in licensing is a circumstance where different parties are offered different deals. A nondiscriminatory license is one where everyone is offered the the same deal at about the same time. F. 1573. The evidence shows that Rambus offered its SDRAM and DDR licenses to everybody on more or less the same terms. F. 1574. The evidence also shows that higher royalties for litigating parties are not discriminatory in an economic sense because litigation involves costs, including legal costs and the diversion of management and litigation involves a risk that the patent will be found invalid or not infringed. F. 1575. Charging higher royalties to litigating parties is therefore cost justified in the sense that it avoids future litigation costs. F. 1578.

Complaint Counsel's economic expert effectively admitted that litigation imposes costs on Rambus and that it is economically rational to develop a strategy to avoid those costs. F. 1580. It would be consistent with economic theory to charge a higher royalty rate to licensees that require the patent holder to incur costs before taking a license. F. 1580. Complaint Counsel's economic expert recognized that litigation imposes risks on Rambus and that a licensing strategy of charging more to companies that choose to litigate would maximize Rambus's profits by reducing its future costs. F. 1580.

Based on this evidence, Complaint Counsel have failed to show that Rambus's royalty rates were anything other than nondiscriminatory. Thus anticompetitive effects, an element of

Counts I, II, and III, has not been proved. Having so held, the liability analysis concludes with an examination of Complaint Counsel's lock in theory.

G. JEDEC Is Not Locked In

Complaint Counsel assert that another element of their legal theory relates to the economic concept of lock in. CCPHB at 22. "Lock in" is a term used in economics to identify a situation where switching costs prohibit consumers from changing to another product or technology. F. 1646. Complaint Counsel argue that "the theory of liability set forth in the Complaint is predicated in part on the allegation that Rambus's bad-faith, deceptive conduct permitted it to acquire monopoly power because by the time Rambus finally began to reveal, publicly, that it possessed patents covering JEDEC's SDRAM standards, the DRAM industry had become locked-in to the existing JEDEC standards and thus was unable to avoid Rambus's patents by switching to alternative, non-infringing standards." CCPHB at 22.

Complaint Counsel, however, have not presented evidence, contemporaneous or otherwise, that the industry is locked in. F. 1582. To the contrary, the evidence demonstrates that DRAM manufacturers are constantly redesigning DRAM products and changing their manufacturing lines to incorporate new designs and manufacturing techniques. For instance, Micron "taped out" numerous new DRAM designs each year. F. 1596-1603. In fact, Micron taped out new designs for SDRAM and/or DDR each year from 1995 to 2002. F. 1597-1602. Infineon's Richmond plant, which started production in 1998, has produced eight different types of SDRAM and two different types of DDR. F. 1608. In 2002, Infineon produced or planned to produce thirty-four different types of DDR, twenty-seven different types of SDRAM, seven different types of Graphics RAM, twenty different types of Mobile-RAM, and six different types of RLDRAM. F. 1612-14. Plainly, economic forces – such as economies of scale and network effects – do not lock in DRAM manufacturers.

As noted earlier, JEDEC's Future DRAM Task Group considered alternatives to each of Rambus's technologies, but ended up adopting the Rambus technologies with full knowledge of Rambus's issued patents and demand for royalties. For example, as late as March and April 2000, JEDEC considered alternatives for programmable CAS latency in DDR SDRAMs. F. 1500. In response to proposals by Micron entitled "Avoid Programmable Latency in SDR/DDR SDRAMs," Bob Fusco of Hitachi wrote, "for DDR2, we have no legacy to live with, so I like the Micron proposal. For DDR-1 it's not too late for minor, carefully considered changes, so I'm open to either proposal." F. 1505-06. Similarly, Bill Hovis of IBM rejected these proposals but stated that he was "*currently not locked in*." F. 1507, 1656 (emphasis added). As Complaint Counsel's own expert testified, JEDEC members would not be discussing alternatives to Rambus technologies, even as late as 2000, unless they thought that such alternatives could be adopted. F. 1501.

The evidence also demonstrates that the DRAM industry routinely coordinates transitions to new DRAM standards. AMD, starting from scratch in June 1997, so quickly coordinated the design and production of every complementary product – motherboards, chip sets, BIOS, etc. – for its newly designed microprocessors, that complete computer systems were shipping in 1999. F. 1624-34. Since then, the industry has coordinated transitions for the AMD microprocessor from PC100 to PC133 to DDR200 and 266 to DDR 333 to DDR400 in the period from June 1999 to May 2003. F. 1625-34. Similarly, from 1995 to 2002, Compaq coordinated transitions for its computers from EDO to PC66 to PC100 to PC133 to DDR266 to DDR333. F. 1635-42. These transitions required the design, manufacture and coordination of complementary components – new chipsets, new motherboards, etc. F. 1644. Based on the evidence of transitions by such companies, a shift to alternative technologies would thus incur few additional costs or coordination difficulties beyond

those that would be incurred when the industry was in transition to a new standard. F. 1655.

The economic evidence shows that switching costs and coordination issues would not prevent the DRAM industry from going to alternatives, if they existed. Complaint Counsel's economic expert did not produce any evidence quantifying switching costs. F. 1650. It is not possible for an economist to make a sound judgment about whether switching costs are high enough to create lock in without quantifying those costs. F. 1651. Rambus's experts, however, did quantify such costs. F. 1650. They showed that the largest part of a DRAM is the memory array, which comprises ninety percent of the active area. F. 14. The remaining ten percent consists of peripheral circuitry, which, if implemented, would include the four features at issue in this proceeding. F. 14. Thus, the vast majority of DRAM development costs is spent on the memory array portion of the DRAM, and not on the peripheral circuitry. F. 14-15. These calculations show, at least in part, that switching costs for these technologies would be modest compared to DRAM costs of production or the costs of Rambus's royalties. F. 1655. If there were acceptable alternatives, switching costs would not be a barrier to adopting those alternatives. Similarly, the economic evidence shows that coordination issues associated with replacing the four technologies in question with alternatives are not any more costly or difficult than those faced and solved by the DRAM industry in the ordinary course of business and, thus, do not create lock in. F. 1660.

The record in this proceeding thus demonstrates that DRAM manufacturers were not locked in to using Rambus's technologies at any point in time from 1990 to the present. F. 1664. JEDEC membership includes virtually every DRAM and major electronics manufacturer in the world. It therefore had access to the research and development departments of every DRAM manufacturer to design the best memory technology possible. If they wished to avoid paying royalties, they would have been

highly motivated to seek alternatives to Rambus's innovations. This is true for the two Rambus technologies used in SDRAM, the four used in DDR, and the four used in DDR2. The fact that the DRAM industry continues in 2004 to use the four Rambus technologies in DDR2, even after it was well aware of Rambus's patents is persuasive evidence that Rambus's technologies were superior, in cost/performance terms, to any alternatives, despite Rambus's royalty rates. *See* 1665.

IV. SUMMARY OF LIABILITY

For the above stated reasons, Complaint Counsel, the party with the burden of proof, have failed to establish the elements necessary for finding liability on Counts I, II, and III of the Complaint. A review of the three violations alleged in the Complaint shows that although Respondent is in possession of monopoly power in the relevant markets, Complaint Counsel have failed to demonstrate that Respondent engaged in a pattern of exclusionary, anticompetitive conduct which subverted an open standards process, or that Respondent utilized such conduct to capture an unlawful monopoly in the technology-related markets. Analyzing the challenged conduct under established principles of economics and antitrust law and utilizing the preponderance of evidence standard, Complaint Counsel have not proven the elements necessary to support a finding of liability.

PART FOUR: SUMMARY OF CONCLUSIONS OF LAW

Jurisdiction and Burden of Proof

1. Pursuant to Section 5 of the FTC Act, 15 U.S.C. § 45, the Commission has jurisdiction over the subject matter of this proceeding and over Respondent, Rambus Inc.

2. Respondent is organized, existing and doing business under and by virtue of the laws of the state of Delaware, with its office

and principal place of business located at 4440 El Camino Road Real, Los Altos, California 94022.

3. Respondent is a corporation, as "corporation" is defined in Section 4 of the Federal Trade Commission Act, 15 U.S.C. § 44.

4. Respondent's acts and practices, including the acts and practices alleged in the Complaint, are in or affect commerce as "commerce" is defined in Section 4 of the Federal Trade Commission Act, 15 U.S.C. § 44.

5. Pursuant to § 3.43 (a) of the Federal Trade Commission's Rules of Practice, Complaint Counsel bear the burden of proof of establishing each element of the violations alleged in the Complaint by a preponderance of the evidence.

The Relevant Markets and Monopoly Power

6. The relevant geographic market for purposes of determining the possession of monopoly power in this case is the world.

7. The relevant product markets at issue in this proceeding involve technologies that are incorporated in DRAMs for use in current and recent generation personal computers and other electronic memory devices. Each market consists of a type of technology that addresses a specific aspect of memory design and operation. The four relevant product markets are: (1) the latency technology market; (2) the burst length technology market; (3) the data acceleration technology market; and (4) the clock synchronization technology market. In addition, there is a cluster market of synchronous DRAM technologies.

8. Complaint Counsel have demonstrated that Respondent has acquired monopoly power in the relevant markets. However, Complaint Counsel have not demonstrated that Respondent's acquisition or maintenance of monopoly power was unlawful.

No Pattern of Anticompetitive Acts and Practices

9. Complaint Counsel have failed to demonstrate that Respondent's challenged conduct amounted to a pattern of anticompetitive acts and practices.

10. Complaint Counsel's legal theory, i.e., that Respondent's challenged conduct violated Section 5 of the Federal Trade Commission Act, which proscribes "unfair methods of competition," lacks a reasonable basis in law.

11. Complaint Counsel have failed to demonstrate that the duties upon which they base their challenge are clear and unambiguous.

12. The evidence presented at trial does not provide a factual basis for finding a pattern of anticompetitive acts and practices.

13. Complaint Counsel have failed to demonstrate that amendments to broaden patent applications are improper, either under patent law or EIA/JEDEC rules.

No Exclusionary Conduct

14. Respondent has demonstrated that there were legitimate business justifications for the conduct challenged by Complaint Counsel. Maintaining the confidentiality of the proprietary information contained in its patent applications clearly related to a legitimate and normal business purpose and thus precludes a finding of exclusionary conduct in this case.

15. Complaint Counsel have failed to demonstrate that mere participation in a standard setting organization, without more, can form the basis for excluding a member's legitimate right to protect its trade secrets from disclosure.

16. Complaint Counsel have failed to demonstrate that Respondent engaged in exclusionary conduct for reasons extrinsic to the antitrust laws.

No Intent

17. Complaint Counsel have failed to demonstrate that Respondent intended to mislead or deceive JEDEC.

18. Complaint Counsel have failed to demonstrate that Respondent's challenged conduct rises to a level where intent can be inferred.

19. Evidence in the record indicates that Complaint Counsel have failed to demonstrate that the intent element has been met.

No Causation

20. Complaint Counsel have failed to demonstrate a causal link between JEDEC standardization and Respondent's acquisition of monopoly power.

21. Complaint Counsel have failed to demonstrate that Respondent acquired monopoly power by virtue of JEDEC standard setting.

22. The evidence demonstrates that Respondent acquired monopoly power as a result of its superior technology and Intel's choice of Rambus's technology.

23. To the extent that Complaint Counsel's Section 5 cause of action is based upon a breach of duty to disclose under JEDEC's rules, Complaint Counsel have failed to demonstrate that Respondent's omissions or misrepresentations were relied upon by JEDEC or that such reliance was reasonable.

No Anticompetitive Effects

24. Complaint Counsel have failed to demonstrate that there were viable alternatives to Respondent's technologies.

25. Complaint Counsel's economic expert failed to demonstrate that "equal or superior" alternatives were excluded by Respondent's challenged conduct.

26. Under the economic theory of "revealed preference," the evidence demonstrates that even if Respondent had made the additional disclosures alleged to have been required, rational manufacturers and a rational JEDEC would have selected Respondent's technologies because the proposed alternatives were inferior.

27. Complaint Counsel have failed to demonstrate that Respondent's challenged conduct resulted in higher prices to the consumer.

28. The evidence indicates that Respondent's royalty rates are reasonable.

29. The evidence indicates that Respondent's royalty rates are nondiscriminatory.

JEDEC Is Not Locked In To Respondent's Technologies

30. The evidence indicates that DRAM manufacturers were not locked in to using Respondent's technologies at any point from 1990 to the present.

31. JEDECs continued use of Respondent's technologies is due to the fact that Rambus's technologies are superior in cost/performance terms to any alternatives, despite Rambus's royalty rates.

ORDER

Accordingly, Complaint Counsel having failed to sustain its burden of establishing liability for the violations alleged, the Complaint is **DISMISSED.**

OPINION OF THE COMMISSION

By HARBOUR, Commissioner, for a unanimous Commission.

I. INTRODUCTION[1]

Rambus Inc. is a developer and licensor of computer memory technologies. For more than four years during the 1990s, Rambus participated as a member of the Joint Electron Device Engineering Council (JEDEC), an industrywide standard-setting organization (SSO) that operated on a cooperative basis. Through a course of deceptive conduct, Rambus exploited its participation in JEDEC to obtain patents that would cover technologies incorporated into now-ubiquitous JEDEC memory standards, without revealing its patent position to other JEDEC members. As a result, Rambus was able to distort the standard-setting process and engage in anticompetitive "hold up" of the computer memory industry. Conduct of this sort has grave implications for competition. The Federal Trade Commission (FTC or Commission) finds that Rambus's acts of deception constituted exclusionary conduct

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[1] This opinion uses the following abbreviations:

CA - Complaint Counsel's Appendix
CE - Order Granting Complaint Counsel's Motion for Collateral Estoppel
CCAB - Complaint Counsel's Appeal Brief
CCRB - Complaint Counsel's Reply Brief
CX - Complaint Counsel's Exhibit
DX - Demonstrative Exhibit
ID - Initial Decision of the Administrative Law Judge (ALJ)
IDF - Numbered Findings of Fact in the ALJ's Initial Opinion
JX - Joint Exhibits
RA - Respondent's Appendix
RB - Respondent's Brief on Appeal and Cross-Appeal
RFF - Respondent's Proposed Findings of Fact
RRB - Respondent's Rebuttal Brief
RX - Respondent's Exhibit
Tr. - Transcript of Trial before the ALJ.

under Section 2 of the Sherman Act, and that Rambus unlawfully monopolized the markets for four technologies incorporated into the JEDEC standards in violation of Section 5 of the FTC Act.

Standard setting occurs in many industries and can be highly beneficial to consumers. Standards can facilitate interoperability among products supplied by different firms, which typically increases the chances of market acceptance, makes the products more valuable to consumers, and stimulates output. But standard setting also poses some risks of harm to competition. By its very nature, standard setting displaces the competitive process through which the purchasing decisions of customers determine which interoperable combinations of technologies and products will survive.

Typically, the procompetitive benefits of standard setting outweigh the loss of market competition. For this reason, antitrust enforcement has shown a high degree of acceptance of, and tolerance for, standard-setting activities. But when a firm engages in exclusionary conduct that subverts the standard-setting process and leads to the acquisition of monopoly power, the procompetitive benefits of standard setting cannot be fully realized.

At the beginning of a standard-setting process, if there are a number of competing technologies, and if any one of them could win the standards battle, then no single technology will command more than a competitive price. Once the standard has been set, however, the dynamic changes. Soon after a standard is adopted, industry participants likely will start designing, testing, and producing goods that conform to the standard. Early in the process of implementing a standard, industry members still might find it relatively easy to abandon one technology in favor of another. But as time passes, and the industry commits greater levels of resources to developing products that comply with the standard, the costs of switching to alternative technologies begin to rise. Industry members may find themselves "locked in" to the

standardized technology once switching costs become prohibitive. Once lock-in occurs, the owner of the standardized technology may be able to "hold up" the industry and charge supracompetitive rates.

Many SSOs have taken steps to mitigate the risk of hold-up by avoiding unknowing lock-in to a technology that may command supracompetitive rates. Many SSOs, for example, require their members to reveal any patents and/or patent applications that relate to the standard. These types of disclosures enable SSO members to evaluate potential standards with more complete information about the likely consequences, before the standard is finalized. Some SSOs also require members to commit to license their patented technologies on reasonable and nondiscriminatory (RAND) terms, which may further inform SSO members' analysis of the costs and benefits of standardizing patented technologies.

JEDEC operated on a cooperative basis and required that its members participate in good faith. According to JEDEC policy and practice, members were expected to reveal the existence of patents and patent applications that later might be enforced against those practicing the JEDEC standards. In addition, JEDEC members were obligated to offer assurances to license patented technologies on RAND terms, before members voted to adopt a standard that would incorporate those technologies. The intent of JEDEC policy and practice was to prevent anticompetitive hold-up.

Rambus, however, chose to disregard JEDEC's policy and practice, as well as the duty to act in good faith. Instead, Rambus deceived the other JEDEC members. Rambus capitalized on JEDEC's policy and practice – and also on the expectations of the JEDEC members – in several ways. Rambus refused to disclose the existence of its patents and applications, which deprived JEDEC members of critical information as they worked to evaluate potential standards. Rambus took additional actions that misled members to believe that Rambus was not seeking patents

that would cover implementations of the standards under consideration by JEDEC. Rambus also went a step further: through its participation in JEDEC, Rambus gained information about the pending standard, and then amended its patent applications to ensure that subsequently-issued patents would cover the ultimate standard. Through its successful strategy, Rambus was able to conceal its patents and patent applications until after the standards were adopted and the market was locked in. Only then did Rambus reveal its patents – through patent infringement lawsuits against JEDEC members who practiced the standard.[2]

The Commission finds that Rambus violated Section 5 of the FTC Act by engaging in exclusionary conduct that contributed significantly to the acquisition of monopoly power in four relevant and related markets. We further find a sufficient causal link between Rambus's exclusionary conduct and JEDEC's adoption of the SDRAM and DDR-SDRAM standards (but not the subsequent DDR2-SDRAM standard). Questions remain, however, regarding how the Commission can best determine the appropriate remedy. Accordingly, the Commission orders additional briefing for further consideration of remedial issues.

II. BACKGROUND

A. Technology Background

The dispute before us involves four relevant product markets: (1) latency technology; (2) burst length technology; (3) data

[2] Complaint Counsel also allege that Rambus engaged in spoliation of evidence. Rambus instituted a document retention policy that entailed the systematic destruction of a large volume of documents. This destruction policy included documents related to Rambus's participation in JEDEC and Rambus's patent prosecution files. As discussed in greater detail *infra*, Section V, however, we need not resolve the spoliation question because our findings are firmly grounded on the surviving evidence.

acceleration technology; and (4) clock synchronization technology. These markets include technologies that, beginning in 1993, have been incorporated into the JEDEC standards for computer memory, and over which Rambus now claims patent rights.[3]

1. The Function of Computer Memory

Main memory – often referred to as random access memory, or RAM – consists of integrated circuits that hold temporary instructions and data for the central processing unit (CPU), the central "brain" of a computer system[4]. The CPU performs each command given by a computer user by extracting instructions from the computer's memory, then decoding and executing them. Most computers use a type of RAM known as dynamic random access memory (DRAM),[5] which stores and processes information while the computer is on.[6]

DRAM is only one piece in the computer hardware infrastructure. A typical personal computer is built around a motherboard – the main circuit board upon which many of the important components of a computer system are fastened. The

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[3] Rambus has not contested the definition of the four relevant product markets delineated by Complaint Counsel. *See infra* note 394. Nor does Rambus contest Complaint Counsel's allegation, or the ALJ's finding (which we adopt), that the relevant geographic market is worldwide. Complaint ¶ 117; IDF 1016-17; ID 250.

[4] Rhoden, Tr. 271-72; RA 3. Most types of RAM are volatile, which means they lose all data when the power is turned off or the system shuts down. CA A-3; RA 3.

[5] DRAM is "dynamic" because it must be refreshed every fraction of a second to prevent memory loss. Rhoden, Tr. 266-67.

[6] Rhoden, Tr. 267-68. DRAM also is incorporated into other electronic devices such as servers, printers, and cameras. IDF 3; Rhoden, Tr. 298; RA 3.

motherboard includes, for example, the CPU, chipset, and graphics and sound cards. A computer system also includes a system clock, a power supply, mass storage devices (such as hard drives or CD ROM drives), assorted controllers that enable the computer to connect to external peripheral devices (such as monitors, printers, and scanners), and a main memory system (containing DRAM). The main memory circuits typically attach to the memory module (a small printed circuit board that plugs into the motherboard)[7]. Communications between the main memory circuits and the CPU are managed by a memory controller, which generally is part of the chipset[8]. DRAM must be compatible and interoperable with other components in the same computer system.[9]

2. Evolution of RDRAM and SDRAM Memory Technologies: Breaking Through the Memory Bottleneck

In the early 1980s, an imbalance emerged in the speed at which CPU technology was developing relative to memory technology[10]. CPU speeds have doubled every eighteen months for the past two decades,[11] while memory speeds have increased more slowly. This "memory bottleneck problem"[12] became a

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[7] Rhoden, Tr. 269, 272-73; RA 4.

[8] Rhoden, Tr. 275-76; CA A-1; RA 2.

[9] *See, e.g.*, IDF 6.

[10] IDF 27-40.

[11] Farmwald, Tr. 8068 (describing "Moore's law," based on observations by Intel co-founder Gordon Moore regarding the rate of increase in CPU speeds).

widely recognized concern in the computer hardware industry during the early 1990s[13]. The industry considered several different solutions.[14]

One of those solutions – Rambus DRAM, or RDRAM – was developed by Rambus[15]. Rambus was founded in March 1990 by two professors who wanted to commercialize their concept for a new DRAM design that would break the "memory bottleneck."[16] Rambus develops, secures patents on, and licenses technologies to companies that manufacture semiconductor memory devices.

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[12] One of Rambus's founders, Paul Michael Farmwald, testified that the "memory bottleneck" problem was a potential bottleneck in which memory chip performance could limit computer performance. Farmwald, Tr. 8068-69, 8071-73.

[13] IDF 36-40.

[14] *See, e.g.*, CX 711 at 1; Sussman, Tr. 1359-60, 1364; G. Kelley, Tr. 2584-85. In the last decade most DRAMs have been synchronized with the system clock, in order to maximize the number of instructions a CPU can process in a given time. This design is called "synchronous DRAM," or SDRAM (as distinguished from earlier, asynchronous DRAMs). Jacob, 5394-95; CA A-4; RA 5.

[15] RDRAM reflected innovations with respect to bus width, the interface between the bus and computer chips, and the DRAM. IDF 86-90; CA A-4; RX 81 at 3,7; Horowitz, Tr. 8618-20; Rhoden, Tr. 400-401. Buses essentially are a computer's highway system. A memory bus comprises the lines that connect each memory device to the memory controller. Computer buses, like highways, can vary by width, which means they can have a differing number of lines linking the computer's components (just as highways may have more or fewer lanes to carry traffic). The speed at which a computer operates is affected by its buses. Rhoden, Tr. 275-76; CA A-1.

[16] IDF 27-48, 58; CX 533 at 8; CX 545 at 7; Farmwald, Tr. 8089-93; Horowitz, Tr. 8486.

Rambus is not a manufacturing company; rather, Rambus earns its revenue through the licensing of its patents.[17]

A month after its founding, on April 18, 1990, Rambus filed Patent Application No. 07/510,898 (the '898 application) with the U.S. Patent Trademark Office (PTO)[18]. This application described many of the technologies developed and integrated into the initial RDRAM design. The '898 application also is the original source of the patents that Rambus has asserted with regard to the four technologies at issue in this case**.** The PTO issued a restriction requirement in late 1990, requiring Rambus to decide which of the multiple claimed inventions it wished to pursue in the '898 application. On March 5, 1992, Rambus responded to the PTO's demand by filing ten divisional applications.[19]

Beginning in 1990, Rambus tried to license its RDRAM technology to manufacturers of DRAM chips and DRAM-compatible microprocessors[20]. Rambus attempted to position RDRAM as the *de facto* standard[21]. Rambus made numerous presentations on RDRAM to the major DRAM manufacturers in

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[17] Parties' First Set of Stipulations, Item 2 (April 23, 2003); *see also* CX 2106 (Farmwald FTC Dep.) at 220 (*in camera*) ("[r]oyalties are the lifeblood of Rambus").

[18] CX 1451.

[19] A restriction requirement forces a patent applicant to separate each distinct invention or group of inventions into separate applications known as "divisionals." Nusbaum, Tr. 1509-11.

[20] *See* CX 533 at 9-10. Major DRAM manufacturers included Samsung Electronics Co., Micron Technology, Inc., Hyundai Electronics Industries (subsequently, Hynix Semiconductor Inc.), LG Semicon Ltd., NEC Corporation, Siemens AG (subsequently, Infineon Technologies AG), Toshiba, Mitsubishi Electric Corporation, and Hitachi, Ltd. *See* CX 2747 at 7.

[21] *Id.* at 3.

an effort to persuade them to adopt the technology[22]. Rambus also tried to develop relationships with major systems companies, and pursued commitments from these companies to introduce systems using RDRAM technology[23]. RDRAM failed to achieve significant market success, however, at least in part because manufacturers were reluctant to pay royalties and licensing fees to Rambus.[24]

These manufacturers rejected RDRAM and instead turned to standards promulgated by JEDEC. JEDEC was a semiconductor engineering standardization body within the Electronic Industries Association (EIA). It comprised manufacturers and purchasers of DRAM, as well as producers of complementary products and computer systems[25]. JEDEC's JC 42.3 committee was responsible

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[22] *See, e.g.*, Sussman, Tr. 1429-31; CX 535 at 1, 4-5; CX 543a at 11; CX 2107 at 63 (Oh FTC Dep.) (*in camera*).

[23] *See, e.g.*, Kellogg, Tr. 5049-54; Bechtelsheim, Tr. 5816-19; CX 535 at 2, 5-6.

[24] *See, e.g.*, Rapp, Tr. 10248-49 (RDRAM sales represented less than 2% of the market for at least six years following the adoption of SDRAM) (providing market-share statistics); JX 36 at 7 ("Some Committee members did not feel that the Rambus patent license fee fit the JEDEC requirement of being reasonable."); CX 961 at 1 (September 1997 Intel e-mail to Rambus Chief Executive Officer (CEO) Geoff Tate, stating that, upon analyzing the royalty obligations attached to RDRAM, the industry would develop alternatives); RX 1482 at 12 (post-1996 Rambus Strategic Review stating, "Memory manufacturers need to focus on cost reduction to restore profitability" and describing RDRAM as "a guaranteed bad bet for margin enhancement").

[25] *See* J. Kelly, Tr. 1774-75; Rhoden, Tr. 293-94; Landgraf, Tr. 1685; JX 18 at 1-3. Between 1991 and 1996, JEDEC was an organization within the EIA. IDF 222; J. Kelly, Tr. 2075. EIA engages in a variety of different activities in support of the electronics industry in the United States, including government relations, marketing research, trade shows, and standard setting. J. Kelly, Tr. 1750-51, 1764. In 1998, EIA was renamed the Electronic Industries Alliance, and JEDEC became an EIA division. CX 302 at 11. By the first quarter of 2000, JEDEC became separately incorporated, but remained contractually affiliated with EIA. J. Kelly, Tr. 1752; CX 302 at 11.

for RAM issues, and, in particular, for the development of DRAM standards.[26]

At issue here are three generations of DRAM standards developed and adopted by JEDEC: synchronous DRAM (SDRAM),[27] DDR SDRAM,[28] and DDR2 SDRAM[29]. In the course of designing these standards and determining which technologies would be incorporated, the JEDEC members evaluated numerous technologies relating to various aspects of

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[26] Rhoden, Tr. 284-85, 288; Williams, Tr. 763; J. Kelly, Tr. 1769. JEDEC was divided into several committees. Each committee focused on a particular aspect of the semiconductor and solid state electronics industries, and was subdivided into several subcommittees.

[27] JEDEC designed the SDRAM standard during the early 1990s and first published it in 1993. IDF 297-315, 355-56. By 1998, JEDEC-compliant SDRAM was the most widely used type of memory device. IDF 370; CA A-5. The SDRAM standard incorporated technologies from the latency and burst length markets. IDF 355; 1013; RA 5. Rambus has asserted that its patents cover the implementations of these two technologies in the SDRAM standard. IDF 1022-29.

[28] DDR SDRAM was a second-generation standard promulgated by JEDEC. RA 2. DDR SDRAM included some of the features of SDRAM, and also incorporated new technologies that increased the speed and efficiency of the memory system. IDF 430; CA A-1. JEDEC first published DDR SDRAM in 1999. IDF 427-29; RA 2. JEDEC-compliant DDR SDRAM was forecast to overtake SDRAM as the predominant memory device by 2002-03. *See* McAfee, Tr. 7227 (presenting DX 141), 7430-31 (presenting DX 219). DDR SDRAM incorporated technologies from the latency, burst length, data acceleration, and clock synchronization markets. Rambus has asserted that its patents cover the implementations of these four technologies in the DDR SDRAM standard. IDF 1022-29.

[29] DDR2 SDRAM is the third-generation standard that JEDEC developed using SDRAM technology. RA 2; CA A-1. By the time of the 2003 trial, JEDEC had published to its members preliminary specifications for this standard that retained the latency, burst length, data acceleration, and clock synchronization technologies that Rambus has claimed infringe its patents. RA 2.

main memory, including the technologies that comprise the four relevant product markets in this case. Rambus eventually claimed that its patents cover the specific versions of these four technologies that ultimately were adopted by JEDEC for the SDRAM, DDR SDRAM, and DDR2 SDRAM standards.

3. The Four Relevant Technology Markets

a. Latency Technology

Latency is a measure of the amount of time between a request and a response[30]. Memory latency is the length of time between the memory's receipt of a read request and its release of data corresponding with the request[31]. Latency technology comprises those technologies used to control the length of this time period.[32]

In the early 1990s, several types of latency technology were available, including programmable latency, fixed latency, blowing a fuse on a DRAM, and dedicated pins. These alternative solutions are discussed in greater detail below[33]. JEDEC first incorporated programmable column address strobe (CAS) latency into its SDRAM standard and retained the technology in its DDR SDRAM and DDR2 SDRAM standards[34]. Programmable CAS latency controls data output timing by determining the number of clock cycles that should be allowed to elapse after a defined point[35]. Programmable CAS latency provides users of DRAMs

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30 IDF 114.

31 Horowitz, Tr. 8529-30.

32 McAfee, Tr. 7348.

33 *See infra* Section IV.C.3.b.

34 IDF 355, 433; RA 2, 5.

35 CA A-3.

with flexibility, *i.e.*, a single part can be programmed so as to provide the optimal latency in a variety of systems.[36]

Rambus claims that its patents cover JEDEC's implementation of programmable CAS latency technology.

b. Burst Length Technology

Burst length technology controls the amount of data transferred between the CPU and memory in each transmission. JEDEC's SDRAM, DDR SDRAM, and DDR2 SDRAM standards adopted programmable burst length technology, which provides a means for varying the number of cycles of data that are transmitted to the memory controller in response to an individual command[37]. Programmable burst length technology is similar to programmable CAS latency technology in that it allows DRAM customers to use one part for many different types of machines that require different burst lengths.[38]

In the early 1990s several alternatives to programmable burst length were available, as discussed in greater detail below[39]. One alternative was the use of fixed burst length parts[40]. Another alternative was to use "burst terminate commands," which establish a long burst length as the default and use the memory

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[36] Soderman, Tr. 9346-47, 9433-34; Kellogg, Tr. 5140.

[37] CA A-3.

[38] *See, e.g.*, G. Kelley, Tr. 2550-51 ("The programmable [burst length] feature allowing you to make that selection when the PC or computer powered up was a nice feature because it allowed you to use devices that were common from multiple suppliers, put them into many different types of machines. . . . One part number fits many applications.").

[39] *See infra* Section IV.C.3.b.

[40] Jacob, Tr. 5398-99.

controller to terminate the burst if a shorter burst length is desired.[41]

Rambus claims that its patents cover JEDEC's implementation of programmable burst length technology.

c. Data Acceleration Technology

Data acceleration technology determines the speed at which data are transmitted between the CPU and memory. JEDEC's DDR SDRAM and DDR2 SDRAM standards adopted one particular type of data acceleration technology, known as dual-edge clocking, which captures data off both the rising and falling edges (the "tick" and the "tock") of the clock[42]. This technology enables twice the amount of data to be sent in each clock cycle compared to single-edge clocking, by which data are sent only on one edge of the clock.[43]

When JEDEC was considering whether to adopt dual-edge clocking technology as part of its DDR SDRAM standard, several alternatives were available. As discussed in greater detail below,[44] alternative technologies included interleaving ranks on the module (using different clock signals for separate groups of DRAM chips), double clock frequency (operating a single-edge clock at twice the frequency of a dual-edge clock[45]), and toggle mode

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41 Jacob, Tr. 5409-10.

42 RA 3.

43 CA A-2.

44 *See infra* Section IV.C.3.b.

45 Jacob, Tr. 5433-34.

(which, as formulated by IBM, combined synchronous and asynchronous features[46]).

Rambus claims that its patents cover JEDEC's implementation of dual-edge clocking technology.

d. Clock Synchronization Technology

Clock synchronization technologies coordinate the internal clock on each DRAM chip with the timing of the computer's system clock. Phase lock loop (PLL) and delay lock loop (DLL) technologies use circuits to align more closely the timing of the internal clock on each DRAM with the system clock[47]. Rambus developed a technology that places a PLL/DLL[48] on the SDRAM chip itself[49]. On-chip PLL/DLL clock synchronization technology was incorporated into JEDEC's DDR SDRAM and DDR2 SDRAM standards.

One alternative approach to on-chip PLL/DLL involved placing a PLL/DLL circuit on the memory controller that synchronizes all DRAMs[50]. Another approach involved placing

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[46] *See* Jacob, Tr. 5608, 5416-17; Soderman, Tr. 9398; G. Kelley, Tr. 2514.

[47] Jacob, Tr. 5442-43; Kellogg, Tr. 5150-55; RA 4; CA A-3. PLLs use voltage oscillators to synchronize the internal clock with the system clock. *See* Jacob, Tr. 5443, 5616-17; Soderman, Tr. 9401. In contrast, DLLs introduce a variable amount of delay into the internal clock to synchronize that clock with the system clock. *See* Jacob, Tr. 5443, 5616-17; Soderman, Tr. 9401.

[48] Horowitz, Tr. 8607 (Rambus co-founder testified that, under his usage of the terms, "a PLL is the generic term for any circuitry that adjusts phase, so a DLL is a kind of PLL").

[49] Farmwald, Tr. 8117-18; Horowitz, Tr. 8503-05; 8521-22, 8527-28.

[50] Jacob, Tr. 5445.

one or more PLL/DLL circuits on the memory module[51]. Still other alternatives involved the use of vernier circuits, which introduce static delays on a signal to reduce timing uncertainties in a memory system, or reliance on a data strobe to signal the memory controller the timing of data capture[52]. These alternatives, which were considered by JEDEC prior to its adoption of on-chip PLL/DLL, are discussed in greater detail below.[53]

Rambus claims that its patents cover JEDEC's implementation of on-chip PLL/DLL technology.

B. Procedural History

1. History of FTC Matter

The Complaint in this matter was issued on June 18, 2002. The Complaint charged that Rambus: (1) monopolized certain memory technology markets through a pattern of anticompetitive and exclusionary conduct; (2) attempted to monopolize these markets; and (3) engaged in unfair methods of competition.[54]

The Complaint's allegations focused on Rambus's participation in JEDEC. It alleged that Rambus deceived JEDEC's members by, for example, concealing the fact that it

> was actively working to develop, and did in fact possess, a patent and several pending patent applications that involved specific technologies

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[51] Jacob, Tr. 5448-49.

[52] Jacob, Tr. 5450, 5456-57.

[53] *See infra* Section IV.C.3.b.

[54] *See* Complaint ¶¶ 122-24.

> proposed for and ultimately adopted in the relevant standards. By concealing this information – in violation of JEDEC's own operating rules and procedures – and through other bad-faith, deceptive conduct,

Rambus allegedly conveyed the "materially false and misleading impression that it possessed no relevant intellectual property rights"[55] and that it had no plans to enforce any intellectual property rights that might later become relevant, leaving a materially misleading impression of its intellectual property ownership and plans[56]. The Complaint further alleged that Rambus's conduct resulted in anticompetitive effects including: increased royalties; increased prices for memory products compliant with JEDEC standards; decreased incentives to produce memory using JEDEC-compliant memory technology; and decreased incentives to participate in, and rely on, standard-setting organizations and activities[57]. According to the Complaint, Rambus gave no notice that it intended to claim patent rights over technologies used in JEDEC's DRAM standards, and, by failing to do so, likely affected the content of those standards and/or the terms on which Rambus later licensed its patent rights.[58]

a. Pre-Trial Orders

The case was first assigned to Administrative Law Judge (ALJ) James P. Timony and, upon his retirement, was reassigned

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[55] *See* Complaint ¶ 2; *see also id.* ¶¶ 54 (alleging deception and bad-faith conduct), 71 (alleging that Rambus conveyed "a materially false and misleading impression").

[56] *See* Complaint ¶¶ 70-78.

[57] *See* Complaint ¶¶ 119-120.

[58] *See* Complaint ¶¶ 62, 65, 69, 70-78, 86.

to Chief ALJ Stephen J. McGuire[59]. Before retiring, ALJ Timony issued two orders on February 26, 2003: first, an Order Granting Complaint Counsel's Motion for Collateral Estoppel; and second, an Order on Complaint Counsel's Motions for Default Judgment and for Oral Argument. Both orders influenced the trial and ALJ McGuire's Initial Decision.

On February 12, 2003, Complaint Counsel filed a motion seeking recognition of the collateral estoppel effect of prior factual findings that Rambus had destroyed material evidence. ALJ Timony granted the motion, thus barring Rambus from re-litigating certain findings of fact made by the district court in prior private litigation, *Rambus Inc. v. Infineon Technologies AG*[60]. Those findings included:

1. When Rambus instituted its document retention policy in 1998, it did so, in part, for the purpose of getting rid of documents that might be harmful in litigation.

2. Rambus, at the time it implemented its document retention policy, … [c]learly … contemplated that it might be bringing patent infringement suits during this timeframe if its efforts to persuade semi-conductor manufacturers to license its JEDEC-related patents were not successful.

3. Rambus's document destruction was done in anticipation of litigation.[61]

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[59] All references within this opinion to "the ALJ," unless otherwise specifically identified, will refer to ALJ McGuire.

[60] 155 F. Supp. 2d 668 (E.D. Va. 2001), *aff'd in part and rev'd in part*, 318 F.3d 1081 (Fed. Cir. 2001). The district court's findings, upon which ALJ Timony relied, were not raised on appeal to the Federal Circuit.

[61] CE at 5 (internal quotations omitted).

Complaint Counsel also moved for default judgment as a remedy to counter Rambus's intentional destruction of documents. ALJ Timony denied the motion, but set forth seven rebuttable adverse presumptions against Rambus. The presumptions included:

1. Rambus knew or should have known from its pre-1996 participation in JEDEC that developing JEDEC standards would require the use of patents held or applied for by Rambus;

2. Rambus never disclosed to other JEDEC participants the existence of these patents; [and]

3. Rambus knew that its failure to disclose the existence of these patents to other JEDEC participants could serve to equitably estop Rambus from enforcing its patents as to other JEDEC participants.[62]

Four additional presumptions addressed the foreseeability of litigation and Rambus's document retention program.[63]

b. ALJ McGuire's Initial Decision

On February 17, 2004, ALJ McGuire issued his Initial Decision and Proposed Order dismissing the Complaint in its entirety. Specifically, although he noted that Section 5 of the FTC

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[62] Order on Complaint Counsel's Motions for Default Judgment and for Oral Argument at 9 (Feb. 26, 2003).

[63] *Id*. (announcing presumptions that Rambus's document retention program failed to provide adequate guidance and direction to its employees and that Rambus knew or should have known that litigation over the enforcement of its patents was reasonably foreseeable).

Act authorizes the FTC to define and proscribe unfair methods of competition, the ALJ determined that Complaint Counsel had established no basis for finding a violation of Section 5[64]. He concluded that Complaint Counsel's arguments lacked a reasonable basis in law,[65] and ruled that Complaint Counsel's factual showing was insufficient to establish a violation even if the legal theories had been deemed adequate.[66]

The ALJ found that the adverse presumptions entered by ALJ Timony were not material to the disposition of the case. The ALJ found no indication that Rambus had destroyed any relevant and material documents. He found that the first and second presumptions were moot because Rambus was not required to disclose its patents or patent applications[67]. He also rejected the second presumption on the ground that Rambus's conduct raised sufficient red flags to put members of JEDEC on notice that Rambus had applications pending[68]. The ALJ then found the remaining five adverse presumptions to be irrelevant to the material issues of the case.

The ALJ found that there was no causal link between JEDEC's adoption of Rambus's technology into its standards and Rambus's acquisition of monopoly power. Rather, the ALJ found that Rambus acquired its monopoly power as a result of superior technology and market preferences[69]. Moreover, the ALJ found that JEDEC, and many members of the DRAM industry, were

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64 ID at 254.

65 ID at 254-60.

66 ID at 259-61.

67 ID at 244.

68 ID at 244-45.

69 ID at 300-04.

aware of Rambus's patent portfolio. Thus, according to the ALJ, no member of JEDEC reasonably could have relied on any misrepresentation or omission by Rambus in its dealings with JEDEC[70]. The ALJ found no basis for ascribing to Rambus an intent to deceive.[71]

The ALJ concluded that the challenged conduct did not result in any anticompetitive effect because Complaint Counsel failed to prove there were viable alternatives to Rambus's technologies[72]. Furthermore, according to the ALJ, Complaint Counsel did not demonstrate that Rambus's conduct had resulted in higher prices to consumers[73]. In contrast, the ALJ found that Rambus had put forth legitimate business justifications for its conduct. He agreed with Rambus that its secrecy regarding its patent applications constituted normal and legitimate protection of trade secrets. The ALJ concluded that this business justification precluded a finding of exclusionary conduct.[74]

Finally, the ALJ found that the DRAM industry never became locked into using Rambus's technologies as incorporated into the JEDEC standards, because "economic evidence shows that switching costs and coordination issues would not prevent the DRAM industry from going to alternatives."[75]

c. Questions Raised on Appeal/Cross Appeal

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[70] ID at 304-09.

[71] ID at 295-300, 331-32.

[72] ID at 312-16.

[73] ID at 323-26.

[74] ID at 287-89.

[75] ID at 328, 326-29.

Complaint Counsel filed a notice of appeal on March 1, 2004. They challenge virtually all of the ALJ's rulings and ask that the Initial Decision be set aside in its entirety. They contend that Rambus acquired monopoly power by pursuing a secret and deliberate pattern of conduct to obtain patents covering JEDEC standards. According to Complaint Counsel, Rambus's course of conduct undermined the fundamental purpose of JEDEC to adopt open standards; contravened JEDEC's procedures for adopting patented technologies only on the basis of full information and after securing a commitment to reasonable licensing terms; breached Rambus's duty of good faith; and also violated Rambus's specific obligation, as a member of JEDEC, to disclose patents and patent applications that might be involved in JEDEC's work[76]. Complaint Counsel claim that the facts and a proper application of the law show that Rambus violated Section 5 of the FTC Act, and they offer a proposed cease and desist order to remedy the alleged violation.

Rambus filed a cross appeal arguing that the ALJ erred by applying a "preponderance of the evidence" standard to the government's case, rather than requiring Complaint Counsel to meet a "clear and convincing" burden of proof. Rambus contends that the heightened burden of proof is required due to an "inherent tension" between the interests served by the patent and antitrust laws, as well as by similarities to cases that have required clear and convincing evidence in assessing alleged failures to disclose material information and bad faith enforcement of patents. Rambus also argues that the nature of the remedy sought by Complaint Counsel (which Rambus views as essentially terminating its patent rights), and important policy considerations implicated by SSOs, merit application of the clear and convincing standard.

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[76] CCAB at 27-28.

d. Re-Opening of the Record Before the Commission

The ALJ closed the record on October 9, 2003. The Commission later reopened the record to admit supplemental evidence – entering orders on May 13, 2005, July 20, 2005, and February 2, 2006 – after finding compelling circumstances. The first two orders reopened the record to allow the admission of documents produced in the *Infineon* litigation relating to Rambus's alleged spoliation of evidence, as well as the submission of amended proposed findings of fact and conclusions of law in light of this supplemental evidence. In the third order, the Commission reopened the record to admit documents on Rambus's back-up tapes, described as newly found, from discovery produced during the *Hynix* litigation.[77]

e. Motion for Sanctions

On August 10, 2005, Complaint Counsel moved for sanctions, asserting that Rambus had committed spoliation of evidence. Complaint Counsel asked for entry of default judgment or such other relief as the Commission deems appropriate. Rambus replied on August 17, 2005, arguing that Complaint Counsel failed to prove that Rambus acted in egregious bad faith when it adopted its document retention policy or that the effect of that policy has been to deprive Complaint Counsel of the ability to obtain a full and fair adjudication of this case.

2. Non-FTC Judicial Developments Relating to this Proceeding

Rambus is engaged in myriad litigations involving its efforts to enforce patents it claims cover JEDEC's DRAM standards. Rambus has sued, or been sued by, several of the major DRAM

[77] For discussion of the *Infineon* and *Hynix* litigation, *see infra* Section II.B.2.

manufacturers, including Samsung, Hynix, Infineon, and Micron[78]. Although Rambus and Infineon settled their litigation in 2005, all of the actions involving other companies are ongoing. In addition, the U.S. Department of Justice (DOJ) is investigating whether the major DRAM manufacturers engaged in price fixing in the DRAM market; four of those manufacturers have entered plea agreements[79]. While we will not discuss each of these non-FTC actions in detail, we will highlight certain relevant information.

In late 2000, Rambus sued Infineon Technologies AG, a manufacturer of semiconductor memory devices, in the U.S. District Court for the Eastern District of Virginia for infringement of four patents. Infineon counterclaimed, alleging Rambus committed fraud under Virginia state law by failing to disclose to JEDEC its patents and patent applications related to the organization's SDRAM and DDR SDRAM standards, as required

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[78] These actions include a variety of patent infringement and antitrust-related allegations. *See, e.g.*, Hynix Semiconductor Inc. v. Rambus Inc., No. CV-00-20905 RMW (N.D. Cal.); Rambus Inc. v. Hynix Semiconductor Inc., *et al*., No. CV-05-00334 RMW (N.D. Cal.); Rambus Inc. v. Samsung Electronics Co., No. CV-05-02298 RMW (N.D. Cal.); Samsung Electronics Co. v. Rambus, Inc., No. 3:05-CV-00406-REP (E.D. Va.); Micron Technology, Inc. v. Rambus Inc., No. 3:06-CV-00132-REP (E.D. Va.); Rambus Inc. v. Micron Technology, Inc., No. CV-06-00244 RMW (N.D. Cal.); Micron Technology, Inc. v. Rambus Inc., No. CV-00-792-KAJ (D. Del.); Rambus Inc. v. Micron Technology, Inc., *et. al.*, No. 04-431105 (San Francisco Super. Ct.).

[79] *See* Plea Agreement, United States v. Samsung Electronics Co., No. CR 05-0643 (PJH) (N.D. Cal. Nov. 30, 2005), *available at* http://www.usdoj.gov/atr/cases/f213400/213483.pdf; Plea Agreement, United States v. Hynix Semiconductor Inc., No. CR 05-249 (PJH) (N.D. Cal. May 11, 2005), *available at* http://www.usdoj.gov/atr/cases/f209200/209231.pdf; Plea Agreement, United States v. Infineon Techs. AG, No. 04-299 (PJH) (N.D. Cal. Oct. 20, 2004), *available at* http://www.usdoj.gov/atr/cases/f206700/206700.pdf; *cf.* Information, United States v. Elpida Memory, Inc., No. CR 06-0059 (MMC) (N.D. Cal. Jan. 30, 2006), *available at* http://www.usdoj.gov/atr/cases/f214300/214342.pdf.

by JEDEC's rules. During trial, Judge Payne granted judgment as a matter of law (JMOL) for Infineon, holding that Infineon did not infringe Rambus's patents. The jury later found Rambus liable for fraud associated with JEDEC's standard-setting activities on SDRAM and DDR SDRAM technologies. In response to post-trial JMOL motions by Rambus, the court set aside the jury's verdict of fraud regarding the DDR SDRAM technology, but let stand the fraud verdict regarding the SDRAM technology[80]. The court then issued an injunction against Rambus and awarded attorney fees to Infineon. Both Rambus and Infineon appealed to the Federal Circuit.

In a 2-1 opinion, the U.S. Court of Appeals for the Federal Circuit vacated the JMOL of noninfringement and remanded the case for consideration under a revised claim construction[81]. In addition, the court reversed the denial of JMOL that had allowed the SDRAM fraud verdict to stand, holding that clear and convincing evidence did not support the implicit jury finding that Rambus breached a duty to disclose its patents or patent applications as required by JEDEC's rules. Finally, the Federal Circuit upheld the district court's decision to set aside the DDR SDRAM fraud verdict. These holdings rendered the injunction against Rambus moot, and required the Federal Circuit to vacate and remand the award of attorney fees for reconsideration.

Following remand, Infineon moved to compel production of various documents that Rambus was withholding on the basis of attorney-client and work product privileges. Specifically, the motion was a continuation of an earlier motion to compel under the "crime/fraud exception" to the attorney-client privilege. In ruling on the earlier motion, the district court had concluded that

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[80] Rambus, Inc. v. Infineon Techs. AG, 164 F. Supp. 2d 743 (E.D. Va. 2001).

[81] Rambus, Inc. v. Infineon Techs. AG, 318 F.3d 1081 (Fed. Cir. 2003).

"Rambus implemented a 'document retention policy,' in part, for the purpose of getting rid of documents that might be harmful in litigation."[82]

On May 18, 2004, the district court entered a second order compelling Rambus to produce additional documents[83]. Under this order, the court held that the crime/fraud exception extends to materials or communications created in planning, or in furtherance of, spoliation of evidence[84]. The court also found that Rambus's intentional destruction of documents was "an integral part of its licensing and litigation strategy."[85] The court then required Rambus to produce certain documents that Rambus had claimed were privileged, and allowed Infineon to conduct discovery on the appropriate sanctions for Rambus's behavior.[86]

In March 2005, at the conclusion of a bench trial, Judge Payne orally dismissed Rambus's patent claims against Infineon. The court found that Infineon had proven, by clear and convincing evidence, that Rambus possessed unclean hands and that Rambus had engaged in extensive spoliation of evidence[87]. Before Judge Payne issued a written opinion setting forth his findings, however, Rambus and Infineon settled all of their pending litigation, including the case before Judge Payne.

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[82] *See* Rambus, Inc. v. Infineon Techs. AG, 155 F. Supp.2d 668, 682 (E.D. Va. 2001).

[83] Rambus, Inc. v. Infineon Techs. AG, 222 F.R.D. 280 (E.D. Va. 2004).

[84] *Id.* at 290.

[85] *Id.* at 298.

[86] *Id*. at 299.

[87] *See* Samsung Elecs. Co. v. Rambus, Inc., 398 F. Supp. 2d 470, 473 (E.D. Va. 2005) (discussing Judge Payne's ruling).

As mentioned above, the *Infineon* litigation was only one of many actions involving Rambus and the major semiconductor companies. The other cases have yet to reach a resolution, but there have been some developments worth noting. In *Hynix Semiconductor, et al. v. Rambus Inc.*, the federal district court for the Northern District of California held a two-week trial on Hynix's unclean hands defense to Rambus's patent infringement claims. Judge Whyte issued an opinion on January 4, 2006, concluding that Hynix's defense failed, after finding that Rambus "did not engage in unlawful spoliation of evidence" and that "the evidence presented does not bear out Hynix's allegations that Rambus adopted its Document Retention Policy in bad faith."[88] On April 24, 2006, a jury found that Hynix had infringed Rambus's patents and awarded Rambus damages of $307 million[89]. On July 17, 2006, Judge Whyte granted summary judgment to Rambus on Hynix's claims based on breach of contract, promissory estoppel, and constructive fraud but denied summary judgment for Rambus on Hynix's claims based on allegations of actual fraud[90]. The court also determined that "breach of the JEDEC disclosure policies, without more, cannot give rise to antitrust liability," but it ruled that "Hynix is not barred from asserting that Rambus's overall course of conduct, which may include the circumstances and intent behind its

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[88] Hynix Semiconductor Inc. v. Rambus Inc., No. CV-00-20905 RMW, 2006 WL 565893, at *25, *28 (N.D. Cal. Jan. 5, 2006).

[89] *See* Special Verdict Form, Hynix Semiconductor Inc. v. Rambus Inc., No. CV-00-20905 RMW (N.D. Cal. Apr. 24, 2006), *available at* www.cand.uscourts.gov/cand/judges.nsf/bc83a5777591b96f88256d480060b73c/3db5d3212d350fc88825715a005f7b13/$FILE/00-20905.pdf. The court subsequently ordered a new trial on the issue of damages, but gave Rambus the option of accepting damages in the amount of $134 million. Hynix Semiconductor Inc. v. Rambus Inc., No. CV-00-20905 RMW, 2006 WL 1991760 (N.D. Cal. July 14, 2006).

[90] Hynix Semiconductor Inc. v. Rambus Inc., No. CV-00-20905 RMW, 2006 WL 2038357, at *5-9 (N.D. Cal. July 17, 2006).

decision to not disclose its patents and patent applications, violated antitrust laws."[91] Hynix's remaining contentions that the patents are unenforceable have not yet been tried.

In *Micron v. Rambus*, currently pending in the U.S. District Court for the District of Delaware, a Special Master recently issued recommendations to the court on the disposition of Micron's motion to compel. Micron sought the production of certain privileged documents pursuant to the crime/fraud exception. In his report to the judge, the Special Master found that the exception did not apply, in part because there was no evidence of fraud. That finding, in turn, rested on an analysis of JEDEC's rules, similar to the analysis set forth in the Federal Circuit's *Infineon* decision[92]. The district court affirmed that analysis and conclusion, based on Virginia state fraud law.[93]

Finally, in *Samsung v. Rambus*, the U.S. District Court for the Eastern District of Virginia recently concluded that Rambus had engaged in spoliation of evidence by destroying documents likely to be relevant at a time when Rambus anticipated or reasonably should have anticipated litigation[94]. Ruling in the context of Samsung's motion for an award of attorney's fees, the court found that Rambus planned for litigation throughout 1998 and 1999 and, "as part of the plan . . . implemented a pervasive document

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[91] *Id*. at *12.

[92] Special Master's Report and Recommendations on Motion of Micron Technology to Compel Defendant Rambus to Produce Certain Documents, Testimony and Pleadings, Micron Tech., Inc. v. Rambus Inc., CV-00-792-KAJ (D. Del. Mar. 6, 2006).

[93] Memorandum Order, *Micron v. Rambus*, CV-00-792-KAJ, 2006 WL 1653136 (D. Del. June 15, 2006).

[94] Samsung Elecs. Co. v. Rambus Inc., No. 3:05-CV-00406-REP, 2006 WL 2038417 (E.D.Va. July 18, 2006).

destruction program" that targeted "discoverable documents."[95] The court deemed the contrary ruling in *Hynix* "not persuasive."[96]

III. STANDARD OF REVIEW

We review the record *de novo* by considering "such parts of the record as are cited or as may be necessary to resolve the issues presented and . . . exercis[ing] all the powers which [the Commission] could have exercised if it had made the initial decision."[97] *De novo* review is particularly appropriate in this case because we must consider supplemental evidence, as well as new proposed findings of fact and conclusions of law, that were unavailable to the ALJ[98]. In light of our plenary review, we set aside all findings and conclusions of the ALJ, other than those that are expressly cited and relied upon.

A. Standard of Proof: The Preponderance of the Evidence Standard Applies in FTC Adjudications

FTC enforcement actions typically are governed by the preponderance of the evidence standard[99]. The Supreme Court has

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[95] *Id*. at *42.

[96] *Id*. at *38.

[97] 16 C.F.R. § 3.54 (2005).

[98] The record was reopened on separate occasions after the Initial Decision to admit documents relating to Rambus's alleged spoliation of evidence and documents on Rambus's newly found backup tapes. *See supra* Section II.B.

[99] *See, e.g.*, In re Adventist Health System West, 117 F.T.C. 224, 297 (1994) ("Each element of the case must be established by a preponderance of the evidence"); FTC v. Abbott Laboratories, 853 F. Supp. 526, 535 (D.D.C. 1994) (government must show "by a preponderance of the evidence that [respondent's] action was the result of collusion with its competitors").

held that Section 7(c) of the Administrative Procedure Act (APA), which is applicable to administrative adjudicatory proceedings unless otherwise provided by statute, establishes "a standard of proof and . . . the standard adopted is the traditional preponderance-of-the evidence standard."[100] Furthermore, the preponderance of the evidence standard generally applies in civil suits to enforce federal statutes such as the antitrust laws[101]. Rambus acknowledges that the preponderance of the evidence standard applies in most agency adjudicatory proceedings, including FTC adjudications[102]. Nevertheless, Rambus advances four arguments why the Commission should apply the clear and convincing evidence standard in this matter.[103]

1. Relationship between Patent and Antitrust Law in Cases Involving Fraud on the Patent Office or Patent Enforcement Initiated in Bad Faith

Rambus argues that "Complaint Counsel should bear the burden of proving the essential elements of their claims by clear and convincing evidence"[104] because of what it terms the "inherent tension between the patent and antitrust laws."[105] Rambus's attempt, however, to broaden the applicability of the clear and convincing evidence standard based on "inherent

[100] Steadman v. SEC, 450 U.S. 91, 95-102 (1981) (considering standard of proof in SEC proceedings adjudicating alleged violations of the anti-fraud provisions of the securities laws).

[101] *See* Herman & MacLean v. Huddleston, 459 U.S. 375, 387-91 (1983).

[102] RB at 134.

[103] RB at 134-40.

[104] RB at 140.

[105] RB at 134.

tension" between the patent and antitrust laws is unavailing. Patents are not inherently in tension with antitrust law. Patents do not necessarily create market power[106]. More fundamentally, competition and patent policy both are aimed at encouraging innovation that benefits consumers, and generally work well together in doing so.[107]

Nevertheless, Rambus suggests that two cases, in particular, support an extension of the clear and convincing standard to the facts in this proceeding. Neither case creates such a broad rule. The first case Rambus relies on is the Supreme Court's decision in *Walker Process Equipment v. Food Machinery & Chemical Corp*[108]. In *Walker Process*, the Supreme Court held that a patentee may be liable for violation of the antitrust laws if it enforces a patent obtained by knowing and willful fraud on the PTO, and if all other elements of a violation of Section 2 of the

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[106] Ill. Tool Works, Inc. v. Indep. Ink, Inc., 126 S. Ct. 1281 (2006); *see also* U.S. DEP'T OF JUSTICE & FED. TRADE COMM'N, ANTITRUST GUIDELINES FOR THE LICENSING OF INTELLECTUAL PROPERTY ¶ 2.2 (1995) [hereinafter IP GUIDELINES], *available at* http://www.ftc.gov/bc/0558.pdf.

[107] *See* Atari Games Corp. v. Nintendo of America, Inc., 897 F.2d 1572, 1576 (Fed. Cir. 1990) ("[T]he aims and objectives of patent and antitrust laws may seem, at first glance, wholly at odds. However, the two bodies of law are actually complementary, as both are aimed at encouraging innovation, industry and competition."); IP GUIDELINES, supra note 106, ¶ 1.0 (the patent and antitrust laws "share the common purpose of promoting innovation and enhancing consumer welfare"); FED. TRADE COMM'N, TO PROMOTE INNOVATION: THE PROPER BALANCE OF COMPETITION AND PATENT LAW AND POLICY, ch. 1 at 7-9 (2003) [hereinafter FTC INNOVATION REPORT], *available at* http://www.ftc.gov/os/2003/10/innovationrpt.pdf. When market power does result, "Antitrust law recognizes that a patent's creation of monopoly power can be necessary to achieve a greater gain for consumers." *Id*. at 9. Correspondingly, "[T]he Patent Clause itself reflects a balance between the need to encourage innovation and the avoidance of monopolies which stifle competition without any concomitant advance in the 'Progress of Science and useful Arts.'" Bonito Boats, Inc. v. Thunder Craft Boats, 489 U.S. 141, 146 (1989) (quoting Article 1, Section 8 of the Constitution).

[108] 382 U.S. 172 (1965).

Sherman Act are established[109]. The rationale for this holding was to achieve "a suitable accommodation" between policies of the patent and antitrust laws by enjoining enforcement of a patent that conferred monopoly power when the patent was "procured by deliberate fraud."[110] Complaint Counsel in this case do not, however, allege that Rambus procured its patents through fraud on the PTO. Rather, it is alleged that Rambus manipulated the JEDEC standard-setting process by engaging in deceptive conduct, resulting in the unknowing adoption of standards that included Rambus's lawfully patented technologies.

Rambus's reliance on *Handgards, Inc. v. Ethicon, Inc.*[111] is similarly misplaced. The plaintiff there based a monopolization claim on allegations that the patentee pursued infringement actions in bad faith – with the knowledge that the patents, though lawfully obtained, were invalid[112]. To provide a "means whereby the bad faith infringement action can be identified post hoc with a sufficiently high degree of certainty," the court held that an

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[109] *Id.* at 172, 175-77.

[110] *Id.* at 189-90 (J. Harlan, concurring); *see also id*. at 176; Nobelpharma AB v. Implant Innovations, Inc., 141 F.3d 1059, 1068-69 (Fed. Cir. 1998) (discussing the context in which the Supreme Court established the requirement of knowing and willful fraud). Subsequent cases established that, in *Walker Process* contexts, knowing and willful fraud on the PTO must be proven by clear and convincing evidence. *See* C. R. Bard, Inc. v. M3 Systems, Inc., 157 F.3d 1340, 1365 (Fed. Cir. 1998) (indicating that clear and convincing evidence is necessary because of "the ease with which routine patent prosecution may be portrayed as tainted conduct"); Caphote Corp. v. DeSoto Chemical Coatings, Inc., 450 F.2d 769, 772 (9th Cir. 1971) (justifying the clear and convincing evidence standard for finding *Walker Process* fraud on grounds of the "tortuous" road to the Patent Office and the complexity of patent litigation).

[111] 601 F.2d 986 (9th Cir. 1979).

[112] 601 F.2d at 986, 993-94 (noting that bad faith "is a subjective state of mind the existence of which, while not susceptible to certain proof, easily can spring from suggestive and weakly corroborative circumstances").

infringement suit presumptively is filed in good faith, and that the presumption can be rebutted only by clear and convincing evidence[113]. The court acknowledged that the clear and convincing standard is "not one intended to be utilized in antitrust litigation generally," and expressly limited its holding on the use of the clear and convincing standard to "proceedings in which the alleged violation of the antitrust law consists solely of one or more infringement actions initiated in bad faith."[114] This case, however, involves allegations of deceptive conduct in the context of SSO activities; Rambus is not accused of initiating infringement actions in bad faith.

In short, the cases cited by Rambus do not support its assertion that the clear and convincing standard applies to the elements of this antitrust case because it happens to involve a patent. The Commission is not charged with deciding whether Rambus committed fraud on the PTO, or whether Rambus initiated its infringement actions in bad faith. The issue in the case before the Commission is whether Rambus, through its participation in JEDEC and in the context of JEDEC's standard-setting processes, engaged in a deceptive course of conduct under

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[113] *Id.* at 993, 996 (noting that the clear and convincing standard in *Walker Process* and *Handgards* is commensurate with the statutory presumption of patent validity, 35 U.S.C. § 282). *See also* CVD, Inc. v. Raytheon Co., 769 F.2d 842, 850 (1st Cir. 1985) ("a patentee who has a good faith belief in the validity of a patent will not be exposed to antitrust damages even if the patent proves to be invalid, or the infringement action unsuccessful"), *cert. denied*, 475 U.S. 1016 (1986).

[114] *Id*. Other cases cited by Rambus arose in similar contexts. *See* Loctite Corp. v. Ultraseal, Ltd., 781 F.2d 861, 876-77 (Fed. Cir. 1985) (requiring a clear and convincing showing that a plaintiff brought a patent infringement suit in bad faith, knowing that there was no infringement), *overruled on other grounds*, Nobelpharma AB v. Implant Innovations, Inc. 141 F.3d 1059, 1068 (Fed. Cir. 1998); *CVD*, 769 F.2d at 849-51 (requiring an antitrust plaintiff to prove bad faith assertion of trade secrets – with knowledge that no trade secrets existed – by clear and convincing evidence).

Section 5 of the FTC Act[115]. No court has held that clear and convincing evidence is required to establish Section 5 deception[116]. To the contrary, as previously stated, the Supreme Court held that Section 7(c) of the APA establishes "a standard of proof and that the standard adopted is the traditional preponderance-of-the evidence standard."[117]

2. Standard of Proof Should Be Commensurate With Proposed Remedy

Rambus's second argument – that a heightened standard of proof is necessary because Complaint Counsel seek to bar enforcement of Rambus's patents under certain circumstances – in effect would allow one potential remedy to determine the standard for establishing whether a violation of the antitrust laws occurred. The potential remedy should not influence the standard of proof for liability[118]. To the extent Rambus's arguments might be

[115] *See, e.g.*, Complaint ¶¶ 2, 122-24.

[116] *See generally* FTC v. Algoma Lumber Co., 291 U.S. 67, 78-81 (1934) (holding that proof of fraud is not required to prove Section 5 deception).

[117] *See* Steadman v. SEC, 450 U.S. 91, 95-102 (1981).

[118] None of the cases cited by Rambus in its briefs support this contention. *See* CVD v. Raytheon Co., 769 F.2d 842 (1st Cir. 1985) (appeal to set aside jury verdict; no ruling that remedy sought should determine standard of proof); Livingstone v. North Belle Vernon Borough, 91 F.3d 515 (3d Cir. 1996) (action to determine voluntariness of an oral release-dismissal agreement that waived all civil claims in exchange for dismissal of criminal case; holding that "clear and convincing" evidentiary standard should apply in narrow context of evaluating voluntariness of oral release-dismissal agreements); Shepherd v. Am. Broad. Cos., Inc. , 62 F.3d 1469 (D.C. Cir. 1995) (appeal of judicial sanctions; "clear and convincing" evidentiary standard not used to determine merits of the case); Lindahl v. Office of Personnel Management, 470 U.S. 768 (1985) (addressed issue of whether a federal worker may appeal an agency's denial of disability retirement claim to the Federal Circuit; no ruling that "clear and convincing" evidentiary standard should apply to determine merits of federal worker's underlying claim).

relevant to our consideration of particular remedies, we will address them in that context.

We note, however, that even a remedy barring enforcement of a patent does not necessarily require a heightened standard of proof. The equitable estoppel defense to patent infringement provides an example. A patentee's infringement claim may be barred if an alleged infringer establishes the elements of equitable estoppel (*i.e.*, misleading conduct, reliance, and material prejudice). The Federal Circuit has held that these elements ordinarily must be proven only by a preponderance of the evidence, noting that the clear and convincing standard applies to civil cases only when special circumstances are present.[119]

3. Chilling Participation in SSOs

We are unpersuaded by Rambus's third argument that a heightened burden of proof is necessary to avoid chilling procompetitive participation in standard-setting activities. This argument implicitly assumes that the usual burden of proof, if applied to antitrust claims involving SSOs, somehow will reduce incentives to engage in beneficial standard-setting activities. Rambus provides, and we find, no basis for that assumption.

Rambus's argument ignores the potentially serious chilling effect of deceptive conduct in the SSO context. The Complaint alleged that Rambus deliberately sought to acquire a monopoly by using a standard-setting process to engage in patent hold-up. That

[119] *See* A.C. Aukerman Co. v. R.L. Chaides Constr. Co., 960 F.2d 1020, 1045-46 (Fed. Cir. 1992) (because no "special considerations are implicated by the defense of equitable estoppel as we defined it, we adopt the preponderance of the evidence standard in connection with the proof of equitable estoppel factors, absent special circumstances, such as fraud or intentional misconduct"). The antitrust case before the Commission does not entail the types of circumstances that have supported the requirement of clear and convincing evidence in other cases.

conduct, if established, might itself chill participation in cooperative standard-setting activities[120]. The success of cooperative standard setting depends on some assurance that other participants will not exploit the process by acting deceptively[121]. Requiring a heightened burden of proof when analyzing deception in the SSO context would diminish that assurance.

4. Reliance on Testimony Rather than Contemporaneous Written Evidence

Rambus's fourth argument – that clear and convincing evidence should be required because Complaint Counsel rely on "strained and faded memories"[122] – lacks both legal and factual support. Rambus has not identified a single judicial opinion to support its claim that delayed testimony triggers a heightened evidentiary standard, even though delayed testimony is hardly unusual in litigation. The absence of such opinions is unsurprising: the rule proffered by Rambus would reward

[120] *See, e.g.*, CX 2384 (letter from G. Kelley of IBM regarding a member's failure to disclose patents to JEDEC, stating: "I am and have been concerned that this issue can destroy the work of JEDEC. If we have companies leading us into their patent collection plates, then we will no longer have companies willing to join the work of creating standards"); Appleton, Tr. 6331-32 (if a company enforced a patent after failing to disclose it to JEDEC, it would "very much affect whether Micron participated [in JEDEC] or not"); Rhoden, Tr. 535-38 (Rambus's suits to enforce its patents relating to the JEDEC standards would cause "a fundamental shift away from open industry standardization"); Bechtelsheim, Tr. 5889 (if the "trust into the nature of an open standards process is violated, it makes it very difficult for me to rely on the standards groups developing standards").

[121] *Cf.* HERBERT HOVENKAMP ET AL., II IP AND ANTITRUST § 35.6 at 35-53 (Supp. 2003) (terming a standard-setting organization's desire "to make a fully informed decision on whether to adopt a particular standard" a "presumptively legitimate reason for requiring" disclosure of intellectual property).

[122] *See* RB at 140, RRB at 5.

defendants/respondents who engage in protracted deception and then foster pre-trial delays. In any event, Complaint Counsel in this case rely on contemporaneous documentary evidence in addition to the testimony of numerous witnesses. Many of Complaint Counsel's documentary exhibits are discussed throughout this Opinion.

* * * * *

In sum, Rambus failed to establish a basis for the Commission to impose a heightened "clear and convincing" evidentiary standard to determine liability in this case. Rather, Complaint Counsel have the burden to prove the necessary elements of liability by a preponderance of the evidence, in keeping with the normal rules applicable in FTC adjudications.[123]

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[123] Although the ALJ rejected Rambus's proposed clear-and-convincing standard, he achieved much the same result by citing United States v. United States Gypsum Co., 333 U.S. 364 (1948), for the proposition that "where trial testimony is in conflict with contemporaneous documents, the trial testimony is entitled to little weight." *See* ID at 264-65. *Gypsum* actually was considerably more limited. After noting that "counsel were permitted to phrase their questions in extremely leading form, so that the import of the witnesses' testimony was conflicting" and that the testimony dealt with whether known conduct had involved actions taken in concert, the Court ruled, "Where such testimony is in conflict with contemporaneous documents, we can give it little weight, particularly when the crucial issues involve mixed questions of law and fact." 333 U.S. at 395-96. The ALJ ignores *Gypsum*'s limits and misapplies its rule. We find no inconsistency between the documents and testimony sufficient to invoke broad usage of the rule in *Gypsum*.

The ALJ found the *Gypsum* rule "especially appropriate here, where witnesses would directly benefit from the outcome of this litigation because they work for companies that either manufacture or use DRAMS that may infringe Rambus's patents, work for entities that are entirely controlled by DRAM manufacturers, or are committed to developing technologies that will compete with Rambus's technologies." ID at 265. This standard would call into question the utility and reliability of trial procedures in virtually all antitrust cases. In antitrust litigation, witnesses inevitably are "interested," in the sense that they represent one economic actor or another. In this proceeding, *both* Rambus's and Complaint Counsel's witnesses have an interest in the

IV. MONOPOLIZATION CLAIM[124]

Section 2 of the Sherman Act makes it unlawful to "monopolize, or attempt to monopolize, or combine or conspire with any other person or persons, to monopolize any part of the trade or commerce among the several States, or with foreign nations . . . ."[125] The Supreme Court has identified the basic elements of the offense:

> The offense of monopoly under § 2 of the Sherman Act has two elements: (1) the possession of monopoly power in the relevant market and (2) the willful acquisition or maintenance of that power as distinguished from growth or development as a

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outcome; depreciating their evidence on that basis indicts all live witness testimony. Economic interest gives us no basis to find that trial procedures – such as requiring a foundation for evidence and subjecting witnesses to cross-examination – are inadequate to compile a reliable record. Therefore, absent a specific reason to question the credibility or reliability of a specific witness or a specific statement, we find no basis to discredit any of the testimony in the record.

[124] Because we find that Rambus unlawfully monopolized the four relevant markets delineated by Complaint Counsel (and whose definition was not contested by Rambus), we need not consider the further allegations that Rambus attempted to monopolize those markets or that Rambus's conduct otherwise constituted an unfair method of competition.

[125] 15 U.S.C. § 2. The Commission's authority under Section 5 of the FTC Act reaches conduct that violates the Sherman Act. *See, e.g.*, FTC v. Cement Inst., 333 U.S. 683, 694-95 (1948); Fashion Originators' Guild of America v. FTC, 312 U.S. 457, 463 (1941); Polygram Holdings, Inc., 5 Trade Reg. Rep. (CCH) ¶ 15,453 at 22,452 n.11 (FTC 2003), *available at* http://www.ftc.gov/os/2003/07/polygramopinion.pdf (slip op. at 13 n.11), *enforcement ordered*, Polygram Holding, Inc. v. FTC, 416 F.3d 29 (D.C. Cir. 2005).

> consequence of a superior product, business acumen, or historic accident.[126]

The fundamental issues in this case are: (1) whether Rambus engaged in exclusionary conduct; (2) whether Rambus acquired monopoly power; and (3) whether there is a causal link between Rambus's conduct and its monopoly power. We consider each of these issues in turn.

A. Exclusionary Conduct

1. Framework for Analysis

From the earliest days of Section 2 jurisprudence, courts have held that unilateral conduct, absent an "anticompetitive" or "exclusionary" element, is benign – even if it creates or maintains monopoly power, or is dangerously likely to do so – because "the successful competitor, having been urged to compete, must not be turned upon when he wins."[127] As the Supreme Court noted in *Spectrum Sports, Inc. v. McQuillan*,[128] "[t]he law directs itself not against conduct which is competitive, even severely so, but against conduct which unfairly tends to destroy competition itself."[129]

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[126] United States v. Grinnell Corp., 384 U.S. 563, 570-71 (1966); *see also* Verizon Communs., Inc. v. Law Offices of Curtis V. Trinko, 540 U.S. 398, 407 (2004) (terming the *Grinnell* formulation "settled law").

[127] United States v. Alcoa, 148 F.2d 416, 430-31 (2d Cir. 1945). *See also Verizon v. Trinko*, 540 U.S. at 407 ("To safeguard the incentive to innovate, the possession of monopoly power will not be found unlawful unless it is accompanied by an element of anticompetitive conduct.") (emphasis omitted).

[128] 506 U.S. 447 (1993).

[129] *Id.* at 458.

Exclusionary conduct is "conduct other than competition on the merits – or other than restraints reasonably 'necessary' to competition on the merits – that reasonably appear[s] capable of making a significant contribution to creating or maintaining monopoly power."[130] Stated differently, if "a firm has been attempting to exclude rivals on some basis other than efficiency," it is engaging in exclusionary conduct[131]. The focus, at all times, is on harm to competition, not merely harm to competitors.[132]

The exclusionary element alleged here is that Rambus engaged in a course of deceptive conduct[133]. Complaint Counsel assert that Rambus created the misimpression that it was not seeking relevant patents, thereby misleading JEDEC members regarding the price of Rambus's technology and thwarting their ability to make informed choices. This sort of deceptive conduct is not competition on the merits. Just as "false or misleading advertising has an anticompetitive effect,"[134] distorting choices

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[130] III PHILLIP E. AREEDA & HERBERT HOVENKAMP, ANTITRUST LAW ¶ 651f, at 83-84 (2d ed. 2002). Several courts have relied on this definition. *See, e.g.*, Aspen Skiing Co. v. Aspen Highlands Skiing Corp., 472 U.S. 585, 605 n.32 (1985); Multistate Legal Studies, Inc. v. Harcourt Brace Jovanovich Legal & Prof'l Publ'ns, Inc., 63 F.3d 1540, 1550 (10th Cir. 1995), *cert. denied*, 516 U.S. 1044 (1996); Town of Concord v. Boston Edison Co., 915 F.2d 17, 21 (1st Cir. 1990), *cert. denied*, 499 U.S. 931 (1991).

[131] *See Aspen Skiing*, 472 U.S. at 605 ("If a firm has been 'attempting to exclude rivals on some basis other than efficiency,' it is fair to characterize its behavior as predatory") (footnote omitted), quoting ROBERT H. BORK, THE ANTITRUST PARADOX 138 (1978).

[132] *See, e.g.*, Nynex Corp. v. Discon, Inc., 525 U.S. 128, 139 (1998) (requiring harm to "the competitive process"); *Town of Concord*, 915 F.2d at 21-22 (requiring harm to "the competitive process" such as by obstructing the achievement of lower prices, better products, or more efficient production methods); III AREEDA & HOVENKAMP, ANTITRUST LAW ¶ 651c, at 78-79.

[133] Complaint, ¶¶ 2, 122-24.

[134] Cal. Dental Ass'n v. FTC, 526 U.S. 756, 771 n.9 (1999).

through deception obscures the relative merits of alternatives and prevents the efficient selection of preferred technologies.[135]

The courts have established that deception may constitute "exclusionary conduct" that will support a Section 2 claim in appropriate circumstances[136]. In *United States v. Microsoft*, for example, the United States Court of Appeals for the District of Columbia Circuit found that Microsoft's deception with respect to Java applications was exclusionary[137]. As discussion of the legal and factual circumstances and the nature of Rambus's conduct makes clear, proof of the deceptive conduct alleged in this case would establish the exclusionary element required by Section 2.

We stand on familiar ground when we evaluate whether Rambus engaged in a deceptive course of conduct. Section 5 of the FTC Act proscribes, *inter alia*, deceptive acts and practices, and accordingly, the Commission has developed special expertise to determine whether conduct is deceptive[138]. Lest there be any doubt as to the elements of deceptive conduct under Section 5, those elements were spelled out in the Commission's 1983 Policy

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[135] *Cf.* FTC v. Ind. Fed'n of Dentists, 476 U.S. 447, 461-62 (1986) (describing the anticompetitive consequences of "an effort to withhold (or make more costly) information desired by consumers for the purpose of determining whether a particular purchase is cost justified").

[136] *See* Conwood Co., LP v. U.S. Tobacco Co., 290 F.3d 768 (6th Cir. 2002) (maintaining monopoly power by, *inter alia*, providing misleading market data to retailers in order to distort their purchasing decisions violated Section 2); Caribbean Broad. Sys. Ltd. v. Cable & Wireless PLC, 148 F.3d 1080, 1087 (D.C. Cir. 1998); International Travel Arrangers, Inc. v. Western Airlines, 623 F.2d 1255, 1262-63, 1270 (8th Cir.), *cert. denied*, 449 U.S. 1063 (1980).

[137] *See* United States v. Microsoft Corp., 253 F.3d 34, 76-77 (D.C. Cir. 2001); s*ee also infra* Section IV.A.1.b. (discussing the *Microsoft* case).

[138] FTC v. Colgate-Palmolive Co., 380 U.S. 374, 391-92 (1965); Kraft, Inc. v. FTC, 970 F.2d 311 (7th Cir. 1992).

Statement on Deception (Policy Statement),[139] which the courts have treated as the definitive description of those elements under the FTC Act.[140]

According to the Policy Statement, for conduct to be found deceptive, there must have been a "misrepresentation, omission or practice" that was "material" in that it was likely to mislead "others acting reasonably under the circumstances" and thereby likely to affect their "conduct or decision[s]." Thus, in order to determine whether conduct (including a course of conduct) is deceptive, we must consider "the circumstances" in which the alleged "misrepresentation, omission or practice" occurred. We analyze the legal circumstances, factual circumstances, and nature of the conduct itself in assessing Rambus's conduct.

a. Legal Circumstances

Because this is a monopolization case, Rambus's allegedly deceptive conduct ultimately must be analyzed under Section 2 of the Sherman Act[141]. That requires two modifications to the analysis articulated by the Policy Statement. First, under the Policy Statement, the respondent's state of mind is irrelevant in determining whether the respondent engaged in deceptive conduct under Section 5. Under Section 2, however, the defendant must act "willfully" in acquiring or maintaining monopoly power.

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[139] Federal Trade Commission, *Policy Statement on Deception* (1983), *reprinted in* 4 Trade Reg. Rep. (CCH) ¶ 13,205 at 20,911-12 [hereinafter *Policy Statement*].

[140] Novartis Corp. v. FTC, 223 F.3d 783 (D.C. Cir. 2000); FTC v. Pantron I Corp., 33 F.3d 1088 (9th Cir. 1994), *cert. denied*, 514 U.S. 1083 (1995).

[141] Whatever the potential breadth of Section 5 of the FTC Act in these circumstances, our analysis in this opinion rests on the traditional criteria for evaluating allegations of monopolization under Section 2 of the Sherman Act.

Thus, for Rambus's allegedly deceptive course of conduct to be actionable under the Sherman Act, Rambus must have acted "willfully," as opposed to inadvertently or even negligently.[142]

Second, the Policy Statement does not require proof of competitive harm for a respondent's conduct to be deemed deceptive under Section 5. However, under Section 2, in order to be condemned as "exclusionary," defendant's conduct must harm the competitive process, and that anticompetitive harm must outweigh the conduct's procompetitive benefits, if any[143]. Thus, for Rambus's alleged deceptive course of conduct to be actionable under Section 2, the conduct must have an anticompetitive effect that outweighs any procompetitive benefit.

Rambus argues that we should apply the "sacrifice test" as the framework for our analysis. That is, its conduct should be deemed exclusionary only if it would have been unprofitable to the defendant – if the defendant would have sacrificed profits – "but for" the expectation that the conduct would exclude rivals and permit the defendant to recoup its losses via the acquisition of long-run monopoly power[144]. Stated more generally, the so-called sacrifice test condemns conduct that would not make "economic

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[142] Some commentators have noted that the term "willful" often provides only limited guidance: "every firm 'willfully' maintains its profits or market share . . . ." III AREEDA & HOVENKAMP, ANTITRUST LAW, *supra* note 130, ¶ 651 at 76. They posit that courts often have "focused on conduct while talking about intent." *Id.* In the context of deceptive conduct, however, willfulness helps in determining "whether the challenged conduct is fairly characterized as 'exclusionary' or 'anticompetitive,'" Aspen Skiing, Co. v. Aspen Highlands Skiing Corp., 472 U.S 585, 602 (1985), by distinguishing intentionally deceptive conduct from conduct that, while misleading, is merely inadvertent or negligent.

[143] United States v. Microsoft Corp., 253 F.3d 34, 58-59 (D.C. Cir. 2001).

[144] RB at 110-12.

sense" but for the elimination or lessening of competition[145]. Rambus contends that keeping information about its patent applications secret and refusing to share that information with competitors was beneficial to Rambus, regardless of what happened at JEDEC, and therefore could not be exclusionary[146]. The ALJ concurred[147]. We believe this was error both as a matter of law and as a matter of fact.

As a matter of law, we recognize that the sacrifice test may be well-suited to certain types of Section 2 claims where the risk of interfering with vigorous competitive activity is heightened,[148] but the test is not appropriate here. It misses conduct that reduces consumer welfare, but happens to be inexpensive to execute, and therefore does not involve a significant profit sacrifice. For example, defrauding the PTO in order to secure a patent that

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[145] *See* A. Douglas Melamed, *Exclusive Dealing Arrangements and Other Exclusionary Conduct – Are There Unifying Principles?*, 73 ANTITRUST L.J. 375, 389-403 (2006) (stating views of counsel for Rambus in this proceeding).

[146] RB at 113-15.

[147] *See* ID at 286-87, 289, 292.

[148] Some court decisions have employed the test's underlying concept in the context of predatory pricing. *See, e.g.*, Matsushita Elec. Indus. Co. v. Zenith Radio Corp., 475 U.S. 574, 588-89 (1986) (explaining that pricing below competitive levels entails forgoing profits and that, to make this rational, there must be a reasonable expectation of later recoupment through monopoly profits); Concord Boat Corp. v. Brunswick Corp., 207 F.3d 1039, 1062 (Cir. 2000); Conoco Inc. v. Inman Oil Co., 774 F.2d 895. 905-06 (8th Cir. 1985). Other court decisions have applied similar thinking to unilateral refusals to deal with rivals. *See, e.g.*, Morris Communications v. PGA Tour, 364 F.3d 1288, 1295 (11th Cir.), *cert. denied*, 125 S.Ct. 87 (2004); *cf.* Verizon Communs., Inc. v. Law Offices of Curtis V. Trinko, 540 U.S. 398, 409 (2004) (explaining that in the *Aspen Skiing* refusal-to-deal case, "[t]he unilateral termination of a voluntary (*and thus presumably profitable*) course of dealing suggested a willingness to forsake short-term profits to achieve an anticompetitive end") (emphasis original).

confers a monopoly demands little profit sacrifice, yet the Supreme Court has held that such fraud can violate Section 2[149]. Likewise, in this case, without reducing prices, forgoing sales, or even spending substantial funds beyond what it otherwise would have spent, Rambus's conduct may have imposed substantial costs on rivals and contributed significantly to the creation of monopoly power. In cases such as this, the *Microsoft* analysis – with its focus on determining "whether the monopolist's conduct on balance harms competition"[150] – is the proper lens for scrutinizing allegedly exclusionary conduct.[151]

b. Factual Circumstances

The factual context in which the alleged conduct occurred is critical. For example, in *Microsoft*, the D.C. Circuit concluded that Microsoft violated Section 2 by making misleading statements to Independent Software Vendors (ISVs) in a context

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[149] *See* Walker Process Equipment, Inc. v. Food Mach. & Chem. Corp., 382 U.S. 172 (1965).

[150] *Microsoft*, 253 F.3d at 58-59.

[151] *See* Caribbean Broad. Sys. Ltd. v. Cable & Wireless PLC, 148 F.3d 1080, 1087 (D.C. Cir. 1998) (noting that anticompetitive conduct takes "many different forms" and is highly "dependent on context"). Although Rambus highlights FTC/DOJ support for the sacrifice test in various briefs, the agencies have made it clear that exclusionary conduct "need not always entail economic sacrifice." Brief of Amici Curiae United States & Federal Trade Commission on Writ of Certiorari at 11 n.2 (Dec. 2002), Verizon v. Trinko, 540 U.S. 398 (No. 02-682). Indeed, the agencies suggested a standard that would condemn conduct with harm to competition "disproportionate" to its benefits – along the lines of *Microsoft's* balancing test – for purposes of assessing opportunistic behavior in the standard-setting process. Brief of Amici Curiae United States & Federal Trade Commission at 14-15 (May 2003), *Trinko* (No. 02-682). The agencies urged reserving the "sharper focus" provided by the sacrifice test for situations such as the refusal-to-aid-rivals claim presented in *Trinko*, for which antitrust interference was thought likely to offer "infrequent pro-competitive benefits" and "frequent anticompetitive risks." *Id*. at 15, 17.

in which the ISVs reasonably could have expected that Microsoft would *not* mislead them. Specifically, Microsoft publicly committed to cooperate with Sun Microsystems (Sun), and also offered ISVs a set of "Java implementation tools" that ostensibly would enable them to develop cross-platform applications[152]. Thus, there was a reasonable expectation that the relationship between Microsoft and Sun and, more importantly, between Microsoft and the ISVs, would be characterized by cooperation, not deception. The record showed, however, that Microsoft sought to use unwitting ISVs to generate Windows-dependent applications that were incompatible with other platforms. To that end, Microsoft surreptitiously included in its implementation tools certain key words or directives that could be executed solely by Microsoft's version of the Java runtime environment for Windows[153]. In light of the expectations of a cooperative relationship, Microsoft's deceptive conduct was opaque. Consequently, countermeasures were hard, if not impossible, to implement, and there was a substantial threat of competitive harm.

In contrast, deceptive conduct in competitive environments is less likely to be actionable under Section 2, because misrepresentations, deceptive practices, or omissions in the context of competitive relationships are less likely to be material. For example, we agree with the reasoning in two recent appellate cases finding that misleading statements in the advertising contexts there at issue were not grist for Section 2 claims[154].

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[152] 253 F. 3d at 76.

[153] *Id.*

[154] *See* Am. Council of Certified Podiatric Physicians & Surgeons v. Am. Bd. of Podiatric Surgery, 323 F.3d 366, 370-72 (6th Cir. 2003) (applying a rebuttable presumption that effect on competition of misleading advertising material was *de minimis*); Am. Prof'l Testing Services v. Harcourt Brace Jovanovich Legal & Prof'l Publ'ns, Inc., 108 F.3d 1147, 1152 (9th Cir. 1997) (same).

Those decisions make sense in the "rough and tumble" of the competitive marketplace because the allegedly misleading hyperbole was transparent to rivals, who generally could protect themselves by engaging in their own counter-advertising. Therefore, there was a relatively low risk that significant anticompetitive effects would occur in that context.

Unlike those advertising cases, the very different circumstances presented here suggest that deceptive conduct could have caused lasting competitive harm by obscuring crucial information, known only to one industry member, until it was too late to counteract the consequences. In this context, we cannot stress too strongly the importance we place on the fact that the challenged conduct occurred in the context of a standard-setting process in which members expected each other to act cooperatively. We recognize that standard setting of the type sponsored by JEDEC potentially yields significant efficiencies[155] – especially when the standards facilitate interoperability among various components, to the likely benefit of industry participants as well as consumers[156]. Although standard setting displaces the normal process of selection through market-based competition – by which, without any agreement, the purchasing decisions of customers determine which interoperable combinations of products and technologies ultimately will survive – the efficiency benefits of consensus standard setting easily can outweigh that loss of competition.

Even under the best of circumstances, however, the standard-setting process has a unique potential to skew the competitive

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[155] *See* Moore v. Boating Indus. Ass'n, 819 F. 2d 693, 695 (7th Cir. 1987); *cf.* United States Dep't of Justice and Federal Trade Comm'n, Antitrust Guidelines for Collaborations Among Competitors (2000) *reprinted in* 4 Trade Reg Rep. (CCH) ¶ 13,160, *available at* http://www.ftc.gov/os/2000/04/ftcdojguidelines.pdf.

[156] *See, e.g.*, Williams, Tr. 763; Calvin, Tr. 994; Polzin, Tr. 3972.

process by aligning supply and demand in a prescribed direction[157]. The risk of competitive harm is heightened in the face of exclusionary conduct that does not constitute competition on the basis of efficiency and that interferes with the cooperative nature of the standard-setting process. Exclusionary conduct such as deception may distort the selection of technologies and evade protections designed by SSOs to constrain the exercise of monopoly power, with substantial and lasting harm to competition[158]. Additionally, unlike misleading statements made in advertising – which can be corrected quickly by a competitor's counter-advertising – there are fewer "quick fixes" available to correct the competitive harm caused by deception in the SSO context, once a standard has been chosen and the industry has become locked in. If exclusionary conduct reduces or destroys the efficiencies to be gained through consensus standard setting, it may cause considerable harm to competition. If the anticompetitive harm exceeds any remaining efficiencies, standard setting is no longer beneficial on balance.

Consequently, courts have scrutinized conduct related to standard setting[159]. For example, the Supreme Court has condemned efforts to bias the standard-setting process by

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[157] *See* Standard Sanitary Mfg. Co. v. United States, 226 U.S. 20, 41 (1912); FTC Bureau of Consumer Protection, Standards and Certification Final Staff Report, at 28, 34 (April 1983); Michael Katz & Carl Shapiro, *Systems Competition and Network Effects*, 8 J. ECON. PERSPECTIVES 93, 105-06 (1994); Richard Gilbert, *Symposium on Compatibility: Incentives and Market Structure*, 40 J. INDUS. ECON. 1 (1992).

[158] *See infra* Sections IV.C.1, IV.C.2, and IV.C.3.c., d.

[159] *See* Allied Tube & Conduit Corp. v. Indian Head, Inc., 486 U.S. 492, 500 (1988) ("Agreement on a product standard, is after all, implicitly an agreement not to manufacture, distribute, or purchase certain types of products. Accordingly, private standard setting associations have traditionally been objects of antitrust scrutiny."); Am. Soc'y of Mech. Engineers, Inc. v. Hydrolevel Corp., 456 U.S. 556, 571 (1982).

"stacking" the decision making body with voters interested in excluding a competing product[160]. The Court also has recognized that the power to distort the interpretation of standards is the "power to frustrate competition in the marketplace."[161] Likewise, prior Commission enforcement efforts have targeted distortions of standard-setting processes that have led to the creation of market power.[162]

Antitrust scrutiny of possibly deceptive conduct in the standard-setting context is especially warranted when the standard-setting body has determined to carry out its work in an environment ostensibly characterized by cooperation, rather than rivalry – in other words, when the circumstances closely resemble those in *Microsoft* (as distinguished from the competitive environment in the Section 2 advertising cases mentioned above). In a consensus-oriented context, participants in the standard-setting process are likely to be less wary of deception; they are less likely to detect and take countermeasures to counteract it, and anticompetitive effects therefore are more likely to result. The magnitude of potential anticompetitive consequences may also be

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[160] *See Allied Tube*, 486 U.S. at 508 ("petitioner was at least partially motivated by the desire to lessen competition and . . . stood to reap substantial economic benefits from making it difficult for respondent to compete"), 511.

[161] *See Am. Soc'y of Mech. Engineers*, 456 U.S. at 571.

[162] *See* Union Oil Co., Dkt. No. 9305, Decision & Order, ___ F.T.C. ___, 2005 WL 2003365 (2005), *available at* http://www.ftc.gov/os/adjpro/d9305/050802do.pdf (consent order resolving allegations that Unocal illegally had acquired monopoly power by misrepresenting to a state standard-setting board that certain research was non-proprietary while pursuing patent claims that would have enabled Unocal to charge royalties for low-emission gasoline compliant with the standard); Dell Computer Corp., 121 F.T.C. 616 (1996) (consent order resolving allegations that, after certifying that it had no relevant patents, Dell sought to enforce patents adopted by a standard-setting organization).

as substantial as it was in *Microsoft*, given the potential for a standard to create market or monopoly power.[163]

We do not hold, and our decision should not be read to mandate, that all SSOs should require disclosure of relevant intellectual property. An SSO may choose not to require such disclosures. If, however, an SSO does require such disclosures, then non-disclosure – followed by adoption of a standard incorporating the intellectual property, and royalty demands against those practicing the standard – may be considered a material omission and may constitute deceptive conduct under Section 5. If an SSO chooses not to require such disclosures, SSO members still are not free to lie or to make affirmatively misleading representations. In either case, whether the SSO requires disclosure should be judged not only by the letter of its rules, but also on how the rules are interpreted by its members, as evidenced by their behavior as well as by their statements of what they understand the rules to be.

c. Nature of the Conduct

In order to assess fully the circumstances under which the alleged deception occurred, we also must understand the nature of the allegedly deceptive course of conduct, which combined the acquisition and exploitation of patents with a cooperative standard-setting process. A patent holder's market power may be materially enhanced once the patented technology is incorporated into a standard, as alternatives become less attractive relative to the chosen technology and less able to constrain its price[164]. For

[163] *See* HOVENKAMP ET AL., II IP AND ANTITRUST, *supra* note 121, at § 35.5b at 35-43 (Supp. 2006) ("the competitive risk is that the misrepresentation [defined to include omissions] will cause a standard-setting organization to adopt a standard it otherwise would have rejected, and that the adoption of that standard will in turn confer on the defendant market power it would not otherwise have obtained.").

[164] *See* Dell Computer Corp., 121 F.T.C. 616, 624 (1996) (Statement of the Federal Trade Commission); McAfee, Tr. 7494-95.

this reason, Rambus's alleged course of conduct, if established, could be especially pernicious to the competitive process.

An SSO may elect to require disclosure of patent positions before standardization decisions are made, because this enables SSO participants to make their choices with more complete knowledge of the consequences – including the potential that those practicing the standard may be liable for patent infringement, unless they negotiate licenses and pay royalties. If the SSO members prefer a given technology, notwithstanding the prospect of royalties, they can vote to incorporate it into the standard. If, in light of likely royalty payments, members prefer an alternative technology, they can vote against inclusion of the patented technology.

Disclosure of potential patent liability also helps avoid the possibility of hold-up by enabling SSO participants to seek protection from excessive royalties "*ex ante*" – *i.e.*, before choosing which technologies to incorporate into the standard. For example, an SSO member expecting to sell products that conform to the standard, who gains knowledge of potential patent exposure, may have powerful economic incentives to negotiate a license *before* the technology becomes standardized, based on the lower, *ex ante* value of the patented technology[165]. Similarly, the

[165] Complaint Counsel's economic expert sets out the basis for this reasoning in greater detail. *See* McAfee, Tr. 7260-75. 7294-7308; *see also* Brief Amicus Curiae of Economics Professors and Scholars at 6-7 (presenting the views of six university economists). Rambus's economic expert, Richard Rapp, has acknowledged that "[s]tandard setting has the potential to create market power and enhance the market value of a technology by reducing the number of close substitutes." Richard T. Rapp & Lauren J. Stiroh, Testimony at FTC/DOJ Hearings Regarding Competition and Intellectual Property Law and Policy in the Knowledge-Based Economy, at 2 (Apr. 18, 2002), *available at* http://www.ftc.gov/opp/intellect/020418rappstiroh.pdf. Rapp continued, "In the absence of knowledge about proprietary IP rights in the technologies under consideration, manufacturers may find themselves the victims of opportunism after the standard has been set." *Id*. at 5. (Rapp's testimony identified a number of conditions that he argued must be met for anticompetitive harm to

owner of the patented technology may prefer to offer an *ex ante* license – even at a lower *ex ante* rate – knowing that the other SSO participants otherwise might engage in a cost/benefit analysis and opt to standardize an entirely different technology. Indeed, under certain circumstances, members of an SSO may even collectively negotiate these types of *ex ante* licenses, without necessarily running afoul of the antitrust laws.[166]

In sum, standard setting can function as an efficient substitute for selecting interoperable technologies through direct competition. Rambus's course of conduct allegedly impaired these processes within JEDEC. Complaint Counsel argue that Rambus deprived other JEDEC members of information needed to make an efficient selection of the "best" technologies for SDRAM standards, based on an analysis of likely costs as well as benefits. Rambus's conduct also purportedly prevented other JEDEC members from avoiding exposure to monopoly pricing by securing commitments regarding future royalty rates at a time when alternative technologies still offered unblunted competition. Under the Policy Statement, these circumstances are relevant to our analysis of whether Rambus's course of conduct constituted deception in violation of Section 5 of the FTC Act. Under Section 2 case law, these circumstances suggest exclusionary conduct: deceptive behavior that hides the price of a patented technology is not "competition on the merits,"[167] and deception that thwarts

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occur. We quote his statements for their agreement with Complaint Counsel's general theory, not as representative of any concession that anticompetitive conduct occurred in this case.)

[166] *See* Chairman Deborah Platt Majoras, Recognizing the Procompetitive Potential of Royalty Discussions in Standard Setting, Remarks Before Standardization and the Law: Developing the Golden Mean for Global Trade (Stanford, Cal., Sept. 23, 2005), *available at* http://www.ftc.gov/speeches/majoras/050923stanford.pdf.

[167] *See, e.g.*, Aspen Skiing Co. v. Aspen Highlands Skiing Corp., 472 U.S. 585, 605 n.32 (1985); Multistate Legal Studies, Inc., v. Harcourt Brace Jovanovich Legal & Prof'l Publ'ns, Inc., 63 F.3d 1540, 1550 (10th Cir. 1995),

informed choice is not competition on the "basis [of] efficiency."[168]

2. Rambus's Course of Conduct

Applying the analytical framework to the facts of this case, we first consider whether Rambus engaged in a course of conduct in its JEDEC activities that included potentially deceptive conduct – *i.e.*, "misrepresentations, omissions, or practices."[169] There is little room for dispute about what Rambus did, because much of the evidence in the record regarding Rambus's conduct came from Rambus's own documents and witnesses.[170]

Based on that evidence, we find that Rambus concealed the patent applications it filed, and the patents it obtained, until JEDEC had adopted its SDRAM and DDR SDRAM standards. Once those standards were adopted, Rambus abused their adoption by suing firms that practiced the standards for patent infringement. Rambus also used information derived from JEDEC meetings to develop a patent portfolio that would cover JEDEC's SDRAM standards – a practice which, although it may not be clearly "deceptive" standing alone, nonetheless facilitates hold-up in a cooperative standard-setting context.

The record reveals the following chronology of events.

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cert. denied, 516 U.S. 1044 (1996); Town of Concord v. Boston Edison Co., 915 F.2d 17, 21 (1st Cir. 1990), *cert. denied*, 499 U.S. 931 (1991).

[168] *See Aspen Skiing*, 472 U.S. at 605 ("If a firm has been 'attempting to exclude rivals on some basis other than efficiency,' it is fair to characterize its behavior as predatory") (footnote omitted), quoting ROBERT H. BORK, THE ANTITRUST PARADOX 138 (1978).

[169] *Policy Statement*, *supra* note 139, at 20,911-12.

[170] Of course, documents destroyed by Rambus might have provided additional details regarding Rambus's activities. *See infra* Section V.

a. The Chronology of Concealment

1991. JEDEC was in the early stages of work on the SDRAM standard[171] when Rambus attended its first JEDEC meeting and joined JEDEC in December 1991[172]. Within a few days of that JEDEC meeting, Rambus's Executive Vice President (EVP), Allen Roberts, called Lester Vincent, Rambus's outside patent counsel, to speak with him about "patent deadlines"; Roberts also informed staff that a Rambus goal for the first quarter of 1992 was "patent filing."[173]

1992. Rambus engineer William Garrett represented Rambus at its first JEDEC meeting as a member in February 1992. Following the meeting, Garrett reported to his supervisors that SDRAMs were inevitable and that SDRAM could be standardized sooner than expected[174]. Shortly afterwards, on March 5, 1992, Rambus responded to the PTO's restriction requirement[175] by

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[171] Fully synchronous DRAM initially was proposed to JEDEC in May 1991. IDF 297. Rambus's patented versions of two of the relevant technologies are included in the SDRAM standard: programmable CAS latency and programmable burst length. Rambus's patented versions of the other two relevant technologies – dual-edge clocking and on-chip PLL/DLL – were included in the next generation of SDRAM, called DDR-SDRAM. All of these technologies were considered for inclusion into the SDRAM standard.

[172] CX 602 at 1-3. Rambus already had met with a number of DRAM manufacturers in an effort to convince them to license RDRAM. *See supra* Section II.A.

[173] CX 1705 at 34.

[174] CX 672 at 1 ("SDRAMs will happen.").

[175] *See supra* note 19 and accompanying text.

filing ten divisional applications, all claiming priority based on the 1990 filing date of the original '898 application.[176]

On March 25, 1992, EVP Roberts and outside counsel Vincent discussed the steps Rambus would need to take to be in a position to accuse manufacturers of JEDEC-compliant SDRAM of infringement[177]. Two days later, Roberts and Richard Crisp (an engineer who served as Rambus's primary JEDEC representative from May 1992 until Rambus withdrew from JEDEC membership)[178] met with Vincent again to discuss Rambus's patent position as a member of JEDEC. Vincent advised both Roberts and Crisp that "there could be [an] equitable estoppel problem if Rambus creates an impression on JEDEC that it would not enforce its patent or patent appln [application]," but that the case would be "less clear cut if Rambus is merely silent."[179]

Early in April 1992, Crisp requested and received from Vincent abstracts of Rambus's current patent applications[180]. In

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[176] The patents that Rambus has asserted against SDRAM and DDR SDRAM manufacturers each derive from continuations of the '898 application or from continuations of one of these divisional applications. *See supra* Section II.A; IDF 171; Nusbaum, Tr. 1511-12.

[177] According to Vincent's notes, Roberts told Vincent with regard to JEDEC that Rambus "need[s] preplanning before accus[ing] others of infringement." CX 1941 at 1.

[178] Crisp, Tr. 2929.

[179] CX 1942. Equitable estoppel is a defense against infringement under patent law. It generally means that, if a patent holder's actions justify a belief that he has no intent to enforce the patent, then he is prevented (*i.e.*, equitably estopped) from enforcing the patent at a later date. *See, e.g.*, Stambler v. Diebold, 11 U.S.P.Q.2D (BNA) 1709 (E.D.N.Y. 1988). Vincent also advised that Rambus would be better able to defend against an equitable estoppel claim if Rambus abstained from voting at JEDEC. CX 1942.

[180] CX 1945 at 1; Crisp, Tr. 3050.

April 1992, Crisp attended a JEDEC task group meeting that focused on SDRAMs. Reporting back to Rambus executives on the meeting's events, Crisp discussed the technologies under consideration, stressed the JEDEC members's concern with price, and concluded that "the group is pretty set on using the SDRAMs."[181]

On May 2, 1992, Roberts met with Vincent to discuss claims that Crisp wanted to add to Rambus's patent applications, including a claim covering programmable latency and, if needed, a claim involving programmable burst length – two technologies eventually incorporated into the SDRAM standard[182]. After attending a JEDEC meeting later that month, Crisp spoke with Vincent to discuss adding claims to the divisional applications[183]. In that same month, Rambus CEO Tate called a meeting with Rambus executives, including Crisp and Roberts, to discuss: (1) how JEDEC SDRAMs might infringe Rambus's patents ("What patents do synchronous DRAMs violate of ours?"); (2) how Rambus might add claims to cover JEDEC standards ("What extensions should we be filing to add claims based on original inventions?"); and (3) the nature of Rambus's disclosure duties to

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[181] CX 1708.

[182] CX 1946; Crisp, Tr. 3057-58. Vincent's notes state "Add claims to mode register to control latency output timing depending upon clock – specify clock cycle" and "check whether original application has

block s . . (?)." The latter is a reference to programmable burst length. *See* Horowitz, Tr. 8661-62 (stating that he uses "variable block size" and "variable burst length" interchangeably); Geilhufe, Tr. 9642-43 ("variable block size" and "programmable burst length" are "[d]ifferent terms describing the exact same function"). Crisp was unable "at this point in time" (*i.e.*, at trial) to remember what the reference – misread to him by trial counsel as "blocks" – dealt with, but he acknowledged that he was "unsure whether we had claims in that area" and that he had "suggested to Mr. Roberts that if we didn't, we should have some claims in those areas, including blocks." Crisp, Tr. 3059.

[183] CX 34 at 1, 59; CX 1947.

JEDEC ("What obligation do we have to advise JEDEC that we have filed but unissued patents that sync do/may infringe?").[184]

In June and July 1992, members of the JC 42.3 subcommittee, including Rambus, voted on whether the SDRAM standard should include a programmable mode register to set CAS latency and burst length[185]. The ballot asked the representative of each voting member whether he or she was aware of any relevant patents[186]. The ballot also asked members voting against the proposal to explain their reasons and asked specifically about any patent issues. IBM, which voted against the proposal, noted that "patent issues need to be cleaned up before we proceed."[187] Rambus omitted to disclose the existence of any pending or issued patents,[188] even though Rambus was working on claims relating to the mode register, programmable latency, and burst length at the time[189]. Rambus voted against the proposal, citing technical reasons (*e.g.*, an inadequate number of power pins).[190]

One week after the June 1992 ballot was circulated, Rambus CEO Tate forwarded to the firm's executives a "specific" business plan that outlined a patent strategy regarding SDRAMs:

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[184] *See* CX 5101 (Tate e-mail, asking questions under the heading "JEDEC").

[185] CX 252a.

[186] *Id.* at 2.

[187] JX 13 at 9.

[188] *Id.*

[189] *See* CX 1946; CX 1947.

[190] Crisp, Tr. 3080; JX 13 at 9.

> [W]e believe that Sync DRAMs [SDRAMs] infringe on some claims in our filed patents, and that there are additional claims we can file for our patents that cover features of Sync DRAMs. Then we will be in position to request patent licensing (fees and royalties) from any manufacturer of Sync DRAMs. Our action plan is to determine the exact claims and file the additional claims by the end of Q3/92. Then to advise Sync DRAM manufacturers in Q4/1992.[191]

In August 1992, Rambus specifically assigned JEDEC representative Crisp responsibility for overseeing development of amended patent claims to "provide better coverage" against SDRAMs[192]. Crisp followed up with outside counsel Vincent regarding the status of the planned amendments[193]. In September 1992, Crisp requested that Vincent file an amendment adding claims relating to "DRAM - multiple open row addresses" and "DRAM - programmable latency via control reg" to Rambus's pending applications[194]. Crisp requested these additional claims to "cause problems with synch DRAM."[195] Crisp agreed to provide Vincent with a copy of the "synch DRAM spec."[196] Crisp and Vincent also discussed adding claims relating to on-chip PLLs on

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[191] CX 543a at 14-17 (Rambus 1992-97 Business Plan, devoting a majority of discussion of competition to SDRAM).

[192] *See* CX 5104 at 1 (Rambus CEO Tate's "Notes from 8/26 Strategy Meeting" stating, "Richard [Crisp] will work to add modifications to our patents to provide better coverage, if possible, for Masters and against Ramlink/Sync DRAMs.").

[193] *See* Crisp, Tr. 3087-88; CX 1930 at 42.

[194] Crisp, Tr. 3097, 3099-3100; CX 1949.

[195] CX 1949 at 1.

[196] *Id*. at 4.

DRAMs, in response to a formal presentation at JEDEC[197]. In November 1992, Crisp met with Vincent to follow up on claim amendments and received copies of Rambus's pending patent applications[198]. A December 1992 Rambus planning document noted intentions to "get a copy of the SDRAM spec and check it for features we need to cover as well as features which violate our patents."[199]

1993. In January 1993, Rambus CEO Tate scheduled an "Objectives meeting" to discuss, among other things, "patents – vs. SDRAM."[200] In February 1993, per Crisp's instructions, Rambus worked on adding claims relating to programmable latency and on-chip PLL/DLL[201]. The following month, the JC 42.3 subcommittee voted to send its proposed SDRAM standard, which included programmable CAS latency and burst length, to the JEDEC Council for approval.[202]

On May 17, 1993, while the proposed SDRAM standard was awaiting final approval by the JEDEC Council, Rambus filed a preliminary amendment to another of its divisional

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[197] *Id*. at 1, 5-7.

[198] CX 682; CX 1930 at 59; CX 1951 at 1.

[199] CX 1821 at 24.

[200] CX 5106.

[201] CX 686; Crisp, Tr. 3121-22 (explaining that Crisp provided Rambus engineer Fred Ware with a list of possible claim amendments including "DRAM with programmable access latency . . . [and] DRAM using PLL/DLL circuit to reduce input buffer skews"). Crisp and Vincent continued to communicate regarding patent application amendments during the following months. *See* CX 1930 at 83; CX 1957.

[202] IDF 351; JX 15 at 14.

applications[203]. Rambus engineer Fred Ware shortly afterwards described the amendment, which involved programmable CAS latency, as "directed against SDRAMs."[204] Crisp agreed.[205]

One week after Rambus filed its amendment, on May 24, 1993, the JEDEC Council formally adopted the SDRAM standard[206]. The SDRAM standard incorporated programmable CAS latency and programmable burst length, two of the technologies that Rambus claims are covered by its patents.[207]

After the SDRAM standard was adopted, the JC 42.3 subcommittee turned to work on the next generation of SDRAM, which became DDR SDRAM[208]. At the same time, Rambus continued to amend its patent applications to cover JEDEC-compliant products. In June 1993, Rambus engineers worked with Vincent to amend Rambus's patent applications with claims specifically directed against SDRAMs or future SDRAMs[209]. On June 18, 1993, an e-mail from Ware to Crisp and others noted that a claim for "DRAM with PLL clock generation" that was "directed against future DRAMs" was "partially written up" and

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[203] CX 1456 at 198-210 (amending Patent Application No. 07/847,651).

[204] CX 1959 (June 18, 1993 Ware e-mail); Crisp Tr. 3153-56. Years later, in preparation for Micron's litigation against Rambus, Ware examined the preliminary amendment and concluded that the scope of the claims was not as broad as he originally had thought. CX 2103 (Ware *Micron* Dep.) at 100 (*in camera*).

[205] CX 703.

[206] IDF 354-356.

[207] IDF 355; JX 56 at 114.

[208] *See, e.g.*, Rhoden, Tr. 460-63, 1200; Williams, Tr. 820; Sussman, Tr. 1402, 1429; G. Kelley, Tr. 2567, 2585-87.

[209] S*ee* CX 1959.

needed to be finished and filed[210]. Crisp responded that this "sounds really good [and] matches what I have requested and what I believe has happened."[211]

1994. Rambus executives continued to correspond and meet with Vincent in early 1994 to "talk about patent strategies."[212] In March 1994 Rambus President David Mooring called for an "IP maximization strategy" to be put in place by the next quarter.[213]

Throughout 1994, Rambus continued to work on amending its applications, focusing on SDRAMs or future SDRAMs such as DDR. In May of that year, Roberts requested that Vincent consider ways to add or strengthen claims covering programmable CAS latency and dual-edged clocking, which subsequently became features of DDR SDRAM[214]. Rambus CEO Tate monitored the progress of Rambus's patent activity and asked for progress reports, particularly regarding the claims "that read directly on current/planned sdrams."[215]

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[210] CX 1959. *Compare* Nusbaum, Tr. 1584 *with* Fliesler Tr. 8867 (disagreeing as to whether claims filed on June 28, 1993 actually covered a subsequent PLL proposal).

[211] CX 703.

[212] CX 718 (e-mail dated January 5, 1994, setting up meeting with Vincent for January 12, 1994)CX 19__.

[213] CX 726 (e-mail dated March 15, 1994). Mooring's e-mail also proposed that Rambus "kick-off another patenting spree focused on the controller side of things" to take advantage of "a window of opportunity left while we still have confidential information . . . ." *Id.*

[214] CX 734.

[215] CX 740 (June 1994 e-mail from Tate to Roberts requesting "a list of which claims we are making that read directly on current/planned sdrams and on what most might be, so i can track progress from lester's [Vincent's] periodic status lists").

In September 1994, JEDEC participants made formal presentations relating to on-chip PLL/DLL technology for later-generation SDRAM (which became known as DDR SDRAM)[216]. Although Crisp knew that Rambus had been pursuing patent claims covering on-chip PLL, he omitted to disclose any patents or patent applications at this meeting[217]. His report to Rambus management on the meeting stated, "Obviously we need to think about our position on this for potential discussion with NEC regarding patent issues here."[218] Crisp e-mailed Roberts that he thought Rambus eventually would bring infringement actions in areas such as "PLL on a DRAM . . . programmable access latencies and host of other areas."[219] In that same month, September 1994, Rambus amended its 08/222,646 application (the '646 application) to add claim 151, relating to dual-edged clocking.[220]

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[216] At the JC 42.3 meeting on September 13-14, 1994, NEC made a presentation that proposed "putting a PLL on board their SDRAMs to improve the output delay." CX 711 at 36. This presentation led Crisp to conclude that "others are seriously planning inclusion of PLLs on board SDRAMs." *Id*. at 37.

[217] Crisp, Tr. 3316.

[218] CX 711 at 36.

[219] CX 757 at 1. A few weeks later, another Crisp e-mail to Rambus executives described on-chip PLL as "one of our key technology patents" and emphasized, "If it is allowed, we need to be able to collect on it." CX 763. *See also* CX 766 (October 1994 Crisp e-mail suggesting a strategy for encouraging "the SDRAM boys" to make use of on-chip PLLs so that Rambus could then sue them for infringement).

[220] CX 1493 at 183-85. *Compare* Nusbaum, Tr. 1597-98 *with* Fliesler, Tr. 8858 (both observing that claim 151 involved receiving data in response to both the rising and falling edges of a clock signal but disagreeing as to further implications). Roberts previously had circulated to Rambus executives drafts of the claim amendments, which Roberts described as "[Lester Vincent's] attempt to work the claims for the MOST/SDRAM defense." CX 746 at 1.

1995. In April 1995, Rambus CEO Tate reiterated objectives of "get[ting] royalties from competitive memory" that used just one or a few of Rambus's technologies; called for verification that "all ideas we have requested to be filed as general patents re [SDRAM] have been [filed]"; and directed that Rambus "hold on patent issuances till then."[221] In May 1995, Crisp recommended that Rambus continue to keep its patent position secret, explaining that "it makes no sense to alert them [JEDEC] to a potential problem they can easily work around."[222] Through the summer, Crisp participated in work "on enhancing claim coverage."[223] In October 1995, Rambus amended one of its patent applications to insert claims relating to on-chip PLL/DLL technology[224]. One week after filing these amendments, Rambus received a JC 42.3 survey ballot on "Future Synchronous DRAM Features." The ballot asked whether members believed that "on chip PLL or DLL is important to reduce the access time from the clock for future generations of SDRAMs," and whether "future generations of SDRAMs could benefit from using BOTH edges of the clock for sampling inputs."[225] Rambus did not vote, and it failed to disclose the existence of any application that related to either on-chip PLL/DLL or dual-edge clocking[226]. At the meeting at which the ballot results were discussed, JEDEC member MOSAID disclosed that it had applied for a patent applicable to PLLs/DLLs; Crisp acknowledged that "even after seeing this disclosure of a patent

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[221] CX 5110 at 2-3.

[222] CX 711 at 73.

[223] CX 5112.

[224] IDF 963; CX 1502 at 233-39.

[225] CX 260 at 12 (emphasis original); JX 28 at 45.

[226] Crisp, Tr. 3341; JX 28 at 45 (listing firms that provided responses).

application," he "did not say anything with respect to any Rambus patent application concerning PLLs or DLLs."[227]

Crisp advised management in September 1995 that Rambus should "redouble [its] efforts to get the necessary amendments completed, the new claims added and make damn sure this ship is watertight before we get too far out to sea."[228] In fall 1995, Rambus's new in-house counsel, Anthony Diepenbrock, outlined Rambus's patent strategy at a company-wide retreat[229]. Diepenbrock's presentation described Rambus's "offensive" patent strategy as "find[ing] key areas of innovation in our IP that are essential to creating a competing device" and "claim[ing] these areas as broadly as possible within the scope of what we invented."[230] The first two examples cited in Diepenbrock's presentation were DLLs and dual-edge clocking.[231]

Meanwhile, Diepenbrock advised Crisp – just as Vincent had in 1992 – that Rambus faced a risk of equitable estoppel based on its participation in JEDEC[232]. Diepenbrock urged that Rambus withdraw from JEDEC[233]. At his next JEDEC meeting, in December 1995, Crisp made private inquiries regarding JEDEC's

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[227] Crisp, Tr. 3341-44. Crisp promptly reported MOSAID's disclosure to Rambus management. *See* CX 711 at 192.

[228] CX 837 at 2.

[229] Diepenbrock, Tr. 6129-30.

[230] CX 1267; Diepenbrock, Tr. 6131.

[231] CX 1267; Diepenbrock, Tr. 6132-33.

[232] Crisp, Tr. 3442.

[233] *Id*. at 3442-43.

patent policy[234]. Based on these discussions, as summarized in an e-mail to Rambus executives, Crisp stated that it was unacceptable "to not speak up when we know that there is a patent issue, to intentionally propose something as a standard and quietly have a patent in our back pocket we are keeping secret that is required to implement the standard and then stick it to them later (as WANG and SEEQ did)."[235]

Later that month, Vincent sent Diepenbrock "materials relating to the proposed [FTC] consent order involving Dell computer," which resolved allegations of unfair methods of competition based on Dell's assertion of patent rights after its representative had certified to an SSO that a standard under consideration did not infringe any Dell patents[236]. Vincent's notes from the period conclude that there should be "no further participation in any standards body . . . do not even get close!!"[237]

1996. On January 11, 1996, Vincent met with Rambus executives – including Tate, Crisp, and Diepenbrock – to discuss *Dell* and other matters[238]. Rambus attended no JEDEC meetings after this date[239]. According to Crisp, Rambus was concerned that

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[234] *Id*. at 3440-44, 3447-48; CX 711 at 188 (Crisp e-mail describing conversations with Sanyo's Howard Sussman and VLSI Technology's Desi Rhoden). Crisp testified that he sought this information because Rambus was considering making a presentation regarding a proposed technology. Crisp, Tr. 3440-41, 3447-48.

[235] CX 711 at 188. Crisp's e-mail adds, "I am unaware of us doing any of this or of any plans to do this." *Id*.

[236] CX 1990. *See* Dell Computer Corp., 121 F.T.C. 616 (1996).

[237] CX 1928 (emphasis original).

[238] CX 3126 (Vincent *Infineon* Dep.) at 536-38 (*in camera*).

[239] Rambus Answer, ¶ 41.

attendance at future meetings could leave Rambus in a vulnerable position in future litigation.[240]

During this period, however, Rambus continued to build its patent portfolio. On October 6, 1995, the PTO had sent Rambus's attorney a notice of allowability on the '646 application, which had claims relating to dual-edged clocking[241]. According to Diepenbrock, this meant that "the patent office has reason to believe or believes that the claims should go to issuance."[242] Rambus paid the issuance fee on January 5, 1996, and the ensuing patent, No. 5,513, 327 ("the '327 patent") issued on April 30, 1996[243]. Issuance of this patent was a noteworthy event within Rambus[244].

On June 17, 1996, Rambus sent a letter to JEDEC, signed by Crisp, stating that Rambus was not renewing its membership[245]. Rambus enclosed "a list of Rambus U.S. and foreign patents" and stated that "Rambus has also applied for a number of additional patents in order to protect Rambus technology."[246] The letter emphasized that "Rambus reserves all rights regarding its intellectual property."[247] Rambus omitted from the list that it provided to JEDEC the only then-issued patent that Rambus

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[240] CX 858 at 2 ("the current plan is to go to no more JEDEC meetings due to fear that we have exposure in some possible future litigation"); Crisp, Tr. 3358.

[241] CX 1482; Diepenbrock, Tr. 6190. *See supra* note 220.

[242] Diepenbrock, Tr. 6151.

[243] *Id*. at 6185, 6192; CX 1494.

[244] Diepenbrock, Tr. 6194.

[245] CX 887.

[246] *Id*.

[247] *Id*.

believed covered technology under consideration by JEDEC – the '327 patent.[248]

Rambus's June 1996 withdrawal letter also omitted information that would have allowed JEDEC members to adopt standards that would avoid infringing Rambus's intellectual property. While the letter mentioned inconsistency between JEDEC and Rambus with respect to the "terms" of licensing, and purported to reserve Rambus's rights respecting its intellectual property, Rambus omitted to disclose that it had used information gleaned during JEDEC meetings to develop a patent portfolio covering JEDEC's SDRAM and DDR SDRAM standards, and also omitted to disclose the patent applications Rambus had filed to implement its strategy. To the contrary, the letter stated, "To the extent that anyone is interested in the patents of Rambus, I have enclosed a list of Rambus U.S. and foreign patents."[249] Rambus's list identified *only* patents unrelated to JEDEC's work[250]. Rambus's letter stated that Rambus had applied for "a number of additional patents" but the letter did not suggest that future patents would be any more applicable to JEDEC's DRAM standards than were the issued patents on the list.

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[248] *See* CX 5013 (designated R401208-09) (Joel Karp presentation regarding "Enforcement Scenario for 1999," stating, " '327 – covers DDR (dual-edged clocking)"). (The "R" designation refers to Bates stamp numbers that appear on this and other exhibits admitted into this record from the *Infineon* litigation.)

[249] CX 887.

[250] Although some of the listed patents derived from the '898 application, none of them applied to JEDEC's SDRAM and DDR SDRAM work, Jacob Tr. 5365-66, 5501-02, and none was named in Rambus's infringement complaints or counterclaims against DRAM manufacturers. *Compare* CX 887 at 2 (Rambus's list of issued patents) *with* CX 1855 (complaint against Hitachi), CX 1867 (complaint against Infineon), CX 1878 at 13-14 (counterclaims against Hyundai), CX 1891 at 2 (claims asserted against Hyundai/Hynix), *and* CX 1880 at 29-38 (counterclaims against Micron).

1997 and subsequent years[251]. Although Rambus terminated its JEDEC membership in 1996, Rambus continued to receive information on the activities of JEDEC after 1996. Beginning in 1997, Crisp received information from a source that he referred to as "deep throat."[252] Crisp also received information from three other unsolicited sources known as "Mixmaster," a reporter called "Carroll Contact," and "secret squirrel."[253] According to Crisp, these sources provided information on the features of devices being proposed for standardization[254]. Crisp shared the information he obtained from these inside sources with Rambus's executives and engineers,[255] and this information was used in the

[251] By including herein a discussion of Rambus's post-resignation conduct, we do not mean to suggest that a firm that never participated in a standard-setting process – or that did so without deception, then resigned from the SSO – would be at risk of Section 2 liability if it monitored the standard-setting process from the outside and developed a patent portfolio covering standards it believed would be adopted. Rambus's post-resignation conduct was quite different. It represented the continuation, albeit in a different form, of a deceptive course of conduct that began more than four years before Rambus formally "resigned" from JEDEC. Rambus's "resignation" did nothing to cure its prior course of conduct. If anything, the resignation operated to conceal further Rambus's course of conduct, because Rambus's resignation letter left the impression that Rambus had disclosed what was relevant when, in fact Rambus had done nothing of the sort. Under these circumstances, treating Rambus's post-resignation conduct as benign could invite further abuses of standard-setting processes that otherwise might be procompetitive.

[252] CX 929; CX 932.

[253] IDF 280-81; Crisp Tr. 3412-18.

[254] Crisp Tr. 3417.

[255] CX 935 at 1; CX 929 at 1; CX 973 at 1; CX 979 at 1; CX 1014 at 1.

continuing process of filing and amending Rambus's patent applications.[256]

Additionally, although no longer a JEDEC member, Rambus continued to conceal its relevant patent applications. Rambus CEO Tate, for example, stated in a February 1997 e-mail to Rambus executives, "do *NOT* tell customers/partners that we feel DDR may infringe – our leverage is better to wait."[257] Likewise, a July 1997 e-mail by Rambus Chairman of the Board Bill Davidow stated that "[o]ne of the things we have avoided discussing with our partners is intellectual property problem [infringement by SyncLink and SDRAM/DDR SDRAM] . . . . We are hoping that they will either drop their competitive efforts or discover for themselves that they have violated Rambus patents and will conclude that getting around them will be either extremely difficult or impossible and will take a lot of time."[258] And in its October 1998 "strategy update," Rambus stated, "We should not assert patents against Direct partners until ramp reaches a point of no return."[259] In sum, after leaving JEDEC, Rambus strategically maintained its silence, thereby prolonging the misimpression created by its prior conduct.

By March 1998, a DDR SDRAM standard incorporating all four of the technologies that Rambus claims are covered by its patents had been approved by the JC 42.3 committee[260]. The

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[256] Crisp Tr. 3418. *See generally* CX 5115 (November 1996 Tate e-mail announcing plans for an "IP strategy" panel to discuss Rambus efforts to use intellectual property "in process" to "block . . . SDRAM-2 . . . .").

[257] CX 919.

[258] CX 938 at 1.

[259] CX 5011 at 3 (designated R401155).

[260] IDF 380; JX 40 at 7-8; CX 375.

JEDEC Council approved that standard, and it was published as a JEDEC standard in August 1999[261]. By November 1999, Rambus had obtained all four patents cited in its first complaint against JEDEC-compliant uses (filed against Hitachi) in January 2000.[262]

b. Rambus's "Notice" to JEDEC

Rambus claims that it twice gave notice to JEDEC of its patents and patent applications through responses to questions. Based on our review of the evidence regarding those incidents, we find that, far from giving notice, Rambus's responses were evasive and, indeed, misleading.

The first incident, in May 1992, was an outgrowth of concerns held by IBM and Siemens regarding possible Rambus patents on dual-bank designs. In the course of a discussion of that technology at a JEDEC meeting, some of the participants noted the possibility that Rambus and Motorola might have patents on multi-bank designs (a technology that is not at issue here)[263]. Motorola's representative promised to check and to get back to JEDEC with

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[261] IDF 381; CX 234.

[262] CX 1855. Rambus followed this initial suit with a complaint against Infineon, filed in August 2000, CX 1867, and with counterclaims against Hyundai/Hynix, CX 1878, and Micron, CX 1880, filed in February 2001, all alleging infringement based on JEDEC-compliant uses. Rambus quickly induced other industry members to enter licenses covering production of JEDEC-compliant products. *See* CX 1391a at 8 (November 2000 Tate "Big Picture Update," stating that more than 40% of the "SDRAM/DDR market" had already accepted Rambus licenses); CX 1154 (November 2000 Tate e-mail noting that SDRAM/DDR SDRAM and RDRAM licenses already gave Rambus royalties from close to half of the entire DRAM market); **[REDACTED]**

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[263] *See* RX 297 at 4-5; CX 2089 at 133 (Meyer *Infineon* Trial Tr.) (*in camera*).

an answer[264]. Expressing concern that Rambus might have a patent on multi-bank designs, and noticing that Rambus had stayed silent, Siemens's Meyer asked the DRAM task group chairman, Gordon Kelley of IBM, to pose a direct question to Rambus[265]. Kelley asked whether Rambus wanted to comment[266]. Rambus's representative, Crisp, shook his head "no."[267] Crisp did not explain whether that gesture meant that Rambus lacked such a patent, whether he did not know the answer to the question posed, or something else. He did *not* say that the gesture meant that Rambus would not disclose relevant patents or patent applications, and the record shows that those present did not read that into his gesture.[268]

The second incident relates to a May 1995 JEDEC subcommittee discussion of the SyncLink memory technology.

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[264] *See* CX 2089 at 133 (Meyer *Infineon* Trial Tr.) (*in camera*).

[265] *See* CX 673; CX 2089 at 133, 164 (Meyer *Infineon* Trial Tr.) (*in camera*).

[266] *See* Crisp, Tr. 3066 (Kelley "asked me if I cared to comment and I declined to comment"); CX 673 (Crisp e-mail stating, "Gordon Kell[e]y of IBM asked me if we would comment which I declined."); CX 2089 at 136 (Meyer *Infineon* Trial Tr.) (*in camera*) (Kelley formulated the question as, "Do you want to give a comment on this"). *But cf.* G. Kelley, Tr. 2543 (unable to recall whether he had said anything to Rambus and suggesting that it was Meyer who asked Rambus whether it had patentable material).

[267] *See* CX 673; CX 2089 at 135-37 (Meyer *Infineon* Trial Tr.) (*in camera*) ("he just shook his head"); Calvin, Tr. 1068-70 (Crisp responded in the negative); RX 290 at 3 ("NO RAMBUS COMMENTS"); RX 297 at 5 ("No comments given").

[268] Intel's Calvin testified that the incident gave him no concern. Calvin, Tr. 1070-71. Meyer and Kelley ultimately concluded that Rambus had no relevant patents. CX 2089 at 151-52 (Meyer *Infineon* Trial Tr.) (*in camera*); G. Kelley, Tr. 2545-46, 2562. Only IBM's Kellogg termed the lack of response by Rambus a concern, Kellogg, Tr. 5323, but he also testified that the May 1992 meeting did not cause him to understand that Rambus had intellectual property applicable to SDRAM. *Id*. at 5056.

This is not a technology at issue here[269]. A number of companies were asked whether they had relevant patents. Intel's Sam Calvin asked whether Rambus had patents relevant to SyncLink, and then DRAM task group chairman, IBM's Gordon Kelley, addressed to Crisp a request that Rambus provide a statement as to whether Rambus had patents that covered SyncLink.[270]

At the next JEDEC subcommittee meeting on September 11, 1995, Rambus furnished a written response that focused on its patents and patent applications relevant to SyncLink alone[271]. Indeed, except for the concluding sentence, the entire statement referred exclusively to SyncLink. The record shows that the JEDEC meeting attendees interpreted the statement as relating to SyncLink only and therefore of no moment[272]. Moreover, Rambus

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[269] Crisp agreed that "the SyncLink proposal was similar to the Rambus architecture in a number of places." Crisp, Tr. 3254-55. SyncLink, like RDRAM but unlike SDRAM and DDR SDRAM, involved a narrow-bus technology, using multiplexing and packetization for command and address information. *See, e.g.*, Becker, Tr. 1203-04; Sussman, Tr. 1405 (SyncLink a "totally different architecture" from SDRAM and DDR SDRAM); G. Kelley, Tr. 2573; Crisp, Tr. 3254 (SyncLink packetized); CX 1069 (same); Kellogg, Tr. 5090-91 and 5095 (SyncLink involved a narrow bus and packetization; it had some similarities to RDRAM); Tabrizi, Tr. 9119. RamLink, from which SyncLink evolved, used a narrow-bus, packetized, and fully multiplexed architecture, as did RDRAM. *See id*. at 9116-17, 9119; *see generally* RX 555 at 5 (April 1995 Crisp letter noting that RamLink and RDRAM "work in a very similar manner").

[270] *See* CX 711 at 73 (Crisp's meeting report, indicating that "Kelley asked to have us state whether or not Rambus knows of any patents especially ones we have that may read on Synchlink"); Crisp, Tr. 3266-67 (agreeing that Kelley asked for a report as to whether "Rambus knows of any patents that may read on SyncLink"); G. Kelley, Tr. 2578. JEDEC minutes of the meeting provide no specifics. *See* JX 26 at 10 (stating only, "Patent issues were a concern in this proposal.").

[271] *See* JX 27 at 26.

[272] *See* Sussman, Tr. 1411-13; Kellogg, Tr. 5093-96. Indeed, JEDEC's minutes described the discussion entirely in terms of SyncLink and its

took additional steps to deflect attention from the potential breadth of the statement's final sentence[273]. After Kelley commented that Rambus had not said anything, Crisp re-framed the final sentence in terms of SyncLink: "I reminded them . . . that our silence was not an agreement that we have no IP *related to SycLink* (sic). . . ."[274] In addition, Crisp reminded the members

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predecessor, RamLink. *See* JX 27 at 4 ("SyncLink/ RamLink patents were discussed. Rambus noted at the general meeting their position (see [the message presented by Crisp]).").

Between April and August 1995, Crisp told several people that SyncLink and RamLink likely violated Rambus's patents. *See* RX 555 at 5 (statement to Hyundai regarding RamLink); CX 711 at 73 (statement to Intel representatives regarding SyncLink), 80 and 90-91 (statement to JEDEC consultant regarding RamLink, forwarded by recipient to IBM and Hewlett Packard (HP) JEDEC participants, among others), 104-05 (statement to HP JEDEC participant regarding RamLink and SyncLink); RX 592 at 2 (August 1995 statement to SyncLink Consortium regarding RamLink and SyncLink). Although the ALJ treated Crisp's SyncLink/RamLink disclosures as giving notice regarding JEDEC standards, ID at 280-81, the record shows only that the disclosures raised concerns regarding SyncLink. For example, on June 12, 1995 – two days after receiving a copy of Crisp's statement regarding Rambus patents covering RamLink, CX 711 at 90 – IBM's Gordon Kelley called for an IBM review of possible Rambus patents on SyncLink. RX 575 at 6-7.

In this context, Rambus's September 1995 message sounded no alarm. As Crisp phrased it, subcommittee chairman Kelley's reaction was that "he heard a lot of words, but did not hear anything said." CX 711 at 166. Similarly, Motorola's meeting report termed the Rambus letter a "non-statement statement." RX 615 at 1. Crisp even encouraged the reaction that Rambus was revealing nothing new. *See* RX 576 at 2 (June 1995 Crisp e-mail to an HP JEDEC participant, noting that Crisp already had shared his personal opinion that Rambus patents would cover SyncLink and RamLink, and that in September Rambus would provide an "official" response to JEDEC's request "to report on our patent coverage relative to SyncLink").

[273] Rambus's statement ends, "Our presence or silence at committee meetings does not constitute an endorsement of any proposal under the committee's consideration nor does it make any statement regarding potential infringement of Rambus intellectual property." JX 27 at 26.

[274] CX 711 at 167 (emphasis added).

that Rambus previously had reported a patent to JEDEC, suggesting that this placed Rambus in the category of JEDEC members who had disclosed patents.[275]

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The record demonstrates that Rambus's course of conduct included two species of potentially deceptive conduct set forth in the Policy Statement:

- Rambus made potentially deceptive omissions via its continuing concealment of its patents and patent applications until after the DDR SDRAM standard was in place; and

- Rambus made outright misrepresentations when it gave evasive and misleading responses to questions about its conduct.

In addition, Rambus used information gained through its participation in JEDEC to help shape a patent-filing strategy that included filing patent applications covering key parts of the SDRAM and DDR SDRAM standards.

This course of conduct was intentionally pursued, in accordance with a strategy that was spelled out in Rambus's own internal documents and e-mails. We conclude that Rambus's course of conduct had the potential to be deceptive and, under the circumstances of this case, exclusionary.

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[275] CX 711 at 167; Crisp, Tr. 3312-13. During its membership, Rambus disclosed no patent applications and only one issued patent to JEDEC, U.S. Patent No 5,243,703 ("the '703 patent"), which Rambus disclosed in September 1993. Crisp, Tr. 3173, 3176; CX 1801 at 3; Parties' First Set of Stipulations, Item 11. None of the claims of the '703 patent covered SDRAM or DDR SDRAM. *See* Parties' First Set of Stipulations, Item 10 (stating that as of January 1996 Rambus held no issued U.S. patents essential for compliance with any JEDEC standard); Crisp, Tr. 3173-74; Jacob, Tr. 5498-99.

3. The JEDEC Environment

Next, we consider the standard-setting environment at JEDEC. The ALJ focused on whether JEDEC's rules imposed on JEDEC members an affirmative duty to disclose their patents and patent applications. Finding that the rules did not expressly contain such a requirement, the ALJ concluded that Rambus had no duty to disclose its patent filings and, therefore, that Rambus had not engaged in any wrongful conduct[276]**.** We respectfully find that this analysis and conclusion were erroneous. The Complaint in this case alleged not just a breach of a duty to disclose under JEDEC rules, but a course of conduct that was materially deceptive under *all* of the circumstances in which the standard setting occurred.[277]

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[276] *See* IDF 766-85, 902, 939-82; ID at 260-79.

[277] We recognize that the Federal Circuit in *Infineon* found Rambus not liable, ruling that Rambus had not breached a duty to disclose. However, the case before the Federal Circuit in *Infineon* was very different from the case here. In particular, the claim before the Federal Circuit was a state law fraud claim. Rambus, Inc. v. Infineon Tech. AG, 318 F.3d 1081, 1084, 1087 (Fed. Cir. 2003). In contrast, this case involves a federal antitrust claim alleging exclusionary, deceptive conduct. *See* FTC v. Freecom Commc'ns., Inc., 401 F.3d 1192, 1203 n.7 (10th Cir. 2005) ("A § 5 claim simply is not a claim of fraud as that term is commonly understood . . . ."). The standards of proof for these claims are different. To prove a fraud case in Virginia, the plaintiff had to meet a clear and convincing evidence standard. *Id* at 1096. Here, Complaint Counsel must satisfy a lower preponderance of the evidence burden. *See supra* Section III.

Not only are the claims and evidentiary standards different, but so are the records. We take note that the joint appendix that presented the evidentiary record on which the Federal Circuit relied contained the testimony of only *two* industry witnesses (other than witnesses from Rambus and Infineon and the parties' experts) – AMI-2's Desi Rhoden (previously employed by HP and then by VLSI) and IBM's Gordon Kelley. In contrast, the record in this proceeding, from which we have assessed the industry's understandings and expectations, contains testimony from approximately 30 non-Rambus, industry witnesses. Our record includes testimony from five DRAM manufacturers and from major DRAM customers and developers of systems and complementary components,

In order to determine whether Rambus's course of conduct actually was deceptive, we need to consider the totality of the circumstances in which that conduct occurred. For the reasons discussed below, we find that JEDEC's policies (including the policies of its parent, EIA) and practices, considered as a whole, gave JEDEC's members reason to believe the standard-setting process would be cooperative and free from deceptive conduct. In that environment, we find that Rambus's course of conduct was likely to be "material" because it was likely to infect the decisions of JEDEC members with respect to the SDRAM standards to be adopted.

a. EIA/JEDEC Policies and their Dissemination

The record shows that although EIA/JEDEC policies are not a model of clarity, a duty of good faith underlies the standard-setting process under those policies. Specifically, under the EIA/JEDEC rules, "[a]ll EIA standardization programs . . . shall be carried on in good faith under policies and procedures which will assure fairness and unrestricted participation . . . ."[278] Another general EIA regulation provides that EIA standardization programs "shall not be proposed or indirectly result in . . . restricting competition, giving a competitive advantage to any manufacturer, excluding competitors from the market . . . except where required to meet one or more of the" enumerated "legitimate public interest" objectives[279].

To accomplish that EIA goal, as the majority opinion in *Rambus v. Infineon Technologies A.G.* declared,[280] JEDEC's

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such as Sun, Compaq, Cray, Cisco, Intel, AMD, ATI, nVIDEA, Texas Instruments, and Sanyo, in addition to multiple witnesses from HP and IBM.

[278] CX 204 at 5.

[279] *Id.*

[280] 318 F. 3d 1081, 1098 (Fed. Cir. 2003).

Manual of Organization and Procedure (the JEDEC manual) expressly obligated the subcommittee chairperson to remind members to inform the meeting of any patents or applications "that might be involved in the work" being undertaken[281]. EIA General Counsel/JEDEC legal counsel John Kelly testified that JEDEC's rules required disclosure of patents and patent applications[282]. For most of the time that Rambus was a member

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[281] CX 208 at 19 (JEP21-I, JEDEC Manual of Organization and Procedure) (Oct. 1993). Although Rambus and the ALJ question whether this manual was officially adopted, *see* RB at 15-16, IDF 627-28, the record does not support that speculation. *See* CX 205 at 15 (establishing procedure for amending predecessor manual 21-H); CX 54 at 7, G. Kelley, Tr. 2428, and J. Kelly, Tr. 1925 (together establishing that the specified steps occurred). For present purposes, however, the important point is that manual JEP21-I was operative – it shaped JEDEC members' expectations. Numerous JEDEC members understood that the JEP21-I manual set out JEDEC's disclosure policies. *See, e.g.*, Rhoden, Tr. 311-13; Sussman, Tr. 1349; Landgraf, Tr. 1702-04; G. Kelley, Tr. 2408-09. Indeed, when Crisp requested a copy of JEDEC's patent policies in 1995, JEDEC sent him JEP21-I. CX 2104 at 215–16 (deposition transcript at 851-52) (Crisp *Micron* Dep.) (*in camera*).

[282] *See* J. Kelly, Tr. 1903-04 (disclosure "not optional"), 1925-27 (a "requirement to disclose"), 1870 (EIA Publication EP-3 means that participants need to disclose known patents and patent applications), 1894 (Kelly always understood "patent" to include applications), 1897 (coverage of applications was necessary to make the protections effective), 1931-33 (JEP21-I was an effort "to make it abundantly clear" and "to be emphatic, to pound the table" after WANG had argued that JEDEC patent policy did not reach applications), 1935-36 ("patentable" in sign-in sheets refers to applications). John Kelly served as General Counsel of EIA and legal counsel for JEDEC from September 1990 through the time of the Commission's trial. *Id*. at 1750, 1754. He also became President of JEDEC in early 2000. *Id*. at 1751. Kelly was responsible for providing "legal guidance relating to standardization activities," including dealing with questions regarding "the patent policy of EIA and JEDEC." *Id*. at 1813-14. He testified that he had the "last word" within EIA on how rules were to be interpreted and applied and the "final word" in interpreting and applying JEDEC's separate rules. J. Kelly, Tr. 1822, 1915. Others supported Kelly's descriptions. *See* Rhoden, Tr. 313-14, 345; Sussman, Tr. 1348-49 (people with questions regarding patent policy were referred to Kelly); Grossmeier, Tr. 10957 (same); CX 208 at 18 (JEDEC manual stating, "EIA Legal Counsel can advise the Council and committees from time to time

of JEDEC, the JC 42.3 sub-committee chairman was James Townsend. Townsend created and delivered presentations designed to advise members of JEDEC's patent policy at each JC 42.3 subcommittee meeting, as well as at other JC 42 subcommittee meetings[283]. He also delivered this presentation to new members during their orientation[284].

Furthermore, JEDEC's policies expressly required those disclosing relevant patents or patent applications to supply full technical information and to provide RAND assurances (*i.e.*, that royalties on patents covering any standard would be reasonable and non-discriminatory) before their patents were incorporated into JEDEC standards. As presented in Appendix E to the JEDEC manual, "Standards that call for use of a patented item or process may not be considered by a JEDEC committee unless all of the relevant technical information covered by the patent or pending patent is known to the committee, subcommittee, or working group," and the patent holder submits written assurance that it will license without charge or under "reasonable terms and conditions that are demonstrably free of any unfair discrimination."[285]

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concerning interpretation of legal guides."); CX 306 (EIA/JEDEC Meeting Attendance Roster, referencing EIA patent policy and stating, "Consult the EIA General Counsel about any doubtful question.").

[283] *See, e.g.*, Rhoden, Tr. 324-25, 330; Williams, Tr. 771, 785; Calvin, Tr. 1007-08; Landgraf, Tr. 1694-95; CX 42 at 3. The JC 42 committee and its subcommittees met four to eight times per year, and these meetings lasted several days. Rhoden, Tr. 340. The subcommittee meetings were staggered, permitting Townsend to make his patent presentation at multiple subcommittee meetings. If a JEDEC member participated in more than one subcommittee, the member would hear Townsend's patent presentation multiple times. *Id*. at 338-42.

[284] Rhoden, Tr. 337-42.

[285] CX 208 at 27; *see also* J. Kelly, Tr. 1885-86; CX 208 at 19 (noting that "the word 'patented' also includes items and processes for which a patent has been applied and may be pending"); CX 203a at 11 (EIA Engineering

b. Rambus's Understanding of JEDEC's Policies

Following the lead of the Federal Circuit's *Infineon* opinion, we look to the behavior, understandings, and expectations of JEDEC members, including Rambus, to inform our understanding of the JEDEC environment[286]. Rambus's own documents and witnesses indicate that the company believed it should have disclosed its patent filings. For example, Rambus's JEDEC representative, Crisp, understood that "[t]he job of JEDEC is to create standards which steer clear of patents which must be used to be in compliance with the standard whenever possible."[287] Rambus was aware of JEDEC's disclosure policy through written manuals and oral presentations[288]. Crisp understood that disclosure of patents was mandatory,[289] and as early as December 1992, he acknowledged that he understood that patent applications

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Publication EP-3-F) (1981); CX 207a at 8 (EIA Engineering Publication EP-7-A) (1990); JX 55 at 28 (EIA Engineering Publication EP-7-B) (1995).

[286] *See* Rambus, Inc. v. Infineon Techs. AG, 318 F.3d 1081, 1098 (Fed. Cir. 2003).

[287] CX 903 at 2; Crisp, Tr. 2941-42.

[288] Crisp attended a JEDEC meeting at which revisions subsequently incorporated into the JEDEC manual – including specific references to pending patents and to the participants' obligation to disclose – were presented. *See* JX 14 at 1, 3, 25 (minutes of JC 42.3 meeting, December 9-10, 1992, providing text with proposed changes underlined); Rhoden, Tr. 312; G. Kelley, Tr. 2418.

[289] Crisp, Tr. 3477-78 (stating that "[n]on-presenters were obligated to disclose any known patents they had at the time of the committee letter ballot if those patents were required to – were required by the standard" and that presenters were required to disclose patents and applications earlier); *see also* CX 868 (February 1996 Crisp e-mail stating, with reference to a presentation to JEDEC by Micron, "I think we should have a long hard look at our IP and if there is a problem, I believe we should tell JEDEC there is a problem.").

had to be disclosed under JEDEC's policies at least "in some circumstances."[290]

c. Other JEDEC Participants' Understanding of JEDEC's Policy Objectives

Other witnesses besides Crisp testified that JEDEC had determined that prompt disclosure of relevant intellectual property was important for its standard-setting process to work[291]. Absent such disclosure, JEDEC members would face the possibility of patent hold-up. A member possessing relevant intellectual property could stay silent while JEDEC adopted a standard. Then, after a standard had been adopted and it had become expensive to switch to what initially were good alternatives, the patentee could assert its patent and "hold up" the industry by charging higher royalties than could have been extracted before the standard was set. Witnesses testified that early disclosure of intellectual property helped to identify potential hold-up situations while there still was time to avoid the problem.[292]

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[290] Crisp, Tr. 2978, 2982, 3477-78. *See also* CX 5105 (December 1992 Crisp e-mail stating "I know that JEDEC takes the position that we should disclose," but commenting, "Of course, we believe that we do not want to do this [disclose patent applications] yet.").

[291] *See, e.g.*, Rhoden, Tr. 536 (describing a "fundamental premise inside JEDEC" that standards that are developed are "either free of intellectual property or at least all intellectual property is known at the time of creation of the standard"); Calvin, Tr. 1002 ("you at least needed to understand the [e]ffect of patents upon things that you were standardizing"); Landgraf, Tr. 1694 ("the purpose of the policy is to disclose and make sure that standards do not have any conflicts down the road with their potential use").

[292] *See* Landgraf, Tr. 1694 ("The worst thing to have is a standard and products made according to that standard and then later you find an infringement . . ."); J. Kelly, Tr. 1908 ("It's essential to know what impediments there are to the process, what issues there are going forward, and to know when it's necessary to obtain the written assurances."). Even if the standard later could, in theory, be revised to avoid patent issues, that would entail added cost and potentially crippling delay. *See* Rhoden, Tr. 299-300

For example, EIA General Counsel/JEDEC legal counsel John Kelly testified that JEDEC sought to prevent members with patents covering JEDEC standards from exercising "unbridled discretion to license that IP on any terms and conditions that they elect."[293] He explained:

> Having the technology included in the standard is a privilege, and the condition for that – for having that privilege is to agree to a restriction on licensing. That in turn allows the marketplace to know that they're dealing with a standard that anyone can comply with on a – on a reasonable basis without – without being, if you'll excuse the expression, gouged in terms of IP licensing royalties[294].

Other witnesses agreed that JEDEC wished to secure knowledge of potential patents and protections against the unrestricted exercise of patent rights[295].

("delay is not a viable market option. . . . You have to move in real time at the time that technology is being developed to create the standards.").

[293] J. Kelly, Tr. 1777.

[294] *Id.* at 1782.

[295] *See, e.g.*, Williams, Tr. 771-72, 794; Calvin, Tr. 1002; Sussman, Tr. 1333. Rambus suggests that a portion of the EIA Legal Guides rejects any goal of avoiding hold-up. RB at 9-10; *see also* ID at 261-62. According to those Guides, "Standards are proposed or adopted by EIA without regard to whether their proposal or adoption may in any way involve patents . . . ." CX 204 at 4. The Initial Decision correctly construes this as a "non-liability disclaimer," IDF 633 – the next sentence of the EIA Legal Guides states that EIA does not assume any obligation to parties adopting EIA standards. CX 204 at 4; *see also* J. Kelly, Tr. 1836-37. Treating this as evidence that JEDEC had no goal of avoiding hold-up stretches a mere disclaimer beyond its limits. The language reveals a willingness to accept patented technologies for standardization under stated conditions, but that does not negate a parallel objective to protect against

d. Disclosure Expectations of JEDEC Members

A number of witnesses besides Crisp testified that they understood that the disclosure of *patents* and *patent applications* was expected. For example, witnesses from Micron,[296] NEC/Sanyo,[297] AMI-2,[298] Intel,[299] and Hewlett Packard (HP),[300] among other JEDEC participants,[301] consistently testified that

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hold-up whenever patented technologies are adopted. *See* J. Kelly, Tr. 1837-40.

[296] *See* Williams, Tr. 771-72, 774 (members "had to" disclose), 788-89, 791-96 (disclosure of applications required during 1991-93 period); Lee, Tr. 6595-96 (from the time that he started attending JEDEC meetings in the mid-1990s, disclosure of applications was required); Lee, Tr. 6695-96 ("a requirement to disclose").

[297] *See* Sussman, Tr. 1333, 1346 (disclosure "required," not voluntary), 1333-34 (disclosure of applications required), 1341-42 (requirement to disclose applications antedated JEP21-I by at least 10 years).

[298] *See* Rhoden, Tr. 309, 317-19, 344-45 ("everyone had the obligation to disclose"), 619 ("you were obligated to disclose"), 627, 317 (disclosure of applications was always required), 320-21, 332 (Townsend would always say disclosure of applications was required), 357 (duty to disclose covered applications), 637 (same).

[299] *See* Calvin, Tr. 1003-04 ("anyone who was aware of patent – patented items, that could affect policy, had an obligation to bring that awareness to the group); 1006-07 (a requirement to disclose patent applications), 1012-13 (same).

[300] Landgraf, Tr. 1693-95 (from the time that he started attending JEDEC meetings in 1994, disclosure of applications was required).

[301] *See, e.g.*, **[REDACTED]** ; McGrath, Tr. 9245 (during the 1992-96 period there was "an expectation that patent applications would be disclosed"); CX 2089 at 142-43 (Meyer *Infineon* Trial Tr.) (*in camera*) (JEDEC disclosure rules covered applications in April-July 1992).

JEDEC members were "obligated" or "required" to disclose both patents and applications.[302]

Several of these witnesses also testified to an expectation that members would disclose planned amendments to pending applications. One witness testified that there was an obligation to disclose "everything that is in the patent process . . . if you intend to seek protection of your intellectual property as it relates to the standard . . . ."[303] Similarly, another witness testified that the disclosure obligation focused on the reasonable possibility that a firm's "invention" might apply to what was being discussed within JEDEC, "no matter what stage a patent might be."[304] As stated succinctly by a former HP employee, "the expectation was that members would disclose anything they're working on that they potentially wanted to protect with patents down the road."[305]

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[302] IBM's Gordon Kelley believed that the understanding that disclosure of applications was mandatory may have developed over time, with two JEDEC Committees, JC 42 and JC 16, requiring disclosure of applications by 1991 and JEDEC as a whole doing so by 1993. *See* G. Kelley, Tr. 2667-70, 2685-86, 2690-92. A witness from Mitsubishi presented varying descriptions. *See*

[REDACTED]

. One other witness stated that it was his understanding that applications did not have to be disclosed if any ensuing patents would be made available under reasonable and nondiscriminatory terms, but that that "may have been wrong." Wiggers, Tr. 10591.

[303] Rhoden, Tr. 317-21, 636.

[304] Williams, Tr. 788, 791.

[305] Landgraf, Tr. 1698-99. *See also* Sussman, Tr. 1341 ("something that you're about to apply for"); G. Kelley, Tr. 2406-07 (there was an obligation to disclose "material that would probably become a patent"). EIA General Counsel/JEDEC legal counsel John Kelly explained that the need to disclose when making plans to amend derived from the *present* "interpretation of the original patent or patent application," not from "the future plan, as such." J. Kelly, Tr. 1995. *But see* CX 3136 at 28-29 (Meyer *Infineon* Trial Tr. 110-11) (*in camera*) (stating his understanding that disclosure of plans to modify applications was not required, but explaining that he drew this conclusion only

e. The Behavior of JEDEC Participants

The expectation that members would disclose their patents and patent applications was supported by their actions. Although JEDEC's members were not expected to disclose if they did not plan to enforce their patents against JEDEC-compliant standards,[306] there were numerous examples of JEDEC members disclosing patents and applications relevant to the standards under consideration. For example, in February 1992, during Rambus's first JEDEC meeting as a member, Fujitsu disclosed a patent application, as described by initial Rambus JEDEC representative Garrett in a memorandum to Rambus staff.[307]

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from an absence of discussion of the issue and that he could not state whether or not this was JEDEC's policy).

[306] For example, Micron's Terry Lee testified that Micron had failed to disclose patent activity in or around 2000 when it had "no intent on enforcing the patent against the standard." Lee explained, "My understanding was that if they failed to disclose the patent that may relate to the work of the committee and if it was adopted into the standard, that they would forego their right to enforce the patent against the standard." Lee, Tr. 6599. Micron also disclosed three burst EDO patent applications in April 1996, after the standard already had been issued. *See* Williams, Tr. 937-40. A Micron representative testified that Micron never intended to enforce patents on burst EDO against firms that might practice JEDEC's burst EDO standard. *Id*. at 960-62. *But cf.* CX 364 (Micron letter disclosing the patents to JEDEC and affirming that "[i]n accordance with EIA/JEDEC patent policy" if a patent issued, Micron would license under RAND terms). Burst EDO died, and the standard never became a factor in the market. Williams, Tr. 961-62. Another example was Hitachi's failure to disclose a patent that was never enforced. Sussman, NEC/Sanyo's JEDEC representative, testified that, " . . . Hitachi has never tried to apply the patent, so some engineer has a few extra dollars, and basically a [sic] don't care." Sussman, Tr. 1337-38.

[307] CX 672 at 1; *see also* JX 22 at 14-16 (patent tracking list showing disclosure of both issued patents and applications); CX 42 at 16-17 (same); JX 28 at 6 (minutes describing MOSAID's December 1995 disclosure of "a patent pending on DLL"); CX 711 at 169 (Crisp's description of Fujitsu's disclosure of an application in September 1992); RX 1559 at 2 (Micron's January 2000 disclosure of an application);

JEDEC and its members reacted negatively when members sought enforcement after failing to disclose that a patent was issued or pending, and without providing the necessary RAND assurances. The record reveals three such instances – all of which were known to Crisp and thus to Rambus.[308]

The first instance occurred in the late 1980s and early 1990s involving then-JEDEC member Wang Laboratories. Wang held a patent application relating to memory modules[309]. During its membership, Wang helped JEDEC set a standard relating to memory modules, but failed to disclose its intellectual property[310]. After the standard was adopted, Wang sought to enforce its patents against the industry[311]. Considerable litigation ensued, and the incident generated concern and discussion among JEDEC participants about the need to prevent the problem from recurring.[312]

The second instance involved a proposal by a company called SEEQ, which sought adoption of a standard regarding silicon signature[313]. SEEQ had two patents or applications relating to the

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[308] *See* CX 711 at 188 (Crisp e-mail discussing incidents involving Wang and SEEQ); CX 346 (JEDEC minutes reporting on JEDEC members' reaction to Texas Instruments's conduct).

[309] IDF 689. *See* J. Kelly, Tr. 1931-32.

[310] IDF 690.

[311] Williams, Tr. 787; Sussman, Tr. 1338; Landgraf, Tr. 1697-98.

[312] J. Kelly, Tr. 1932; Grossmeier, Tr. 10954.

[313] Sussman, Tr. 1338.

technology, but disclosed, and provided licensing assurances for, only one.[314] JEDEC learned of the second item when it was recommending standardization of the SEEQ technology, and it sought RAND assurances, which SEEQ apparently refused[315]. Ultimately, JEDEC chose an alternative technology[316]. Although the events traced to 1989, they left "a negative taste in our mouth" that was still "almost current" in 2003.[317]

The third occurrence involved an attempt by Texas Instruments (TI) to enforce an undisclosed patent on Quad CAS technology. After JEDEC learned of the patent in 1993, the JC 42.3 subcommittee placed a ballot covering the technology on hold,[318] and voted to withdraw a preexisting standard[319]. It took the ballot off hold and dropped the withdrawal of the standard only after TI had provided satisfactory assurances of compliance with JEDEC's licensing policies[320]. A witness from Micron testified that TI's actions led to "a great uproar" and that TI's representative was "pummeled in th[e] meeting for his failure to disclose."[321] Crisp reported to his superiors that TI was "chastised" for not reporting the patent and that discussion was

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[314] *Id.* at 1338-39.

[315] CX 3 at 4; CX 711 at 188.

[316] *See* Sussman, Tr. 1338-39.

[317] *See* Sussman, Tr. 1339 ("[W]e were making nasty comments about SEEQ for years . . . .").

[318] JX 17 at 6-7.

[319] JX 18 at 7-9.

[320] JX 25 at 5.

[321] Williams, Tr. 776-77.

"nasty."[322] In the course of the dispute, IBM's Gordon Kelley, chairman of JC 42.3's DRAM Task Group, addressed TI in the strongest of terms:

> I am and have been concerned that this issue can destroy the work of JEDEC. If we have companies leading us into their patent collection plates, then we will no longer have companies willing to join the work of creating standards . . . . If we allow JC-42 standards to be used for patent collection purposes, then we do a great disservice to the very industry that feeds us.[323]

JEDEC's responses to the SEEQ, Wang, and TI incidents evidence that JEDEC members believed that these firms had acted in ways contrary to JEDEC's policies and members' expectations.

f. Knowledge of JEDEC Participants

The ALJ concluded[324] that since 1989 the DRAM industry has been aware of Rambus's inventions in the relevant markets and its plans to seek patent protection. Rambus points to presentations regarding its technologies made to several JEDEC members before and during its membership[325]. Rambus also cites, and the

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[322] Crisp, Tr. 2969, CX 710 at 1. *See also* CX 346.

[323] CX 2384 (G. Kelley letter to TI of January 14, 1994).

[324] ID at 305-09.

[325] *See, e.g.*, RX 273 (Rambus presentation to IBM in April 1992). These presentations were covered by nondisclosure agreements, required by Rambus from each company that was exposed to RDRAM technology. *See* Parties' First Set of Stipulations, Items 3-7 (noting nondisclosure agreements with NEC, Sony, Toshiba, HP, and Samsung); Kellogg, Tr. 5053 (stating that Rambus met with International Business Machines (IBM) and required "a nondisclosure agreement of sorts"); Bechtelsheim, Tr. 5816-19 (noting that Rambus met with Sun Microsystems (Sun) and required nondisclosure

ALJ highlighted, Rambus's publication in the early 1990s of technical descriptions of its inventions, as well as Rambus's 1992 distribution of marketing brochures describing its technology in conjunction with the public announcement of its business plan[326]. Rambus further argues that statements during its campaign to convince various industry players to adopt and license RDRAM placed the industry on notice regarding Rambus's intellectual property.[327]

The only information that Rambus made available, however, was that it was claiming patent rights with regard to technologies in *RDRAM* – not with respect to SDRAM, DDR SDRAM, or any JEDEC-based successors. The prevailing view in the industry was that RDRAM, with its narrow-bus architecture and its multiplexing and packetization, was quite different from the SDRAM and DDR SDRAM standards that were being developed by JEDEC[328]. JEDEC representatives who viewed an RDRAM

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agreements); CX 535 at 1 (stating Rambus's intention to secure nondisclosure agreements from "all parties exposed to the [Rambus] technology"). These nondisclosure agreements barred those hearing the presentations from sharing Rambus information with other firms.

[326] RB at 37; IDF 109-21, 130-34, 144-58; ID at 306.

[327] *See* RB at 36-37.

[328] *See, e.g.*, Rhoden, Tr. 402-03; (RDRAM was multiplexed and packetized); Sussman, Tr. 1431-33 (same); Lee, Tr. 6602-03 (RDRAM used narrow bus and was multiplexed); Farmwald, Tr. 8275 (RDRAM packetized); Horowitz, Tr. 8617-18 and 8620 (RDRAM multiplexed), 8621 (RDRAM packetized); CX 1451 at 9, 43 ('898 application describing a "narrow, multiplexed (time-shared) bus"); RX 81 at 7 (1992 Rambus Corporate Backgrounder describing Rambus technology as "a narrow, high-speed bus"). (Although the initial idea behind RDRAM was to use a narrow bus, Horowitz, Tr. 8619-20, as time went by RDRAM's bus widened. *See* Farmwald, Tr. 8143-44.)

In contrast, SDRAM and DDR SDRAM had a wider bus, little or no multiplexing, and were not packetized in the same sense as RDRAMs. *See*,

presentation emerged with the view that RDRAM bore little or no resemblance to JEDEC-compliant SDRAM[329]. For example, IBM's Gordon Kelley testified that after Rambus presented its technology to IBM in April 1992, he believed that "the Rambus DRAM [RDRAM] was so different from the synchronous DRAM being discussed at JEDEC that [he] just did not believe that anything that Rambus had on the RDRAM might apply to the SDRAM or to JEDEC."[330] Indeed, Rambus's own Joel Karp highlighted the extent to which the industry perceived fundamental differences between RDRAM and SDRAM/DDR SDRAM when, in May 1999, he stated, "They probably think they avoid our IP if they don't go 'packet based.'"[331] Under these circumstances, an awareness that Rambus held or likely would seek patents covering RDRAM did not equate to any contemplation that Rambus could or would obtain patents on SDRAM or DDR SDRAM.

The ALJ and Rambus also rely on the publication in October 1991 of Rambus's international patent application, known as the PCT application, to show that the industry had notice that Rambus

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e.g., Rhoden, Tr. 400-01 (SDRAM had a wider bus than RDRAM); Sussman, Tr. 1439 (same); G. Kelley, Tr. 2573-74 (JEDEC DRAMS were not packetized); Kellogg, Tr. 5298 (JEDEC did not consider narrow bus, packetized architecture); Jacob, Tr. 5462-64 and 5470-71 (JEDEC-based DRAMs used wider buses), 5464-67 (SDRAMs used separate buses for data, control, and address information and were not packetized in same way as RDRAMs); Bechtelsheim, Tr. 5841 (RDRAM used a packet transaction format, and SDRAM did not); Tabrizi, Tr. 9119 (JEDEC DRAMS were not multiplexed).

[329] *See* G. Kelley, Tr. 2538; Sussman, Tr. 1439-40; Kellogg, Tr. 5053; Lee, Tr. 6602-03.

[330] G. Kelley, Tr. 2537-38.

[331] CX 1069.

might acquire patents covering SDRAM and DDR SDRAM[332]. Rambus similarly relies on its September 1993 disclosure to JEDEC of the '703 patent, which had substantially the same written description as the PCT and '898 applications.[333]

We find that these materials did not provide notice that Rambus might seek to enforce patent rights covering the standards under consideration by JEDEC. None of the original 150 claims in the '898 patent application – which were reproduced in the PCT application – covered SDRAM or DDR SDRAM;[334] nor did any claims in the '703 patent.[335] Although notice might come from the written descriptions as well as from the claims, those descriptions, like Rambus's RDRAM marketing efforts, suggested that claims would be confined to the RDRAM architecture – with a narrow bus, multiplexing, and packetization. Several JEDEC members reviewed Rambus's PCT application or '703 patent and concluded that they had no relevance to JEDEC's standards. Thus, when Infineon's Meyer read the PCT application and the '703 patent, he understood them to relate to RDRAM, including, specifically, its multiplexing[336]**.** And when Micron's Terry Lee reviewed Rambus's patent abstracts and the '703 patent in 1995, he concluded that the patents "seemed to apply kind of specifically to

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[332] *See* RB at 39-41, 117; ID at 298, 307. This application, filed pursuant to the Patent Cooperation Treaty ("PCT"), CX 1454 at 1; IDF 826, was virtually identical to the '898 application, the parent application for the patents that Rambus has asserted against SDRAM and DDR SDRAM manufacturers. *See* IDF 826; Fliesler, Tr. 8811; CX 1451; CX 1454; Parties' First Set of Stipulations, Item 22.

[333] IDF 181; Jacob, Tr. 5500-01.

[334] Nusbaum, Tr. 1526; Jacob, Tr. 5494; Parties' First Set of Stipulations, Item 9 (discussing SDRAM).

[335] Parties' First Set of Stipulations, Item 10; *see also* Crisp, Tr. 3173-74; Jacob, Tr. 5498-99.

[336] *See* CX 2089 at 147-48 (Meyer *Infineon* Trial Tr.) (*in camera*).

this bus architecture, to this RDRAM product. . . . the narrow bus with the command/address/data multiplexed with this Rambus architecture and Rambus signaling scheme."[337] Even Rambus's own JEDEC representative, Crisp, initially read the '898 application as limited to multiplexed, packetized architectures, *i.e.*, to RDRAM.[338]

Rambus attempts to transform its argument into a matter of law by presenting the following syllogism: (1) the PTO may only approve patents when their written description covers their claims; and (2) the PTO issued the patents that Rambus has sued upon; so that (3) the written description in the '898/PCT

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[337] Lee, Tr. 6610-11; *see also* Sussman, Tr. 1445, 1449-54 (stating that he found no connection between the PCT application and JEDEC's work). *But cf.* Sussman, Tr. 1467-68 (concluding that a portion of the PCT application highlighted by Rambus counsel did relate to dual-edge clocking).

Rambus argues that because Mr. Lee in 1997 informed JEDEC that a Rambus patent might relate to JEDEC's work, he could not have believed that the Rambus architecture mattered. RB at 41. The technology that Mr. Lee identified to JEDEC was a loop-back clocking scheme, Lee, Tr. 6956-64, one of only two aspects of the '898 application that *did not* contain the multiplexed bus limitation that distinguished Rambus's architecture from JEDEC's work. Nusbaum, Tr. 1520, 1528. Rambus also points to an incomplete translation of Mitsubishi's analysis of the PCT application; the translation shows awareness that the application covered relevant technologies, and found "similar[ity] to SDRAM's latency control," but it also includes several references to "packets" or "packetize[d] bus" and does not indicate whether claims could extend beyond the RDRAM architecture. *See* RX 379a and RX 2213a. Mitsubishi subsequently recommended concentrating on "a wide-bus approach" because "Narrow-bus is Rambus look alike," suggesting that Mitsubishi still believed that avoiding RDRAM architecture mattered. RX 852 at 1.

[338] Crisp, Tr. 2926-27. Crisp added that over time his view of the scope of Rambus's application changed. *Id*. at 2927-28. Rambus's expert witnesses asserted that the written descriptions would have given notice of the potential reach of Rambus's claims, *see, e.g.*, Fliesler, Tr. 8788-89, 8810; Geilhufe, Tr. 9556-59, but Complaint Counsel's experts stated the opposite. *See* Nussbaum, Tr. 1642-43; Jacob, Tr. 5460-67; 54576-85, 5490, 5493, 5498-501.

applications and the '703 patent necessarily must have given adequate notice to the world of every claim that eventually issued[339]. This miscasts an inquiry designed for application with hindsight as a test for the reasonable bounds of foresight. The ability, after the fact, to determine from a written description that at the time of filing an applicant "*was* in possession" of a particular invention "*now* claimed"[340] is not the same thing as the ability to predict, prior to their publication, the potential scope of future claims[341]. Rambus's own patent expert regarded the unrevealed claims of a published application as "the family jewels."[342] Rambus avoided displaying those jewels to JEDEC members, and we find that, without knowledge of Rambus's eventual claims, JEDEC members were unable to foresee the implications of the pending applications.

Finally, the ALJ and Rambus point to two incidents – one involving IBM and Siemens in 1992, the other involving Rambus licensing negotiations in 1995 – to demonstrate the industry's awareness of Rambus's relevant patents and patent applications. The IBM/Siemens incident involved a conference call on April 29, 1992, recorded as follows in Siemens's notes: "RAMBUS has

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[339] RB at 39-40.

[340] *See* Vas-Cath, Inc. v. Mahurkar, 935 F.2d 1555, 1563-64 (Fed. Cir. 1991) (describing patent law's written description requirement) (emphasis added).

[341] Rambus acknowledges this distinction, averring that "[a] patent application continues to hold valuable trade secrets even after the written description becomes public . . . . Disclosure of the written description does not reveal the *claims* in the pending application." RB at 87 (emphasis original).

[342] Fliesler, Tr. 8896. Fliesler agreed that "[a]n engineer or a patent lawyer could not have known for certain what Rambus would claim from reading the '898 specification," *id*. at 8902, although he nonetheless insisted that the '898 application "indicat[ed]" that Rambus had invented the four relevant technologies as used in SDRAM and DDR SDRAM. *Id*. at 8904-05.

announced a claim against Samsung for USD 10 million due to the similarity of the SDRAM with the RAMBUS storage device architecture."[343] The only concern, however, was that Rambus might have a patent on a technology outside any of the alleged relevant product markets in this case[344]. Ultimately, IBM and Siemens both concluded that Rambus posed no patent problems for SDRAM.[345]

The other incident involved Rambus meetings with LG Semiconductor, Samsung, NEC, and Oki in 1995, at which Rambus CEO Tate claimed he announced that Rambus was seeking patents on DDR SDRAM[346]. In his testimony, Tate did not indicate the specific information that he purportedly conveyed. While his testimony names on-chip PLL and dual-edge clocking as the likely technologies at issue, nowhere does he state that he identified those technologies to the outside firms.

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[343] RX 286a at 2. The record does not provide details regarding this claim which, had it existed, would have antedated Rambus's first issued patent by more than a year. Parties' First Set of Stipulations, Item 11; CX 1460 at 1.

[344] *See* RX 297 at 5 (showing that a few days later, in the course of discussing two-bank designs at JEDEC's May 4-8, 1992 meetings, Siemens and Philips indicated that they were "concerned about [the] patent situation" with regard to Rambus and Motorola); *see also* RX 303 (June 1992 presentation by Gordon Kelley to IBM and Siemens engineers listing "cons" for SDRAMs to include "Patent Problems? (*Motorola/Rambus*)") (emphasis added); CX 2089 at 41-44 (Meyer *Infineon* Trial Tr.) (the concern in May 1992 for Meyer was the possibility that Rambus might obtain patents covering two-bank synchronous DRAM design); RX 289 at 1 (Siemens document prepared by Meyer on May 6, 1992, stating concern that "2-BANK SYNC MAY FALL UNDER RAMBUS PATENTS"). Although the ALJ also cites an IBM "Rambus Assessment" as revealing IBM's concern that Rambus might have patents over SDRAM, IDF 791-95, ID at 307, the document says nothing about such patents. RX 279.

[345] G. Kelley, Tr. 2537-38, 2545-46; CX 2089 at 151-52 (Meyer *Infineon* Trial Tr.) (*in camera*).

[346] CX 2111 at 313-21 (Tate FTC Dep.) (*in camera*).

Other evidence suggests that any information conveyed by Rambus would have been opaque. Indeed, a 1997 Tate e-mail indicates that LG continued to believe that DDR SDRAM was a "royalty-free alternative[]" to RDRAM[347]. Moreover, Rambus President Mooring admitted that, to the best of his knowledge, Rambus did not inform any DRAM manufacturer that [Rambus intellectual property covered SDRAM and did not tell anyone that on-chip PLL might infringe a Rambus patent until late 1999[348]. Similarly, Rambus's Senior Vice President Gary Harmon testified that any discussion relating to the [scope of Rambus's patents in the course of 1993-96 licensing negotiations, including those with all four firms identified by Tate, would have been "just a passing reference" and that, even in the case of the one firm with which discussions were more extensive, "I don't believe we ever specifically stated that we had intellectual property that applied to – outside of the Rambus-compatible area]."[349]

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[347] CX 957 at 1. Tate did not correct LG's misimpression, despite having an incentive to do so if he already had chosen to inform LG of Rambus's patent position on DDR SDRAM.

[348] CX 2112 at 172-73, 179-80 (deposition transcript at 171-72, 178-79) (Mooring FTC Dep.) (*in camera*). Rambus apparently did tell Intel in late 1997 or early 1998 that Rambus might have patent applications related to DDR, but Rambus provided "no specifics" and gave "nothing concrete" as to what the applications covered. MacWilliams, Tr. 4905.

[349] CX 2070 at 42-47 (Harmon *Micron* Dep.) (*in camera*). In addition, a 1997 e-mail from the Chairman of Rambus's Board of Directors, William Davidow, stated that "[o]ne of the things we have avoided discussing with our partners is [the] intellectual property problem," which he identified as the fact that "SLDRAM and SDRAM-DDR infringe our patents." CX 938.

Even assuming *arguendo* that certain JEDEC representatives who observed Rambus's presentations were aware of the extent of Rambus's patent portfolio, each representative's company was prohibited by non-disclosure agreements from discussing the content of Rambus's license presentations. *See, e.g.*, RX 24 at 2-3 (nondisclosure agreement between Rambus and IBM); RX 570 (nondisclosure agreement between Rambus and NEC); Rhoden, Tr.

JEDEC members repeatedly testified that they were unaware of Rambus's patent position when they adopted the standards. NEC/Sanyo's Sussman testified that prior to 1999 Rambus never suggested or did anything that put him on notice that its patents might relate to either SDRAM or DDR SDRAM[350]. HP's Landgraf stated that while he was at JEDEC (from 1994 through 1998), he "did not know of patents or patent applications with regard to dual edge clock or PLL on chip" and believed that the DDR SDRAM standard was free of undisclosed patents[351]. Cisco's Bechtelsheim termed Rambus's infringement suits "a complete surprise"; when asked whether before 2000 he had ever heard any rumor or suggestion that Rambus might have patents that would extend to SDRAM or DDR SDRAM, Bechtelsheim answered, "I did not."[352] Similarly, IBM's Gordon Kelley testified that when he voted to include programmable CAS latency and burst length in SDRAM, he had no understanding that Rambus might have relevant patents.[353]

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521 (HP); Kellogg, Tr. 5052-53 (IBM); Bechtelsheim, Tr. 5818-19 (Sun); CX 673 (Crisp, interpreting NEC's nondisclosure agreement to bar circulation of a published international patent application). JEDEC members would not have been able to discuss the implications of Rambus's patents, absent disclosure by Rambus itself. *See, e.g.*, CX 993 (Tate 1998 e-mail stating, "[O]ur partners employee's [sic] working on competitive products, e.g., DDR, might have access to our confidential information. [T]hey might even go to committees like jedec to discuss DDR. BUT they are obligated as employees of our partners' [sic] to keep our confidential information secret . . . .").

[350] Sussman, Tr. 1455-56.

[351] Landgraf, Tr. 1711-12.

[352] Bechtelsheim, Tr. 5880-81.

[353] G. Kelley, Tr. 2561-62.

Contemporaneous views support this testimony. In October 1993, when Willibald Meyer prepared documentation for Siemens of the status of work regarding SDRAM, he concluded that "we had managed to define a public domain version" of the next generation DRAM, free of intellectual property[354]. Hyundai's July 1997 "DRAM Product Roadmap" described DDR SDRAM as the most "cost effective" next generation DRAM with an "open architecture without royalties or fees."[355] A 1998 Siemens presentation compares RDRAM's "Proprietary solution (Royalties, License fees)" unfavorably with SDRAM II's "Open standard."[356]

In addition, it makes little sense that JEDEC members – which had, for example, "chastised" TI during a "nasty" discussion when it attempted to enforce an undisclosed patent[357] and which cared deeply about cost[358] – would, if they had known about Rambus's patents and patent applications, simply have ignored them and, knowingly and without discussion or hesitation, adopted a standard incorporating Rambus's technology. At a minimum, we

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[354] CX 2089 at 151-52 (Meyer *Infineon* Trial Tr.) (*in camera*).

[355] CX 2294 at 15. Similarly, Hyundai's 1998 cost comparison between DDR SDRAM and Direct RDRAM listed "Direct Rambus Royalty" as a "Cost Adder." CX 2303 at 16. And Hyundai's April 1999 presentation to the PC Platform APAC Technology Forum contrasts the benefits of DDR SDRAM's open standard with the negative impact of RDRAM's royalty cost. CX 2334 at 25, 27.

[356] CX 2442 at 36. Although Rambus cites a 1997 internal Micron e-mail as evidence that an Intel employee had told Micron's Intel account representative that Rambus might claim patent coverage over DDR SDRAM, Micron regarded the rumor as "typical" of "misinformation" and "overstatements" that were circulating in advance of Rambus's initial public offering and did not credit it. *See* Lee, Tr. 6700-10, discussing RX 920 at 1-2.

[357] *See supra* note 322 and accompanying text.

[358] *See infra* notes 404-408 and accompanying text.

would expect the members to have confronted Rambus and demanded RAND terms (even if, as Rambus argues, its technology was so superior that JEDEC had no choice but to adopt it).[359]

Rambus's own documents evince the belief that it had kept secret its patent position relative to JEDEC's standards. In August 1997, Rambus CEO Tate remarked, "[W]e already have the 327 patent but few people are aware of what it means," continuing, "[O]ur policy so far has been NOT to publicize our patents and i think we should continue with this."[360] In May 1999, Rambus Intellectual Property Vice President Karp surmised, "They probably think they avoid our IP if they don't go 'packet based.'"[361] In November 1999, Rambus named its IP initiative "Lexington 'The Shot Heard Around the World,'"[362] which Karp thought fitting because, "We fully anticipated at that point that once people became aware that we had IP covering sync DRAM, DDR, that it was going to make some noise."[363] Even in December 1999 Tate was still directing that, if asked whether DDR SDRAM infringes Rambus IP, "it's important NOT to indicate/hint/wink/etc what we expect the results of our [infringement] analysis to be!!!"[364]

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[359] *See infra* Section IV.C.3.b. (concluding that Rambus has not demonstrated its claims of superior technology).

[360] CX 942; *see also* CX 919; CX 987 at 4.

[361] CX 1069 (commenting on an article entitled "Industry group will push DDR DRAMs").

[362] CX 5002 (designated R401047).

[363] CX 5069 at 54 (deposition transcript at 563) (Karp 2004 *Infineon* Dep.).

[364] CX 1089.

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We find nothing in the record to suggest that, in the cooperative environment prevailing at JEDEC, the incidents to which the ALJ and Rambus have pointed were sufficient to put JEDEC members on notice that Rambus would pursue a deceptive course of conduct to obtain patents covering JEDEC's standards, then engage in patent hold-up to extract royalties on terms of Rambus's choosing.

4. Rambus's Conduct Was Deceptive

JEDEC's policies (fairly read) and practices, as well as the actions of JEDEC participants, provide a basis for the expectation that JEDEC's standard-setting activity would be conducted cooperatively and that members would not try to distort the process by acting deceptively with respect to the patents they possessed or expected to possess. Those policies rested on an express duty of good faith, as well as an objective of avoiding creation of unnecessary competitive advantages. The policies also included rules to ensure that members periodically were reminded to disclose patents and patent applications, and that patented technologies would be included in standards only after receipt of RAND assurances. JEDEC thus presented the type of consensus-oriented environment in which deception is most likely to contribute to competitive harm.

JEDEC's members expected disclosure of both patents and patent applications that might be applicable to the work JEDEC was undertaking, if the patents ever were going to be enforced against JEDEC-compliant products. These expectations were fostered by JEDEC's policies and were reflected by the behavior and understandings of JEDEC participants. Rambus's own descriptions of its understanding of the SSO's objectives and requirements reinforce that conclusion.

Rambus's course of conduct played on these expectations. Rambus sat silently when other members discussed and adopted technologies that became subject to Rambus's evolving patent claims. Rambus voted and commented on inclusion of programmable CAS latency and burst length without revealing that it was seeking patent coverage of those technologies, despite language on the ballot that called for disclosure of relevant patents. Rambus twice evaded direct questions about its patent portfolio, coupling a nonresponsive answer with a reminder that it previously had disclosed a patent (which lacked any claims then relevant to JEDEC's work). Rambus even provided JEDEC with a list of its patents that omitted the one patent Rambus believed covered JEDEC's work.

At the same time that Rambus was avoiding disclosure of its patent activity, Rambus was engaged in a program of amending its applications to develop a patent portfolio that would cover JEDEC's standards. Rambus made full use of information gleaned from its JEDEC participation to accomplish this objective. Rambus's JEDEC representative was charged with overseeing development of patent claims that would provide better coverage of products compliant with JEDEC's SDRAM standards, and Rambus's CEO asked for progress reports on claims that would cover the JEDEC standards.

Rambus argues that amending patent applications based on competitive information is a legitimate business practice condoned by the patent laws[365]. Rambus cites *Kingsdown Medical Consultants, Ltd. v. Hollister, Inc.*[366] and its progeny as establishing that there is nothing improper in amending claims to cover a competitor's product that the applicant learns about during the patent prosecution process. The cases relied upon by Rambus

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[365] RB at 89-91.

[366] 863 F.2d 867 (Fed. Cir. 1988), *cert. denied*, 490 U.S. 1067 (1989).

find no impediment, from a *patent law* perspective, to prosecuting or enforcing a claim developed under those circumstances[367]. These cases do not, however, involve either facts or law relevant here. None considers how the applicant learned of the competing product, or whether the applicant used that information in ways inconsistent with the understandings of other participants in a cooperative standard-setting environment. None of those cases examines the competitive consequences of the conduct.

In contrast, our concern in this proceeding is harm to competition, not to the patent system. Here, Rambus used information gained through participation in cooperative JEDEC processes by tailoring its patent claims to facilitate hold-up, while deceiving other JEDEC members regarding its patent position. The abuse of industrywide standard-setting efforts, and the competitive harms that may ensue, were not at issue in the cases cited by Rambus – but these factors are central to determining whether Rambus's actions constituted exclusionary conduct.

We find that Rambus's course of conduct constituted deception under Section 5 of the FTC Act. Rambus's conduct was calculated to mislead JEDEC members by fostering the belief that Rambus neither had, nor was seeking, relevant patents that would be enforced against JEDEC-compliant products. Rambus's silence, in the face of members' expectations of disclosure, created a misimpression that Rambus would not obtain and/or enforce such patents. When suspicions arose, Rambus allayed them with the reminder that it had made a prior disclosure. The message that Rambus reasonably conveyed – in a context in which it had been asked about its patent position, and in which

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[367] *See, e.g., Kingsdown*, 863 F.2d at 869, 872, 874 (considering a patent applicant's actions in terms of the "deceitful intent" element of purported "inequitable conduct before the [PTO]"); Emerson Electric Co. v. Spartan Tool, LLC, 223 F.Supp. 2d 856 (N.D. Ohio 2002) (refusing to infer that an applicant had deceived the patent examiner by amending a claim without highlighting all ramifications of the change).

other members expected disclosure of patents and applications – was that Rambus would have disclosed if it had had anything relevant to reveal. Even Rambus's withdrawal letter misleadingly conveyed the impression that it was listing its issued patents, while failing to disclose the one patent that might have mattered to the other JEDEC members. Under the circumstances, JEDEC members acted reasonably when they relied on Rambus's actions and omissions and adopted the SDRAM and DDR SDRAM standards.

Rambus withheld information that would have been highly material to the standard-setting process within JEDEC. JEDEC expressly sought information about patents to enable its members to make informed decisions about which technologies to adopt, and JEDEC members viewed early knowledge of potential patent consequences as vital for avoiding patent hold-up. Rambus understood that knowledge of its evolving patent position would be material to JEDEC's choices, and avoided disclosure for that very reason[368]. We thus find that Rambus engaged in representations, omissions, and practices that were likely to mislead JEDEC members acting reasonably under the circumstances, to their substantial detriment, and we conclude that Rambus intentionally and willfully engaged in deceptive conduct.

As discussed in detail in Sections IV.B. and IV.C. below, Rambus's course of deceptive conduct contributed significantly to Rambus's acquisition of monopoly power by distorting JEDEC's technology choices and undermining JEDEC members' ability to protect themselves against patent hold-up. This conduct caused harm to competition**.** In sum, the record establishes a *prima facie* case that Rambus engaged in exclusionary conduct.

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[368] Rambus now argues that disclosure would not have changed JEDEC's decision because of the superiority of Rambus's technologies. We address that argument *infra* in Section IV.C.3.b.

5. Rambus's Procompetitive Justification for its Conduct

Our finding that Complaint Counsel established a *prima facie* case of exclusionary conduct shifts the burden to Rambus to establish a nonpretextual, procompetitive justification for its conduct[369]. Rambus must prove "that its conduct is indeed a form of competition on the merits because it involves, for example, greater efficiency or enhanced consumer appeal."[370]

Deceptive conduct is extraordinarily difficult to justify[371]. Rambus tries to avoid this challenge by characterizing its conduct as a refusal to deal with its competitors or a failure to "share its trade secrets with others."[372] Rambus then defends its conduct on the grounds that it preserved the secrecy of Rambus's patent applications, which contained confidential information about Rambus's inventions[373]. Rambus's characterization ignores much of its deceptive course of conduct, as well as the context in which that conduct occurred.

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[369] A respondent may rebut a *prima facie* case of exclusionary conduct by introducing evidence of a procompetitive justification for its actions. *See* United States v. Microsoft Corp., 253 F.3d 34, 59 (D.C. Cir.), *cert. denied*, 534 U.S. 952 (2001).

[370] *See id*. For example, the D.C. Circuit found that Microsoft had "valid technical reasons" to cause its Windows operating system to ignore user-chosen browser defaults in certain circumstances. The court then found that the plaintiffs had failed either to rebut that justification or to demonstrate that the anticompetitive effect of the challenged action outweighed it. *Id.* at 67.

[371] *Id.* at 77 ("[u]nsurprisingly, Microsoft offers no procompetitive explanation for its campaign to deceive developers.")

[372] RB at 113.

[373] *See* RB at 86-88, 114-15.

As discussed above, Rambus engaged in a deliberate course of deceptive conduct that included selective omissions and outright misrepresentations relating to its intellectual property[374]. Indeed, Rambus used information obtained via its participation in JEDEC to help shape and refine the very patent applications it now claims it was seeking to protect[375]. Rambus's supposed desire to maintain the secrecy of its intellectual property does not justify the totality of its deceptive conduct in the standard-setting context.

We weigh Rambus's justification in the context of its conduct. In the competitive marketplace, companies generally are justified in choosing not to disclose or share their unpublished patent applications and trade secrets[376]. The ALJ (and Rambus), citing Rambus's patent law expert, found three reasons why, in a competitive context, the non-disclosure of this information serves legitimate and procompetitive purposes[377]. However valid these justifications might be in the abstract – or when applied within a competitive marketplace – they do not fit the record facts or the context that existed here. Further, if protecting trade secrets was critical to Rambus, it had the option to refrain from participating in JEDEC.

First, Rambus argued that withholding of information was justified because disclosure of that information "shows which inventions the applicant is seeking to protect, and thus reveals both technical information and the applicant's business strategies." Preserving trade secrets by preventing access by

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[374] *See supra* Section IV.A.

[375] *Id.*

[376] The PTO held patent applications in confidence during the period that Rambus belonged to JEDEC. In 1999, the law changed to require publication of most patent applications 18 months after filing. 35 U.S.C. § 122.

[377] ID at 288-89; RB at 87.

rivals in a competitive marketplace often may be procompetitive, particularly when that information is not otherwise protected from free-riding by those rivals. However, the technical information comprising Rambus's inventions (as opposed to its intentions to claim that those inventions covered technologies in JEDEC's DRAM standards – which, as discussed above,[378] could not be divined until the ultimate claims became public) already had been disclosed with publication of the written descriptions of the inventions in the PCT application and the '703 patent. Morever, Rambus has claimed in its numerous infringement actions that the patent laws provide full protection against unlicensed use of its technical inventions, at least for periods after Rambus's patents issued.

It is true that if Rambus had disclosed its relevant patent applications to JEDEC members, the disclosure might have exposed Rambus's business strategy to obtain patents covering JEDEC's DRAM standards – but Rambus does not explain how keeping that strategy secret would be procompetitive given the cooperative atmosphere of the SSO. To the contrary, disclosure would have enabled other participants in the standard-setting process to make their decisions based on knowledge that Rambus's business strategy was to enforce its patents and demand royalties if they were incorporated in standards adopted by JEDEC. As one treatise summarizes, withholding information as to the existence of patent applications in such a setting "would be most valuable as a tool for deception."[379]

Second, Rambus argued that disclosure "could jeopardize the applicant's ability to obtain foreign patents" by "enabl[ing] a competitor to win the 'race'" to foreign patent offices, most of

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[378] *See supra* notes 328-338 and accompanying text.

[379] II HOVENKAMP ET AL., IP AND ANTITRUST § 35.5 at 35-40 n. 17.11 (2006 Supp.).

which have "a 'first to file' rule."[380] But under typical first-to-file rules, patents go to the first *inventor* to file[381]. If a competitor merely read or heard Rambus's disclosure, copied its application, and filed first in a foreign jurisdiction, the competitor would not have invented the technology and would not be entitled to a patent[382]. Rambus failed to identify any foreign jurisdiction in which its ability to obtain patent protection would have been threatened by disclosures within JEDEC. Under these circumstances, and on this record, the only effect of Rambus's behavior was to prevent JEDEC participants – who expected Rambus to conduct itself cooperatively and without deception – from making their standard-setting decisions with knowledge of the consequences. That is not procompetitive.

Third, we are not persuaded that Rambus's non-disclosure of its patent applications was justified because disclosure "may enable a competitor to slow down or interfere with the patent application process," such as by "enabl[ing] a competitor to provoke an 'interference' at the Patent Office by claiming the

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[380] RB at 87_88.

[381] *See* Gerald J. Mossinghoff, *The First-To-Invent Rule in the U.S. Patent System has Provided No Advantage to Small Entities*, 87 J. PAT. & TRADEMARK OFF. SOC'Y 514 (2005) ("As between two true inventors claiming the same invention – as contrasted to copiers – *every* nation in the world, except the United States, grants the patent to the inventor who first undertakes to use the patent system . . . . In shorthand, this is called a first-to-file system of priority, but it is more appropriately called a first-inventor-to-file system.") (emphasis original); MARTIN J. ADELMAN *et al*., CASES AND MATERIALS ON PATENT LAW 160 (2003) (under a first-to-file system, "the *inventor* who first files a patent application obtains the patent, even if another actually invented the technology first") (emphasis added); Fliesler, Tr. 8839 (explaining the first-to-file race in terms of "*inventor* A and *inventor* B who are conceiving and reducing to practice and working independently, but simultaneously on the same invention") (emphasis added).

[382] *See* Fliesler, Tr. 8839 (the first one to file "that is otherwise entitled to a patent" prevails).

same invention in one of the competitor's applications."[383] This, too, is a hypothetical justification. There is no evidence in this record that Rambus's patent position in the United States or elsewhere would have been jeopardized in that fashion.

Finally, Rambus cites Crisp's trial testimony and an e-mail he sent to Rambus executives to support its claim regarding the protection of trade secrets[384]. Crisp testified that Rambus's outside patent counsel advised him that patent applications should be confidential; however, Crisp did not state that counsel's advice was tied to Rambus's course of conduct in the JEDEC standard-setting context[385]. Moreover, although Crisp's e-mail mentioned the desirability "of not disclosing our trade secrets any earlier than we are forced to," the context suggested that this comment reflected Rambus's desire for leverage over its customers[386]. There is abundant additional evidence in the record that Rambus's conduct was motivated by a desire to anticompetitively bias the standard-setting process[387]. In short, there is nothing to support Rambus's claim except the claim itself.

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[383] RB at 87.

[384] *See id*. at 49-50, 98-99.

[385] Crisp, Tr. 3473, 3495-96. Other, more specific advice from Rambus counsel (Diepenbrock as well as Vincent) identified the equitable estoppel risks associated with Rambus's JEDEC membership. *See* CX 837 at 1; CX 1942; CX 3125 at 320-21 (Vincent *Infineon* Dep.) (*in camera*).

[386] Crisp's same e-mail also referenced the need "to get the necessary amendments completed [and] the new claims added," and "make damn sure the ship is watertight," before making disclosures. *See* CX 837 at 2.

[387] *See, e.g*., CX 711at 73 ("it makes no sense to alert them to a potential problem they can easily work around."); CX 919 ("do *NOT* tell customers/partners that we feel DDR may infringe – our leverage is better to wait."); CX 1277a at 2 ("do not tell them :-").

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We find that Rambus did not carry its burden of establishing that its conduct served procompetitive purposes. The record establishes that the purpose and effect of Rambus's deceptive conduct was to manipulate the standard-setting process at JEDEC and gain market power. Furthermore, even if we were to credit Rambus's proffered justification, we find that it would not outweigh the anticompetitive effects of Rambus's exclusionary conduct, particularly in light of the potential to distort industrywide standard setting.

B. Possession of Monopoly Power

Monopoly power may be established either by direct evidence of such power – *i.e.*, the power to raise price above competitive levels or to exclude competition – or by indirect evidence, such as a high market share in a properly defined relevant market with high barriers to entry[388]. In order to support a Section 2 violation, such monopoly power must be durable. When barriers to entry are low, any attempt to exercise monopoly power (even by a firm with 100 percent market share) quickly would be countered by competition from new entrants.[389]

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[388] *See, e.g.*, United States v. Dentsply Int'l, Inc., 399 F.3d 181, 187 (3d Cir. 2005) ("monopoly power may be inferred from a predominant share of the market"); United States v. Microsoft Corp., 253 F.3d 34, 51 (D.C. Cir.), *cert. denied*, 534 U.S. 952 (2001) ("monopoly power may be inferred from a firm's possession of a dominant share of a relevant market that is protected by entry barriers").

[389] *See, e.g.*, Tops Markets, Inc. v. Quality Markets, Inc., 142 F.3d 90, 99 (2d Cir. 1998) ("We cannot be blinded by market share figures and ignore market place realities, such as the relative ease of competitive entry"); United States v. Syufy Enters., 903 F.2d 659, 665-66 (9th Cir. 1990) ("In evaluating monopoly power, it is not market share that counts, but the ability to *maintain* market share.").

As discussed above,[390] the alleged relevant product markets involve technologies that are incorporated in DRAM for use in current and recent-generation electronic memory devices[391]. The four alleged relevant technology markets are: (1) the latency technology market; (2) the burst length technology market; (3) the data acceleration technology market; and (4) the clock synchronization technology market. With respect to each of these four technology markets, the product market comprises alternative technologies available to address a given technical issue arising in the course of DRAM design[392]. The alleged relevant geographic market for each of these four technologies is the world[393]. Rambus accepts these market definitions.[394]

Rambus held over 90 percent of the market share in the relevant markets[395]. JEDEC's standards have been ubiquitous in

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[390] *See supra* Section II.A.

[391] IDF 1010-15.

[392] The Initial Decision also identifies a "cluster market" for synchronous DRAM technologies, which contains these four product markets. IDF 1014. In view of our findings regarding the four separate product markets, we need not separately consider the cluster market.

[393] IDF 1016-17. *See* IDF 1017 ("The relevant geographic market for each relevant product market is the world because: buyers of technology typically do not care about the geographic source of technology; technologies tend to be licensed worldwide; technologies tend to flow across national borders; downstream products are produced and used worldwide; and transportation costs of both technology and DRAMs are negligible.").

[394] *See* IDF 1013, 1015 ("Respondent does not challenge Complaint Counsel's product market definitions. Respondent's economic expert . . . testified the 'relevant market is not crucial to understanding competition and market power in this setting.'").

[395] *See* IDF 1020-21; CX 1386 at 4 ("We are on the cusp of achieving our original BHAG [Big Hairy Audacious Goal] • SDRAM + DDR + RDRAM > > 90% of the DRAM market"); CX 2112 at 310-11 (deposition transcript at 309-10) (Mooring FTC Dep.); McAfee, Tr. 7430 (testifying that the percentage

the computer industry: from 1998 on, the decided majority of DRAMs sold have complied with the JEDEC SDRAM and DDR SDRAM standards[396]. Rambus claims that its patents are necessary to make, use, or sell DRAMs that comply with the JEDEC standards[397]. Courts typically find such a high market share sufficient to infer the existence of monopoly power[398]. The ALJ determined that Rambus possessed monopoly power in the four key technology markets alleged, and Rambus does not dispute his findings in this respect[399]. We reach the same

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of worldwide commercial DRAM production exposed to Rambus's patent claims was "in the upper nineties").

[396] *See* CX 35 at 14-15 ("This JEDEC standardization process creates the structure from which all DRAM designs begin . . . JEDEC is the fulcrum for DRAM standards in Asia, the Americas and Europe").

[397] CX 2067 at 171 (Davidow *Infineon* Dep.) (*in camera*) ("Q. So am I right, then that it's Rambus's position [] that any SDRAM or RDRAM being used in main memory PCs today [January 31, 2001] are covered by their patents? . . . [A.] I would say that it is highly likely that is true."); McAfee, Tr. 7427-28 ("JEDEC standards have dominated the DRAM industry"), 7432-33; Rapp, Tr. 10248-49 (presenting market share statistics).

[398] *See* Eastman Kodak Co. v. Image Technical Servs. 504 U.S. 451, 481 (1992) (80% market share, with no readily available substitutes, sufficient to survive summary judgment on the possession of monopoly power); United States v. Grinnell Corp., 384 U.S. 563, 571 (1966) (87% of the relevant market left no doubt that defendants had monopoly power); United States v. E.I. du Pont de Nemours & Co., 351 U.S. 377, 379, 391 (1956) (control of 75% of a relevant market would constitute monopoly power); American Tobacco Co. v. United States, 328 U.S. 781, 797 (1946) (control of over two-thirds of the market is a monopoly).

[399] "Complaint Counsel have demonstrated that Respondent has monopoly power in the relevant markets." IDF at 252; *see also* IDF 1010-15. Rambus's economic expert, Rapp, testified that Rambus possessed market power. Rapp, Tr. 10046 ("[I]t is the case isn't it, that, in your view, Rambus today possesses market power in each of the relevant markets defined by [Complaint Counsel's expert] Professor McAfee? A. Yes.").

conclusion, and find that Rambus did acquire a monopoly position.

Rambus argues, however, that its monopoly power was not durable because the industry could have switched to alternative technologies relatively easily without incurring significant additional costs. We must therefore determine whether Rambus's deceptive and exclusionary conduct in the standard-setting context enabled Rambus to acquire durable monopoly power. We address that question below, as part of our broader analysis of causation issues.[400]

C. Causation

Having concluded that Rambus engaged in a deceptive course of conduct that constituted exclusionary conduct, and having found that Rambus acquired a monopoly position in the relevant markets, we turn to the critical issue of causation – *i.e.*, whether Rambus's exclusionary conduct was linked to its monopoly position.

We find that the same evidence establishing that Rambus engaged in exclusionary conduct and that it acquired monopoly power respecting the four key technologies incorporated into JEDEC's SDRAM standards contributes to a *prima facie* showing of a causal link between Rambus's conduct and its power. More specifically, we conclude that the evidence (1) links Rambus's conduct to JEDEC's adoption of SDRAM standards incorporating Rambus's patents and (2) links JEDEC's adoption of those standards to Rambus's acquisition of monopoly power.

1. Link between Rambus's Conduct and JEDEC's Standard-Setting Decisions

[400] *See especially infra* Section IV.C.3.d. (discussion of lock-in).

Rambus's strategy was to cause JEDEC to adopt SDRAM and DDR SDRAM standards incorporating its patents, and then to charge those practicing the standards royalties of its choosing. Although purpose is not a substitute for effect in a monopolization case, it is well-settled that "[e]vidence of the intent behind the conduct of a monopolist is relevant . . . to the extent it helps us understand the likely effect of the monopolist's conduct."[401] As the Supreme Court explained, "[K]nowledge of intent may help the court to interpret facts and to predict consequences."[402] Thus, we initially infer from the evidence respecting Rambus's purpose that, but for Rambus's deceptive course of conduct, JEDEC either would have excluded Rambus's patented technologies from the JEDEC DRAM standards, or would have demanded RAND assurances, with an opportunity for *ex ante* licensing negotiations. Indeed, the one time that JEDEC members had advance knowledge that a Rambus patent was likely to cover a standard under consideration, the members took deliberate steps to avoid standardizing the Rambus technology.[403]

JEDEC members – DRAM manufacturers and customers – were highly sensitive to costs, and that keeping costs down was a

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[401] United States v. Microsoft Corp., 253 F.3d 34, 59 (D.C. Cir.), *cert. denied*, 534 U.S. 952 (2001).

[402] Chicago Board of Trade v. United States, 246 U.S. 213, 238 (1918). *See also* United States Football League v. NFL, 842 F.2d 1335, 1359 (2d Cir. 1988) ("Evidence of intent *and* effect helps the trier of fact to evaluate the actual effect of challenged business practices in light of the intent of those who resort to such practices.") (emphasis original).

[403] In March 1997, when NEC proposed a "loop-back" clock system, some members expressed concern that it might be covered by Rambus's '703 patent, the one patent that Rambus had disclosed while it was a member of JEDEC. JX 36 at 7. The JEDEC committee immediately dropped the proposal and turned to consideration of technologies that it believed avoided Rambus's patent. *See* Rhoden, Tr. 527-28; Lee, Tr. 6695-96; CX 368 at 2.

major concern within JEDEC[404]. As a report by Rambus's Crisp put it, "Compaq (Dave Wooten) like the others, stressed that price was the major concern for all of their systems. They didn't particularly seem to care if the SDRAMs had 1 or two banks so long as they didn't cost any more than conventional DRAMs . . . Sun echoed the concerns about low cost. They really hammered on that point."[405] More succinctly, Crisp explained, "[T]hey want cheap, cheap, cheap."[406]

JEDEC members considered the potential cost of patents in weighing different alternatives. Witnesses, including representatives from DRAM manufacturers and their major customers, testified that knowledge of patents was an important factor in their decisions as JEDEC members[407]. For example, after

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[404] *See, e.g.*, G. Kelley, Tr. 2562 ("The overriding factor on all of my votes on DRAM was low cost"); Bechtelsheim, Tr. 5814 (JEDEC's "overarching goal" was "a cost-effective solution" for memory interfaces); CX 2107 at 136-37 (Oh FTC Dep.) (*in camera*) (avoiding costs, including royalties or fees, was important to Hyundai); CX 34 at 31 (IBM: "LOW COST!!! (<5% more than [previous generation] DRAM)"); CX 711 at 1 (Crisp e-mail reporting, "Desi [Rhoden of Advanced Memory International (AMI-2)] added that if the SDRAM doesn't cost less than 5% more than [previous generation] DRAM they will not be used"); CX 2383 (Sun letter to JEDEC members stating, "[S]ince we are very cost conscious we are willing to drop features that add too much cost or complexity"); CX 2777 (Micron: "[T]he age old rule for DRAMs still appl[ies]. Customers will take as much performance as we can give them for absolutely no added cost over the previous technology. They will not pay extra for increased DRAM performance."). An October 1994 internal Rambus e-mail summarized, "Our industry is very cost sensitive." CX 5109 at 4.

[405] CX 1708 at 2.

[406] CX 711 at 34 (explaining that "customers are willing to leave performance on the table in exchange for having lower cost systems").

[407] *See, e.g.*, Sussman, Tr. 1417 (Sanyo's JEDEC representative testifying, "If I understood that there was IP on the programmable, I would have voted – changed my direction and voted to take the fixed one."); Landgraf, Tr. 1714 (HP's JEDEC representative testifying that if Rambus had

testifying that the potential for royalty-bearing patents would have been relevant in analyzing programmable CAS latency and programmable burst length as compared to alternatives, Andreas Bechtelsheim added, "I personally and Sun [Microsystems] as a company would have strongly opposed the use of royalty-bearing elements in an interface patent – in an interface specification."[408] The total cost of payments for Rambus's undisclosed patents could amount to several billion dollars,[409] with some individual

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disclosed its patent applications, "If we knew in advance that they were not going to comply with the JEDEC patent policy, we would have voted against it."); G. Kelley, Tr. 2576 (IBM's JEDEC representative noting that "[p]atent issues are a concern on every JEDEC proposal" and that when a technology was considered for the first time "it was especially valuable to have the consideration of patents so that we could possibly avoid them"); Lee, Tr. 6686, 6717 (knowledge of Rambus's patent applications would have caused Micron to oppose on-chip PLL/DLL and dual-edge clocking); *see also* JX 5 at 4 (JEDEC minutes stating, "The important thing is disclosure. If it is known that a company has a patent on a proposal then the Committee will be reluctant to approve it as a standard.").

[408] Bechtelsheim, Tr., 5813-14. JEDEC members' response to Rambus's proprietary RDRAM technology reflected similar cost sensitivity. *See, e.g.*, JX 36 at 7 ("Some Committee members did not feel that the Rambus patent license fee fit the JEDEC requirement of being reasonable."); CX 961 at 1 (September 1997 Intel e-mail to Rambus CEO Tate stating the concern that, for at least the low end of the market, "absolute cost is the critical factor" and alternatives "need not be equivalent performance" and warning that, upon analyzing the royalty obligations attached to RDRAM, the industry would develop alternatives); RX 1482 at 12.

[409] *See* McAfee, Tr. 7653-54 (*in camera*) (estimating royalty payments to Rambus of $600 million per year); CX 527 at 1 (*in camera*) (projecting annual Rambus royalty revenue on SDRAM and DDR SDRAM of $2.1 billion dollars by 2005); CX 1391 at 32 (*in camera*) (suggesting that Rambus DRAM royalties could total more than $8 billion over the six years between 2000 and 2005); CX 1401 at 10 (*in camera*) (Rambus business plan projecting that DDR SDRAM royalties in 2005 would range from several hundred million dollars up to as much as $2.5 billion).

DRAM manufacturers each paying hundreds of millions of dollars[410]. Numbers of this magnitude are not easily overlooked.

Alternative technologies were available when JEDEC chose the Rambus technologies, and could have been substituted for the Rambus technologies had Rambus disclosed its patent position[411]. Some of the major firms in the industry found these alternatives viable, and even preferable[412]. JEDEC members – the principal buyers of the relevant technologies – gave these alternatives serious, searching consideration; in fact, the technologies as to

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[410] *See* Appleton, Tr. 6390-92 (Rambus's requested royalty would cost Micron hundreds of millions of dollars; Rambus royalties would be the equivalent of 25-50% of Micron's R&D expenditures).

[411] S*ee, e.g.*, G. Kelley, Tr. 2548-49 and Jacob, Tr. 5370-93 (alternatives to programmable CAS latency); Kellogg, Tr. 5110-11, 5131-32 and Jacob, Tr. 5397-5412 (alternatives to programmable burst length); Jacob, Tr. 5416-38 (alternatives to dual-edge clocking); Jacob, Tr. 5443-58 and Lee, Tr. 6655, 6664-67, 6676-78 (alternatives to on-chip PLL/DLL). *See generally* Bechtelsheim, Tr. 5786 ("in typical design activity one can make any number of choices, including choosing an interface that was not encumbered by a patent or royalty").

[412] For example, Samsung advocated the use of fixed, rather than programmable, CAS latency, JX 10 at 71; Rhoden, Tr. 425-27; Kellogg, Tr. 5099-100, and Cray proposed the use of fuses to set latency, CX 34 at 149, Kellogg, Tr. 5104. For setting burst length, Cray proposed using fuses, CX 34 at 149; Sussman, Tr. 1388-89; Kellogg, Tr. 5103-05, and Mitsubishi proposed using pins. Rhoden, Tr. 430-34; Kellogg, Tr. 5102; JX 10 at 5, 74. Samsung proposed fixed, rather than programmable, burst length. Rhoden, Tr. 425-27; JX 10 at 71. With regard to data acceleration, TI proposed doubling the frequency of a single-edge clock in place of dual-edge clocking. Lee, Tr. 6711-14; CX 371 at 3. As alternatives to on-chip PLL/DLL, Samsung proposed placing a single PLL on the memory controller, Rhoden, Tr, 513-14; Lee, Tr. 6691; JX 31 at 71; IBM proposed using vernier circuits, Kellogg, Tr. 5155; and Micron proposed using what it termed an "echo clock," Lee, Tr. 6655-56; 6664-67; JX 29 at 4, 17-22. Both Micron and Silicon Graphics also presented proposals for using data strobes in place of on-chip DLLs. CX 368 at 1-2, 4; CX 370 at 2-3; Lee, Tr. 6666-67, 6682-83.

which Rambus subsequently revealed patent claims sometimes were chosen only after prolonged debate.[413]

The ALJ rejected this evidence regarding JEDEC's cost sensitivity and technology debates because, in his opinion, it was based on "the subjective perceptions of JEDEC members at the time," reasoning that while it "may speak to whether JEDEC would have selected a [substitute] technology, it does not go to whether an alternative is equal or superior in objective terms."[414]

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[413] As to CAS latency and burst length, NEC/Sanyo's Sussman testified, "I had a lot of arguing to do to get the degree of programmable features into the part." Sussman, Tr. 1380. AMI-2's Rhoden explained that using fuses to set CAS latency and burst length "was one of the options that was considered for a very long time, until we finally settled on the [programmable] register." Rhoden, Tr. 429-30. Subsequently, sentiment for moving to fixed CAS latency and burst length remained strong: the SDRAM Lite task group proposals for reducing the cost of SDRAM included fixed CAS latency and burst length. *See* Rhoden, Tr., 475-76; Lee, Tr. 6626. Indeed, results of the SDRAM Lite survey ballot announced in January 1996 showed consensus support for fixed CAS latency of three and for fixed burst length of four, but no consensus for an additional latency or burst length. *See* Lee, Tr. 6627-32; JX 29 at 13-15.

Dual-edged clocking held only "mixed support" within JEDEC. JX28 at 35 (results of 1995 survey ballot). (This confirms a 1991 report from NEC's Sussman, finding a split between those who preferred high-speed, single-edge clocking and those who preferred dual-edge clocking at lower speeds. *See* Sussman, Tr. 1368-72; CX 20 at 1.) Debate over on-chip PLL/DLL reflected "differing viewpoints," with some JEDEC members preferring to use a data strobe and finding on-chip PLL/DLL unnecessary, but others wanting the latter feature; the result was "a compromise . . . to do both but provide the ability to turn off the DLL." *See* Lee, Tr. 6682-83; Sussman, Tr. 1404 (summarizing the on-chip PLL/DLL debate, "Ten engineers; 12 opinions."). *See also* CX 2713 at 2 and Lee, Tr. 6654 (1997 Micron e-mail arguing to JC 42.3 members that on-chip DLL has "more disadvantages than advantages" and should be eliminated); MacWilliams, Tr. 4918-20 (Intel study found on-chip DLL unnecessary at speeds under consideration).

[414] ID at 317.

The ALJ's analysis misses the point of the causation inquiry. Evidence that a properly-informed JEDEC may have selected a substitute technology suggests a causal link between Rambus's deceptive course of conduct and JEDEC's decision-making process. This evidence – combined with the evidence of Rambus's strategy, JEDEC members' overriding concern with costs, and the magnitude of the potential royalties in the absence of RAND assurances or the opportunity to negotiate *ex ante* – is enough to show that JEDEC's adoption of the SDRAM and DDR SDRAM standards was linked to Rambus's exclusionary conduct.

2. Link Between JEDEC's Standards and Rambus's Monopoly Power

JEDEC's adoption of standards incorporating Rambus's patented technologies is linked to Rambus's monopoly power. More specifically, as previously stated, the record shows: (1) that Rambus claims that its patents are necessary to make, use, or sell DRAMs that comply with the JEDEC standards; (2) that most DRAMs sold complied with the JEDEC SDRAM and DDR

SDRAM standards;[415] and (3) that Rambus acquired 90 percent market shares in all four of the relevant markets.[416]

These market results were a natural consequence of DRAM industry attributes. In part, the results reflected the nature and composition of JEDEC, a broad-based organization that included essentially all the DRAM manufacturers and their largest customers[417]. Once JEDEC reached a consensus as to which technologies to standardize, it is hardly surprising that those same manufacturers produced, and those same customers bought, products conforming to the standard they had adopted[418].

The market results also reflected the nature of the DRAM product itself, which drove standardization in the DRAM

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[415] In each year from 1994 through 2002, products compliant with JEDEC standards captured between 87-97% of DRAM revenues. *See* Rapp, Tr. 10099-100, 10248-49; Prince, Tr. 9020-21; CX 2112 at 310-11 (deposition transcript at 309-10) (Mooring FTC Dep.) (*in camera*). Rambus argues that multiple DRAM standards may and do exist at any given time, but almost without exception, the "multiple standards" in the market have been succeeding generations of JEDEC standards. *See* Rapp, Tr. 10248-49. Only with RDRAM in 2001-02 did any non-JEDEC-compliant DRAMs capture more than 3% of revenues. *Id*. Indeed, customers expressed reluctance to purchase anything other than JEDEC-compliant DRAMs for commodity applications. Rambus President Mooring, for example, testified that HP, Apple, and Sun all told him in 1991 that "we only use memories approved by JEDEC." CX 2054 at 47-48 (Mooring *Infineon* Dep.) (*in camera*). "[I]n the DRAM business, the only standard is JEDEC." CX 2079 at 118 (Mooring *Micron* Dep.) (*in camera*). *See also* Becker, Tr. 1152-53 (Infineon makes only JEDEC-compliant DRAMS because "that's all our customers are willing to buy").

[416] *See supra* Section IV.B.

[417] *See* Rhoden, Tr. 293-94; Peisl, Tr. 4453; JX 18 at 1-3.

[418] *See* Rhoden, Tr. 297-98 ("working with the customer inside an area like JEDEC . . . when everyone agrees, then they have essentially an automatic market . . . basically a presold customer base just by complying and working with the standard"); Macri, Tr. 4596.

industry. DRAMs must interoperate with complementary components, which provided a compelling incentive to develop DRAM specifications that ensured compatibility[419]. JEDEC provided the necessary mechanism for coordinating the evolution of DRAMs and their complements[420]. Moreover, customers desired a commodity DRAM market whereby multiple DRAM suppliers could supply interchangeable DRAMs; standardization made this possible.[421]

These considerations strongly suggest that the market was likely to coalesce around a standardized choice[422]. Joined with the

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[419] *See, e.g.*, Williams, Tr. 763 (Micron's customers "require that they are able to buy products from multiple sources and that these products interoperate, and JEDEC is the body that sets those standards by which there [is] interoperability"); Calvin, Tr. 994; G. Kelley, Tr. 2387-88; Polzin, Tr. 3943-44 ("It was crucial that we had a common standard that would allow interoperability"), 3972; Peisl, Tr. 4382 (standards "enable [] essentially the whole industry to develop products that work together in more or less a predefined manner"), 4386, 4408-10; McAfee, Tr. 7189-90, 11218.

[420] *See, e.g.*, Calvin, Tr. 994; Polzin, Tr. 3946-47 ("JEDEC was the natural forum and process for resolving the numerous differences."); Peisl, Tr. 4410 ("You have to make sure that your part is fully compliant with all the specifications of the other chips. This is why everybody is working towards the JEDEC specification. That's the common denominator."); McAfee, Tr. 11301-02.

[421] *See, e.g.*, Rhoden, Tr. 298-99; Williams, Tr. 763; Becker, Tr. 1152-53 ("[customers like Dell, IBM, and Compaq] want to be able to buy my parts or Samsung's parts or Micron's parts and use them interchangeably, and through the standards process, they get that benefit"); Sussman, Tr. 1328; Landgraf, Tr. 1692-93; G. Kelley, Tr. 2387-88; Heye, Tr. 3641 ("Apple thought it was very, very important to have multiple suppliers"); Polzin, Tr. 3973; Peisl, Tr. 4408-10; Goodman, Tr. 6013; McAfee, Tr. 7225-26; Farmwald, Tr. 8296; CX 1354 at 5 (1999 Tate presentation stating, "Customers want multiple sourced, compatible DRAMs").

[422] *See* McAfee, Tr. 11228-29. Indeed, outside the litigation context, Rambus recognized this very point. *See* CX 533 at 9 (1989 RamBus Business Plan noting "[t]he DRAM industry's penchant for standardization)"; CX 1284

historical record of the predominant market position of DRAMs compliant with the JEDEC standards, these industry attributes support our finding that JEDEC's choice of standards significantly contributed to Rambus's monopoly power.

3. Rambus's Claims That The Chain of Causation Was Broken

Rambus claims that its course of conduct and its acquisition of monopoly power cannot be linked for four principal reasons.

a. Rambus's Intel Claim

First, Rambus argues (and the ALJ agreed) that Intel's technology choices,[423] not any conduct in which Rambus engaged, caused the monopoly position Rambus enjoyed with respect to SDRAM technologies[424]. If we were to accept this conclusion, implicitly we would be assigning to Complaint Counsel the burden of proving that Rambus's conduct was the *sole* cause of Rambus's monopoly position. This is error as a matter of law.

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at 28 (1989 RamBus Technology Overview stating, "There is real value in having a world DRAM standard").

[423] In late 1996, Intel announced that its future chipsets – the "gatekeeper" or "traffic cop" components that link CPUs with main memory – would support RDRAM exclusively. *See* IDF 1058; Crisp, Tr. 3432-33; Tabrizi, Tr. 9134-35; RX 1532 at 2. By March 1999, however, Intel determined that "a strategy that puts our chipset and value processor line dependent, solely on Rambus is no longer viable." CX 2527 at 2. In June 1999, Intel announced it might discontinue its exclusive support of RDRAM, and two months later, Intel confirmed that it would also support main memory compliant with JEDEC's SDRAM standard. Tabrizi, Tr. 9201-03; CX 1077; CX 2338 at 57 (*in camera*). By October 1999, Intel informed Rambus that it had "been forced to re-architect its chipset roadmap to accommodate additional SDRAM products." CX 2541 at 2; *see* CX 2540 at 1.

[424] RFF 1538-47; ID at 303-04. Rambus did not raise this argument in its appeal or rebuttal briefs to the Commission.

Exclusionary conduct need not be the exclusive cause of the monopoly position. In an equitable enforcement action, it is sufficient that the exclusionary conduct "reasonably appear[s] capable of making a significant contribution to creating or maintaining monopoly power."[425] As Professors Areeda and Hovenkamp explain:

> [B]ecause monopoly will almost certainly be grounded in part in factors other than a particular exclusionary act, no government seriously concerned about the evil of monopoly would condition its intervention solely on a clear and genuine chain of causation from an exclusionary act to the presence of monopoly[426].

Further, as the U.S. Court of Appeals for the District of Columbia Circuit reasoned in *Microsoft*, requiring Section 2 plaintiffs "to reconstruct the hypothetical marketplace absent a defendant's anticompetitive conduct would only encourage monopolists to take more and earlier anticompetitive action."[427]

Moreover, the record does not support Rambus's claim as a matter of fact. Intel first announced and then withdrew exclusive

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[425] United States v. Microsoft Corp., 253 F.3d 34, 79 (D.C. Cir.), *cert. denied*, 534 U.S. 952 (2001), citing language currently appearing at III AREEDA & HOVENKAMP, ANTITRUST LAW, ¶ 651f at 83-84; *see also* Einer Elhauge, *Defining Better Monopolization Standards*, 56 STAN. L. REV. 253, 331-32 (2003).

[426] III AREEDA & HOVENKAMP, ANTITRUST LAW, ¶ 651f at 83. *See also Microsoft*, 253 F.3d at 79 (finding no case standing for the proposition that "as to § 2 *liability* in an equitable enforcement action, plaintiffs must present direct proof that a defendant's continued monopoly power is precisely attributable to its anticompetitive conduct") (emphasis original).

[427] *Microsoft*, 253 F.3d at 79.

support for RDRAM, and RDRAM never became a major factor in the DRAM market[428]. Intel, acting alone, did *not* successfully impart monopoly power on its temporarily anointed choice; nor was the withdrawal of its support the sole reason for the proliferation of SDRAM technologies. Rather, the record shows that JEDEC's standards captured the market. JEDEC adopted standards that included programmable CAS latency and burst length, dual-edged clocking, and on-chip DLL/PLL, and these technologies succeeded. JEDEC did not adopt other aspects of RDRAM, and they became insignificant. Thus, the record shows that JEDEC's adoption made the difference, and significantly contributed to Rambus's acquisition of monopoly power.

b. Rambus's Inevitability/Superiority Claim

Second, Rambus argues (and the ALJ agreed) that any monopoly power it obtained from the incorporation of its technologies into the JEDEC DRAM standards resulted from the superiority of Rambus's technology, not from its conduct. We also reject this claim. To begin with, Rambus and the ALJ assumed that Complaint Counsel had the burden of proof on this claim. That is error. As noted by Professors Areeda and Hovenkamp:

> In addition to proving [monopoly] power, the plaintiff generally has the burden of pleading, introducing evidence, and presumably proving by a preponderance of the evidence that anticompetitive behavior has contributed significantly to the achievement or maintenance of the monopoly. *The defendant may, of course, introduce its own proof*

[428] During the period of Intel's exclusive support, RDRAM accounted for .5% (in 1996), 1.3% (in 1997), 1.6% (in 1998), 1.1% (in 1999), and 3% (in 2000) of DRAM revenues. Rapp, Tr. 10248-49. Its share was 12.5% in 2001, *id*. at 10249, and then fell below 10% by 2002. CX 2112 at 309-10 (Mooring FTC Dep.) (*in camera*).

> *of inevitability, superior skill*, or business justification…."[429]

The court in *Microsoft* essentially reached the same conclusion. There the plaintiff met its threshold burden by showing that Microsoft unlawfully had maintained its monopoly position by "engag[ing] in anticompetitive conduct that reasonably appear[s] capable of making a significant contribution to . . . maintaining monopoly power."[430] The court then inferred causation – ruling, in essence, that the plaintiff had met its burden without a particularized reconstruction of what would have occurred in the but-for world. Rather than requiring the plaintiff "to reconstruct the hypothetical marketplace absent a defendant's anticompetitive conduct," the court explained, "To some degree the defendant is made to suffer the uncertain consequences of its own undesirable conduct."[431]

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[429] III AREEDA & HOVENKAMP, ANTITRUST LAW, ¶ 650c at 69 (emphasis added).

[430] *Microsoft*, 253 F.3d at 79 (citation to Areeda & Hovenkamp treatise omitted).

[431] *Id*. *See also* Morgan v. Ponder, 892 F.2d 1355, 1363 (8th Cir. 1989) ("[w]e need not determine the exact cause of [plaintiffs's firm's] demise. Nor must plaintiffs systematically eliminate all possible non-predatory causes.") (*dictum*). *Cf*. Hecht v. Pro-Football, Inc., 570 F.2d 982, 991 (D.C. Cir. 1977) (holding that *defendants* bear the burden of proof when they seek to avoid charges of monopolization by asserting that their monopoly power results from natural monopoly).

Rambus argues that in a standard-setting case, the plaintiff "must establish that the standard-setting organization adopted the standard in question, and *would not have done so but for* the misrepresentation or omission." RB at 121, citing II HOVENKAMP ET AL., IP AND ANTITRUST, § 35.5b at 35-40 (emphasis added by Rambus). The treatise, however, only states that such analysis should apply when the SSO has (1) "no policy with respect to intellectual property ownership in the standards they promulgate" or (2) "a history of promulgating standards even when they are aware that the proposer owns intellectual property rights in the standard." *Id*. at 35-40 to 35-41. Neither of those factors is relevant to the question of product superiority. Indeed, when the treatise

Rambus argues that, even in light of full disclosure, JEDEC still would have standardized Rambus's technologies, because they were superior to all alternatives on a cost/performance basis. We find that the evidence does not establish that Rambus's technologies were superior to all alternatives on a cost/performance basis[432]. Although Complaint Counsel argue that at least six alternative technologies were available in each of the relevant product markets, we focus, with one exception,[433] on the technologies that Rambus's economic expert, Richard Rapp, analyzed. Because Rambus has failed to prove that its patented technologies were superior to all of these technologies, we need not examine additional alternatives.[434]

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does discuss what Rambus portrays as the fact pattern – when "a standard would have become dominant anyway in a *de facto* standards competition" and the patent "confers an economic monopoly because of the absence of feasible noninfringing alternatives" – the treatise is silent as to the burden of proof. *Id* at 35-41 to 35-42.

[432] Unless stated otherwise, all subsequent references in this section to the superiority of a given technology reflect an overall assessment based on a mix of cost and performance characteristics.

[433] Rapp did not analyze the cost information about toggle mode (a possible alternative to Rambus's dual-edge clocking) because he concluded that this technology's performance suffered above certain clock speeds. Rapp, Tr. 9856-57. We examine toggle mode because Rapp failed to explain why, as an economic expert, he made a judgment based on engineering attributes of this technology, but did not evaluate the performance implications of other technologies.

[434] Rapp excluded two categories of alternatives from consideration on dubious grounds. First, he did not consider any alternative that Donald Soderman, one of Rambus's engineering experts, identified as potentially subject to a Rambus patent. Rapp, Tr. 9831, 10215, 10217. The mere identification of possible patent infringement by Rambus's own expert witness – an engineer who lacked legal training – is an insufficient reason to exclude an alternative technology.

Latency Technology. As discussed above,[435] latency technologies control the length of time between the memory's receipt of a data request and its release of responsive data[436]. The JEDEC DRAM standards incorporated programmable CAS latency technology, which Rambus now claims is covered by its patents. Alternatives available in the early 1990s included fixed CAS latency, blowing a fuse on a DRAM, and dedicated pins.

Rambus compares the variable cost of programmable CAS latency with the variable cost of each of these three alternative technologies. Based on this comparison, Rambus concludes that the alternatives were more costly even when Rambus's royalties were taken into consideration[437]. However, Rambus's cost estimates are unreliable for at least two reasons. First, Rambus assumes, without demonstrating, that alternatives to programmable CAS latency would have provided support for three latency values[438]. Considerable evidence indicates that

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Second, Rapp excluded alternatives that Complaint Counsel's economic expert, McAfee, failed to find commercially viable. Rapp, Tr. 9810, 9841. In only one instance, however, did McAfee actually determine that an alternative was not commercially viable. In other instances, he merely concluded that he lacked sufficient information to reach a judgment one way or the other, or else stated that he was "agnostic" as to an alternative's commercial viability. *See* McAfee, Tr. 7362-63, 7372, 7385, 11354-56. Given that Rambus bears the burden of proving product superiority, McAfee's statements did not justify Rapp's decision to omit such alternatives from his comparison.

[435] *See supra* Section II.A.3.a.

[436] McAfee, Tr. 7348; Horowitz, Tr. 8529-30.

[437] *See* Rapp, Tr. 9813-18, 9831-33.

[438] *See* Geilhufe, Tr. 9578. Rambus's other engineering expert presented general testimony that different latencies provided optimal performance with different bus speeds and that users benefitted from the flexibility afforded by programmable CAS latency. Soderman, Tr. 9347, 9350-51.

JEDEC would have required only one or two latency values if it had standardized one of the alternatives[439]. Second, Rambus fails to take account of ways in which the alternative technologies may have reduced costs[440].

Fixed CAS Latency: A fixed CAS latency part sets a single latency value[441]. Rambus did not present any evidence that this technology had any performance issues. Nevertheless, Rambus argues that fixed CAS latency was not a viable alternative, estimating that it would have increased per-unit costs by three cents for reduced yields and two cents for inventory (while simultaneously reducing per-unit costs by one cent for improved testing)[442]. Rambus potentially overstates the inventory costs because it assumes that three latencies would have been supported – a premise that, as discussed above, is not established by the evidence[443]. Rambus also fails to consider any factors that might

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[439] *See* McAfee, Tr. 11245-48. The record establishes that SDRAMs primarily used only two CAS latency values in main memory. *See* Rhoden, Tr. 394; Lee, Tr. 11004-05, 11063-67, 11097 (testifying that while Micron did produce a part that used a third CAS latency value, this was a small-volume part targeted to the graphics industry). JEDEC standards frequently have required only two latency values. IDF at 1140. In 1991, Samsung advocated a fixed CAS latency of two. JX 10 at 71; Rhoden, Tr. 425-27; Kellogg, Tr. 5099-5101. In 1995, discussion of SDRAM Lite within JEDEC focused on supporting one or two values. Lee, Tr. 6629-32, 11007-08.

[440] Complaint Counsel's engineering expert, Professor Bruce Jacob, testified that shifting to alternatives for programmable CAS latency would have enabled partial elimination of the mode register. *See* Jacob, Tr. 5376-77, 5384, 5388, 5593-95. One of Rambus's engineering experts acknowledged that this simplification could have reduced costs. *See* Soderman, Tr. 9419, 9515.

[441] Jacob, Tr. 5371.

[442] IDF at 1161-62.

[443] Using two latencies, instead of three, would have reduced inventory cost by one cent, which means that the total variable cost increase for this technology would have been three cents. Moreover, according to Complaint

have improved yield,[444] even though its expert's testimony indicated that yield problems tended to be solved "very quickly."[445]

Blowing a Fuse on DRAM: Latency parts can include two CAS latency circuits, each of which can set a different latency value and has a fuse attached[446]. DRAM manufacturers can apply electric or laser technology to blow one of the fuses and prevent the use of the associated latency circuit[447]. Once blown, the DRAM manufacturer would have a fixed latency part with the desired latency value[448]. Rambus's engineering experts testified that electrically-blown fuses were less reliable than laser-blown fuses[449]. However, witnesses from Micron, IBM, and Infineon all

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Counsel's engineering expert, some manufacturers used inventory systems that would have supported the use of fixed CAS latency without any cost increase. Jacob, Tr. 5592-93 (some manufacturers already assigned different part numbers to different latencies).

[444] *See* Geilhufe, Tr. 9577-78.

[445] While explaining how the cost of a DRAM could fall approximately 90% in 12 to15 months, Geilhufe stated that engineers "solve yield problems very quickly. You know, hundreds of engineers work on what is causing yield problems. So we get down the learning curve very, very quickly." *Id.* at 9586-87. *See also* Lee, Tr. 11013 (testimony by Micron's director of advanced technology and strategic marketing that fixed CAS latency parts were less complex than programmable CAS latency and therefore would have improved yields).

[446] Jacob, Tr. 5378-80.

[447] *Id.*

[448] Soderman, Tr. 9354; Geilhufe, Tr. 9585-86.

[449] Soderman, Tr. 9356-57; Geilhufe, Tr. 9581-82 (Intel discontinued using electric fuses on certain products for reliability reasons).

testified that their companies used electric fuse-blowing technology.[450]

Rambus argues that programmable CAS latency was superior, in terms of both cost and performance, to setting CAS latency by blowing fuses[451]. As discussed above, Rambus has failed to establish the need to support three latency values or to demonstrate its predicted yield cost increase. Rambus also failed to rebut the testimony of Complaint Counsel's engineering expert, Professor Bruce Jacob, that computer system OEMs themselves could blow the electric fuses, enabling the DRAM manufacturers to sell a single part,[452] thereby holding down inventory costs.

Dedicated Pins: Dedicated pins can determine latency during DRAM operation[453]. A single dedicated pin can store two CAS latency values, setting one CAS latency under a high voltage and the other latency under a low voltage.[454]

Rambus argues that programmable CAS latency enjoyed cost and performance advantages over dedicated pins. The record does

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[450] *See* Lee, Tr. 11022, 11170 (*in camera*) (Micron had been using such fuses since 1989 and included a substantial number in its SDRAM products); Kellogg, Tr. 5130; Soderman, Tr. 9525-26 (*in camera*); *see also* Jacob, Tr. 5595-96.

[451] Geilhufe testified that this alternative to programmable CAS latency would have increased per-unit costs by three cents for reduced yield, two cents for inventory (covering three latency values), and one cent for certain testing. Geilhufe, Tr. 9584-86, 9589. *See also* Soderman, Tr. 9354.

[452] *See* Jacob, Tr. 5379-81.

[453] Jacob, Tr. 5386-87; Soderman, Tr. 9463.

[454] *See* Jacob, Tr. 5386-87; Polzin, Tr. 3991-92. Rambus's engineering expert agreed that two latencies can be supported with a single pin. Soderman, Tr. 9463.

not establish this argument. First, Rambus again fails to show that any alternative to programmable CAS latency would have had to support three latency values[455]. As discussed above, numerous witnesses disagreed with Rambus on this point. Rambus also fails to rebut testimony that, under most circumstances, the implementation of dedicated pins might have been considerably more cost-effective than Geilhufe's predictions.[456]

In terms of performance, Rambus's engineering expert testified that implementing dedicated pins would have required additional wiring and "quite possibl[y]" could have created a "noise glitch."[457] However, IBM's engineer, Mark Kellogg, testified that such wiring would not have been necessary;[458] and the chief platform architect of Advanced Micro Devices (AMD), Steve Polzin, testified that pin-based solutions "probably could

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[455] Geilhufe testified that the use of dedicated pins would have increased per-unit costs by four cents, reflecting the fact that four dedicated pins would have been required to replace the range of latency values available with programmable CAS latency. Geilhufe, Tr. 9590. An alternative that supported two latency values would have required the addition of at most two pins (given that pins must be added in pairs). *See generally* Polzin, Tr. 3991-92 (use of pins to set latency would "[c]ertainly" be "no more costly" than programmable CAS latency).

[456] According to both Jacob and Lee, many JEDEC-compliant configurations included pins that served no existing function and could be used to set latency. Jacob, Tr. 5387, 11106 ("[n]early all" JEDEC pin-out diagrams had two extra pins available" and "most" had two or more); Lee, Tr. 11030, 11037 (extra pins "almost always" provided); CX 234 at 80-142. If JEDEC had used these extra pins to set latency, there would have been no cost increase for this alternative to programmable CAS latency. Geilhufe's counter-testimony was limited; he argued only that extra pins were unavailable "in the highest density cases." Geilhufe, Tr. 9722-23.

[457] Soderman, Tr. 9361-62.

[458] Kellogg, Tr. 5126-27.

have been made to work just fine."[459] Rambus does not demonstrate that its contrary assertions deserve greater weight.

Burst Length Technology. As discussed above,[460] burst length technology controls the amount of data transferred between the CPU and memory in each transmission. The JEDEC DRAM standards adopted programmable burst length technology, which Rambus now claims is covered by its patents.

Rambus's economic expert, Rapp, analyzed the costs associated with two alternatives to programmable burst length: fixed burst length and burst terminate commands. Rambus claims that programmable burst length was superior to any alternative because it allowed DRAM users to use one part for different types of machines that required different burst lengths, providing important flexibility[461]. However, Rambus assumes that JEDEC would have required more than two burst length values if it had adopted an alternative. The record does not establish that point[462].

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[459] Polzin, Tr. 3991-92.

[460] *See supra* Section II.A.3.b.

[461] *See* Soderman, Tr. 9368-70; G. Kelley, Tr. 2550-51 ("The programmable [burst length] feature allowing you to make that selection when the PC or computer powered up was a nice feature because it allowed you to use devices that were common from multiple suppliers, put them into many different types of machines. . . . One part number fits many applications.").

[462] For example, Intel only used a burst length of four. Polzin, Tr. 3994. AMD, another microprocessor manufacturer, designed its microprocessors based on a single burst length of eight. *Id*.; *see also* Lee, Tr. 11048-54, 11095. JEDEC's preliminary specification for DDR2 SDRAM required only a burst length value of four, Macri, Tr. 4673-74, but subsequently was amended to include a burst length of eight to accommodate AMD. *See* Polzin, Tr. 3994; Lee, Tr. 11048-54, 11095.

Rambus has not shown that additional burst length flexibility was critical to DRAM technology.[463]

Fixed Burst Length: A fixed burst length part sets a single burst length[464]. Rambus argues that fixed burst length technology was not a cost-effective alternative to programmable burst length. According to Rambus, the use of fixed burst length would have increased inventory costs by three cents per unit, while decreasing certain test costs by one cent[465]. However, Geilhufe's inventory cost estimate assumed that four burst length values would have been provided[466]. If, instead, he had assumed that only two burst lengths would have been supported, his entire projected cost increase would have disappeared. Geilhufe also failed to consider cost savings that would have resulted from partial elimination of the mode register.[467]

Burst Terminate Commands: Burst terminate command technology uses long, fixed burst lengths that can be terminated by the memory controller if a shorter burst length is desired[468]. Rambus argues that this technology was not a viable alternative

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[463] JEDEC required burst lengths of four and eight when it first published the SDRAM standard in 1993. *See* JX 56 at 114; Williams, Tr. 801-03; Lee, Tr. 11013-14. Ten years later, the proposed specification for DDR2 SDRAM required the same two burst length values. *See* RX 2099-14 at 21; RX 2099-39 at 20; Soderman, Tr. 9369; Rhoden, Tr. 411-12.

[464] Jacob, Tr. 5398-99.

[465] Geilhufe, Tr. 9593-96.

[466] *See* Geilhufe, Tr. 9595.

[467] *See* Jacob, Tr. 5401-10, 5593-95 (either fixed burst length or a burst terminate command would have enabled elimination of part of the mode register and the circuitry required to initialize it).

[468] Jacob, Tr. 5409-10.

because it could support only a narrow range of burst lengths and therefore would have limited DRAM performance[469]. We are unconvinced. As noted above, Rambus has failed to establish that JEDEC likely would have required more than the two burst lengths supportable with burst terminate commands.

Rambus also argues that the burst terminate command technology causes system inefficiencies[470]. However, several witnesses questioned the significance of these inefficiencies[471]. Furthermore, those witnesses explained that the problems would have been minimized, or avoided, by supporting just two burst length values – such as four and eight[472]. On this record, Rambus has failed to demonstrate serious performance issues with burst terminate command technology.[473]

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[469] Soderman, Tr. 9377 (implementation of burst terminate in DDR2 SDRAM was limited because it could support only burst length values of four and eight); Geilhufe, Tr. 9598 (questioning whether a burst terminate command could support a burst length value of one).

[470] *See* Soderman, Tr. 9374-76 (a burst terminate command causes inefficiencies when a read burst interrupts a write burst or vice versa); Polzin, Tr. 4038-40; CX 392 at 5; CX 415 at 10 ("an internal device timing nightmare").

[471] *See* Jacob, Tr. 5411 (problem not very significant), 5604-06 (might affect bus efficiency by up to 10-15% in a "hypothetical worst case situation[]"), 11109-10 (type of inefficiency at issue is common and inherent in the DDR protocol).

[472] *See* Jacob, Tr. 11142-46; Macri, Tr. 4774-76 (*in camera*) (limiting interruptions to a precise place and under precise conditions makes burst terminate commands "much easier"; "there's a slight burden to the designer, but, you know, in the big scheme of things, this is a trivial thing . . . ."); RX 2099-39 at 20, 63. Even Rambus's engineering expert acknowledged that limiting burst terminate commands to specific conditions avoids timing problems. Soderman, Tr. 9377.

[473] Rambus acknowledges that use of burst terminate commands would not have increased costs. *See* Rapp, Tr. 9826.

Data Acceleration Technology. As discussed above,[474] data acceleration technology determines the speed at which data are transmitted between the CPU and memory. JEDEC's DDR SDRAM and DDR2 SDRAM standards adopted dual-edge clocking technology – a technology Rambus now claims is covered by its patents.

Interleaving ranks on the module, double clock frequency, and toggle mode were some of the alternatives to dual-edge clocking considered by JEDEC. Rambus argues that all three of these alternatives had significant cost and performance limitations. We agree that interleaving ranks on the module had such limitations. However, Rambus has not adequately supported is conclusions regarding double clock frequency and toggle mode.

Interleaving Ranks on the Module: DRAM chips on the memory module can be partitioned into two separate groups that operate on independent system clock signals[475]. This approach – known as interleaving ranks on the module – can double the rate at which data are transmitted between the CPU and memory[476].

Rambus argues that dual-edge clocking enjoyed performance and cost advantages over this alternative. Rambus cites evidence that both Intel and AMD found signal integrity problems during preliminary evaluations of the interleaving-ranks technology[477]. Complaint Counsel do not rebut this evidence. Rambus's engineering expert testified that this alternative offered less flexible memory increments and was not appropriate for every

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[474] *See supra* Section II.A.3.c.

[475] Jacob, Tr. 5426-27.

[476] *Id.*

[477] *See* RX 1976 at 49 (*in camera*); Polzin, Tr. 4035-36.

application[478]. Complaint Counsel offer only a partial rebuttal. The record also shows that interleaving ranks would have resulted in increased costs because it would have required additional technology and hardware[479]. Complaint Counsel again fail to rebut the evidence. Finally, Kentron in 1999 informed JEDEC that it had a patent pending on this technology[480]. Complaint Counsel's economic expert, McAfee, acknowledged that this technology might require royalty payments.[481]

Based on the totality of the evidence, we find that Rambus has established the superiority of dual-edge clocking over this particular technology.[482]

Double Clock Frequency: Double clock frequency involves operating a single-edge clock at twice the frequency of a dual-edge clock[483]. Rambus has failed to demonstrate that this technology was an unacceptable alternative to dual-edge clocking.

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[478] Soderman, Tr. 9389-91.

[479] Soderman, Tr. 9389-91; Goodman, Tr. 6082. Geilhufe testified that the necessary hardware would have increased costs by 25 cents per DRAM. Geilhufe, Tr. 9605-06; *see also* Goodman, Tr. 6046-47, 6083 (each module would have required eight switches at $1 per switch).

[480] *See* CX 150 at 110.

[481] *See* McAfee, Tr. 7404-05.

[482] Because we conclude that Rambus has not established the superiority of dual-edge clocking over double clock frequency and toggle mode, however, a showing of superiority over interleaving ranks matters little. Absent a sufficient showing regarding the remaining alternatives, Rambus has not demonstrated that its monopoly power resulted from the superiority of its technology, rather than from its failure to disclose its patent position.

[483] Jacob, Tr. 5433-34.

Rambus argues that double clock frequency raises clock distribution problems,[484] requires that the internal circuitry operate at twice the speed of a dual-edge clock,[485] and presents electromagnetic interference concerns[486]. However, these performance concerns were rebutted by Micron's Lee, IBM's Kellogg, and Complaint Counsel's expert witness, Jacob[487]. Other testimony portrayed double clock frequency as a technologically satisfactory alternative to dual-edge clocking[488]. TI clearly found double clock frequency desirable: in 1997 it proposed that JEDEC adopt double clock frequency for its standards.[489]

Rambus's expert testified that double clock frequency would increase per-unit costs by 28 cents,[490] including 24 cents for a clock on the dual in-line memory module (DIMM), which he believed would be necessary[491]. However, the record does not support Rambus's assertion that an on-DIMM clock would be

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[484] Soderman, Tr. 9393-94.

[485] Soderman, Tr. 9394-95.

[486] Soderman, Tr. 9395; 9500-01 (asserting that this interference might breach Federal Communications Commission guidelines).

[487] *See* Jacob, Tr. 5433-34, 11115, 11128-29 (slightly reducing voltage mitigates the interference problem); Lee, Tr. 11039-40; Kellogg, Tr. 5182-83 (engineers reduce electromagnetic interference over time).

[488] *See* Kellogg, Tr. 5182, 5184-85; Macri, Tr. 4779-80 (*in camera*) (identifying a "huge" benefit from single-edge clocking).

[489] *See* Lee, Tr. 6711-14; CX 371 at 3.

[490] Geilhufe, Tr. 9610.

[491] Geilhufe, Tr. 9609-10 (speaking in terms of "on-DIMM clock circuitry, possibly on-DIMM PLL/DLL"), 9715 (speaking in terms of an "[o]n-DIMM PLL or DLL circuit, maybe more than a PLL/DLL").

needed[492]. Moreover, considerable evidence suggests that Rambus's estimates for the cost of an on-DIMM clock are unreliable[493]. Finally, Rambus fails to consider design, construction, and testing cost savings that would have resulted from substituting a single-edge clock for Rambus's dual-edge clock.[494]

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[492] Geilhufe neither spoke to anyone to confirm the assumption, nor conducted his own timing analysis. Geilhufe, Tr. 9715, 9729. In contrast, a July 28, 1997 TI proposal for using a high-frequency clock made no mention of an on-DIMM PLL/DLL. *See* CX 371. According to Micron's Lee, this proposal would have required "some changes to the bus topology," but not the addition of clock circuitry or a DLL to the module, and "would not have any additional cost over what we were doing." Lee, Tr. 6713-14, 11040. Indeed, Rambus's other engineering expert, Soderman, did *not* claim that on-DIMM clock circuitry would be needed. *See* Soderman, Tr. 9393-95.

[493] Geilhufe testified that an on-DIMM clock costs $3.80 per module (which, allocated over 16 DRAMs, increases cost 24 cents per unit). Geilhufe, Tr. 9606, 9609-10. Geilhufe acknowledged that 16 DRAMs was "the smallest number of units" over which the cost of on-DIMM clock circuit could be allocated. Geilhufe, Tr. 9605-06. For computers with more than 16 DRAMS, this calculation would overstate the clock-circuitry cost per DRAM.

On cross-examination, Geilhufe was shown a document stating that a Kentron PLL circuit cost $2, rather than the $3.80 that he had assumed. Geilhufe acknowledged that he had unsuccessfully sought cost information about the Kentron PLL. *See* CX 2613 at 7; Geilhufe, Tr. 9718-19. Kentron's CEO, Robert Goodman, stated that a standard PLL costs around $1, Goodman, Tr. 6049. Lee testified that Micron pays only 90 cents for PLLs used on register memory modules. Lee, Tr. 11179 (*in camera*); *see also id.* at 11180-81 (*in camera*) (mounting would add further cost but would be "much less" than the cost of the PLL itself). Geilhufe testified that he "did not review specifically the costs for register [memory modules]," but he did not explain why he had not done so. Geilhufe, Tr. 9719. Rambus seeks to dismiss the PLL cost data by suggesting that the Micron PLLs might not operate at the appropriate frequency, but fails to demonstrate that this was so.

[494] *See* Jacob, Tr. 5420-25, 5433-34.

Toggle Mode: Toggle mode was designed by IBM and uses synchronous technology for outputs but asynchronous technology for inputs[495]. JEDEC considered toggle mode in 1990 and 1991[496]. Rambus's contention that IBM's asynchronous design could not achieve the same performance as synchronous technology[497] was contradicted by other evidence[498]. Rambus's engineering expert also testified that the toggle mode alternative would increase per-unit costs by ten cents due to reduced yields and by two cents for design costs and an additional pin[499]. As mentioned above, Rambus's same expert testified that engineers "solve yield problems very quickly,"[500] which casts doubt on this predicted yield cost increase.

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[495] *See* G. Kelley, Tr. 2514; Jacob, Tr. 5608; CX 34 at 32. With asynchronous technology, the internal clock on each DRAM is not coordinated with the computer system clock. *See* IDF 284; Rhoden, Tr. 368. In contrast, operations in DRAMs that use synchronous technology are coordinated with the system clock, which facilitates rapid communication between the CPU and memory. *See supra* note 14.

[496] *See* CX 251 at 1; CX 314 at 1; CX 315 at 1-3; CX 318 at 1.

[497] *See* Soderman, Tr. 9398-99.

[498] *See* Jacob, Tr. 5417. Rambus introduced evidence that an IBM researcher had described toggle mode as "very big, very hot, and very nonstandard," which are "disastrous" attributes "in the commodity market." *See* RX 2099-7 at 16; Soderman, Tr. 9399-9400. Rambus omits that the researcher also found toggle mode "very fast" and, for some purposes, desirable. *See* RX 2099-7 at 16. All of the researcher's conclusions were confined to the "cumulative effect" of combining toggle mode with a specific "low multibit piecepart architecture" and did notextend to toggle mode more generally. *See id*.

[499] Geilhufe, Tr. 9562-64, 9610-12.

[500] Geilhufe, Tr. 9587.

Clock Synchronization Technology. As discussed above,[501] clock synchronization technology coordinates the timing of a computer system clock with the internal clock in each DRAM. JEDEC's DDR SDRAM and DDR2 SDRAM standards adopted technology that uses on-chip PLL/DLL circuits to align more closely the timing of the two clocks. Rambus now claims that its patents cover on-chip PLL/DLL as implemented in JEDEC-compliant products.

Rapp analyzed four alternatives to on-chip PLL/DLL technology: placing DLL circuits on the memory controller; placing DLL circuits on the memory module; using vernier circuits instead of on-chip PLL/DLL circuits; and relying on the DQS strobe rather than the system clock to align timing[502]. Rambus presents scant evidence on the cost or performance limitations of placing DLL circuits on the memory controller or the module, and therefore fails to meet its burden of demonstrating the superiority of its on-chip PLL/DLL technology. Rambus presents slightly more evidence regarding the performance limitations of vernier circuits, but not enough to sustain its burden of proof. The record as to possible performance limitations of the DQS strobe is mixed.

DLL on the Memory Controller: One alternative to on-chip PLL/DLL involves placing a single DLL circuit on the memory controller to synchronize the DRAM's internal clock with the system clock[503]. Rambus presented no cost evidence relating to this alternative, but it did present expert engineering testimony as

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[501] *See supra* Section II.A.3.d.

[502] *See* Rapp, Tr. 9841-42.

[503] *See* Jacob, Tr. 5445.

to potential performance limitations[504]. Complaint Counsel's expert provided equally plausible rebuttal testimony as to performance, and also identified cost advantages from placing the DLL on the memory controller[505]. Other evidence reflected contemporaneous beliefs that this alternative was workable and desirable. For example, in March 1996, Samsung presented a proposal to JEDEC that involved removing the PLL circuit from the DRAM chip and placing it on the memory controller[506]. In light of the evidence as a whole, Rambus has not carried its burden with respect to this alternative.

DLL on the Module: Another alternative to on-chip PLL/DLLs involves placing one or more DLL circuits on the memory module to synchronize the internal clock on each DRAM with the system clock. Rambus argues that DLLs on the module fail to address timing differences among individual DRAMs,[507] but Jacob countered that DLLs would account for internal delay[508].

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[504] Soderman testified that DLL circuits on the memory controller fail to address timing differences among individual DRAMs and therefore impair high-speed performance. *See* Soderman, Tr. 9405-06.

[505] *See* Jacob, Tr. 5446-47 (placing the DLL on the memory controller could potentially eliminate outbound, inbound, and return delays, and thereby enable operation at higher rates of speed than on-chip DLLs; placing the DLL on the memory controller also would lower testing and manufacturing costs and reduce the power consumption of DDR SDRAMs).

[506] *See* JX 31 at 71; Rhoden, Tr. 513-514; Lee, Tr. 6691.

[507] Soderman, Tr. 9406-10.

[508] Jacob, Tr. 5449.

Rambus estimates that an on-DIMM DLL would cost $3.80[509]. We find that Rambus has failed to adequately support this estimate for the same reasons described above with respect to its estimate of the cost of double clock frequency[510]. Rambus's own economic expert assigned no cost to this alternative to on-chip PLL/DLL because he found a "paucity . . . of information."[511] Although Rambus's expert was certain there would be some additional costs, he determined that "it seemed sensible . . . to simply assume there would be no cost penalty" for purposes of his calculations.[512]

Vernier Circuits: Verniers are a type of circuit that – similarly to PLLs and DLLs – can be placed on a DRAM[513]. Vernier circuits introduce a fixed-amount delay into the DRAM's internal clock to synchronize that clock with the system clock[514]. Rambus claims that vernier circuits do not perform well enough to be viable alternatives to on-chip PLL/DLL[515]. However, several witnesses testified as to the advantages of vernier circuits.[516]

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[509] *See* Geilhufe, Tr. 9613. Both Jacob and Geilhufe testified that on-module DLLs would reduce other costs. *See* Jacob, Tr. 5450 (on-module DLLs reduce DRAM power consumption, costs, and design time); Geilhufe, Tr. 9612-13.

[510] *See supra* note 493.

[511] *See* Rapp, Tr. 9848.

[512] *Id.* at 9878, 10228 (it "seemed fairer in some sense to assume zero").

[513] *See* Jacob, Tr. 5450-51.

[514] *Id.*

[515] *See* RFF 1103-11.

[516] Complaint Counsel's expert stated that verniers potentially could eliminate outbound, internal, and return delays, Jacob, Tr. 5451, and that periodic recalibrations could compensate for fluctuations in temperature and voltage. *Id*. at 5450-53. IBM viewed verniers as the optimal solution for data

Rambus notes that the SyncLink consortium considered designing the SLDRAM chip using verniers, without PLLs or DLLs on the DRAM, but ultimately included both verniers *and* DLLs on the DRAM[517]. Rambus argues that this example demonstrates that verniers were not viable alternatives to on-chip DLL/PLL, but the record offers competing explanations for why Synclink included DLLs in SLDRAM.[518]

Rambus further asserts that Micron and SLDRAM hold patents that cover the use of verniers,[519] but provides no element-by-element analysis – indeed, no evidence beyond the bare text of the patents – to support this contention[520]. Rambus makes no argument about the implications of these patents for the viability of vernier circuits as an alternative to on-chip DLL/PLL.

DQS Strobe: A DQS strobe, also referred to as a data strobe, signals to the memory controller the timing of data capture[521]. In doing so, the DQS strobe purportedly makes it unnecessary to

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capture purposes; IBM implemented verniers on a memory card and promoted the use of verniers at JEDEC meetings. *See* Kellogg, Tr. 5168, 5157, 5153-54. Micron's advanced technology director testified that he had considered verniers to be an acceptable alternative to on-chip DLLs in the 1996-97 time frame. Lee, Tr. 6676-78. A March 1997 VLSI presentation to JEDEC included the use of verniers. JX 36 at 7, 58, 64.

[517] *See* RX 2099-43 at 158; Soderman, Tr. 9412-14.

[518] *Compare* Soderman, Tr. 9414-15 (DLLs were included "to provide a stable reference for input sampling d[el]ay lines" (describing RX 2099-11 at 5)) *with* Jacob, Tr. 5620-21 *and* Lee, Tr. 11044-46 (DLLs were included to provide tight timing on the bus, not to assist in data capture), 11092.

[519] *See* RFF 1105, 1111.

[520] *See* RFF 1111 (citing RX 1701; RX 1479).

[521] Jacob, Tr. 5456-57; Kellogg, Tr. 5158-59.

align the internal clock with the system clock[522]. Rambus presented no cost evidence relating to this alternative technology, but claims that DQS strobes are insufficient for high speed performance[523]. The record contains conflicting evidence, however, suggesting that most JEDEC members believed this technology offered adequate performance[524]. Indeed, DQS strobes are part of the DDR SDRAM standard and were included in proposed specifications for DDR2 SDRAM.[525]

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We conclude that Rambus has failed to meet its burden of demonstrating that JEDEC would have standardized Rambus's technologies even if Rambus had disclosed its patent position. With regard to performance attributes, the testimony of Rambus's experts was offset by conflicting testimony from Complaint Counsel's experts, which called into question the significance of Rambus's performance concerns. In many instances, testimony from JEDEC members and evidence of their prior actions in

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[522] *See* Jacob, Tr. 5456-57; Lee, Tr. 6681-83.

[523] *See, e.g.*, Soderman, Tr. 9415-17; RX 1040 (e-mail prepared by HP JEDEC representative Hans Wiggers explaining his preference for using DLLs at high speeds, in response to a message entitled, "Death to DLLs"); RX 1086 at 1 (*in camera*).

[524] *See* Lee, Tr. 6682-83; Kellogg, Tr. 5158-59; CX 368 (Micron proposal that JEDEC standardize DQS strobes in DDR SDRAM without DLLs); CX 370 (Silicon Graphics proposal that JEDEC standardize data strobes without DLLs); RX 911 at 3 (SyncLink's design included a data strobe); CX 711 at 72 (noting Hyundai's belief that strobes eliminate need for PLLs/DLLs); *cf.* Jacob, Tr. 5456-57 (presenting DQS strobe alternative).

[525] JX 57 at 5; RX 2099-14 at 3; RX 2099-39 at 5. On-chip DLLs can be disabled in DDR SDRAM but are needed for normal DDR operation. *See* Lee, Tr. 6680-81, 6683; CX 234 at 176; JX 57 at 5, 16.

sponsoring the alternative technologies substantially buttressed Complaint Counsel's case.

With regard to costs, Rambus failed to demonstrate that alternatives would have been more expensive. Rambus's economics expert, Rapp, compared the added variable costs associated with the alternatives, based on Geilhufe's cost estimates, to the costs of paying royalties for Rambus's patented technologies. Rapp testified that the least costly alternatives would add .82 percent to the selling price of SDRAM and 5.65 percent to the selling price of DDR SDRAM[526]. He concluded that these costs exceeded Rambus royalties of .75 percent of selling price for SDRAM and 3.5 percent for DDR SDRAM.

Rapp's calculations are fraught with uncertainty and potential for error. They are based on Geilhufe's admittedly imprecise cost estimates. Geilhufe acknowledged that his cost estimates were approximations and he assigned them a sizeable 25 percent margin of error[527]. Yet a 25 percent reduction of Rapp's estimate of the least-costly alternative to SDRAM would bring that estimate well below the level of SDRAM royalties[528]. Moreover, Geilhufe drew many of his estimates from personal experience, without verification by actual cost data or substantiation by

[526] Rapp, Tr. 9831-32, 9850-54. To compare the dollar figures calculated for cost increases with the percentage figures used in stating Rambus's royalties, Rapp projected an average selling price over the expected lifetimes of the products, calculating an average selling price of $4.87 for SDRAM and $5.13 for DDR SDRAM. *Id*. at 9816-17, 9845. Rapp then translated the increased variable costs of the alternatives into a percentage of average selling price. *Id*. at 9816-17, 9845.

[527] *See* Geilhufe, Tr. 9665.

[528] A 25% margin of error for SDRAM equates approximately to .21% of selling price.

supporting record evidence.[529] As to DDR SDRAM, Rapp had to premise his comparisons on projections of future DRAM selling prices and sales volumes.[530]

Rapp's cost estimates drop considerably when revised to reflect different assumptions. For example, recalculating Rapp's estimate of a least-cost alternative to Rambus technologies in SDRAM based on support of two, rather than three, latencies[531] yields total increased cost of .62 percent of selling price, which is less than the .75 percent SDRAM royalty paid to Rambus[532]. Similarly, applying Rapp's methodology to alternatives to Rambus technologies in DDR SDRAM yields costs well below Rambus royalty levels[533]. Moreover, Rapp's calculations, like

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[529] *See* Geilhufe, Tr. 9665-67. Geilhufe acknowledged that he did not seek actual cost data from DRAM manufacturers to verify his cost estimates. *Id*. at 9666-67.

[530] Rapp had to estimate future DRAM prices over the expected life of DDR SDRAM, then weight those prices by estimating sales volumes for each of the future years. *Id.* at 9816-17. Rapp acknowledged that for DDR SDRAM, with limited historical data, the numbers were "mostly estimate." *Id*. at 9845.

[531] *See supra* note 439 and accompanying text.

[532] *See supra* notes 443 and 473 (showing a total cost increase of only $.03 per unit for a combination of fixed CAS latency and burst terminate commands).

[533] If, as the record suggests, no clock-circuitry was needed for double clock frequency, *see supra* note 492, total increased cost for a combination of fixed CAS latency, burst terminate commands, double clock frequency, and a clock synchronization technology would have been seven cents, or 1.36% of DDR SDRAM selling price, which is far below Rambus's 3.5% royalty. (Like Rapp, we assign no added cost for alternative clock synchronization technology.) If clock-circuitry was necessary, the record shows that PLLs sold for between 90 cents and $2. *See supra* note 493. Even based on the *highest* price, the increased cost for the combination of alternatives to Rambus's four patented technologies would have exceeded Rambus's royalty by less than Geilhufe's admitted margin of error.

Geilhufe's estimates, wholly ignore several possibilities for cost reductions from adoption of the alternative technologies.[534]

In sum, Rambus has not shown that all alternatives would have been more costly than its royalties and has not carried the burden of establishing its inevitability/superiority defense.[535]

c. Rambus's Claim that the Link between its Conduct and the Standards Did Not Matter

Rambus backstops its inevitability/superiority claim by asserting that even if its conduct distorted the decisionmaking process at JEDEC, that did not have the effect of harming competition because the interests of JEDEC and it members were not necessarily aligned with the interests of the public as a whole[536]. We reject that argument. As discussed above, JEDEC comprises a broad range of industry participants – including, most importantly, the principal purchasers of both DRAM technologies and DRAMs. The technology choices made by the JEDEC members during the standard-setting process reflect the opinions

[534] *See supra* notes 440, 445, 452, 456, 467, and 494 and accompanying text.

[535] Rambus also argues that the decision of three JEDEC members, with knowledge of Rambus's patents, to develop and manufacture a DRAM chip known as RLDRAM, using programmable CAS latency and burst length and dual-edge clocking, was evidence of the superiority of Rambus's technologies. RB at 59-60. RLDRAM, however, was a high-price, niche product used for specialty applications such as high-speed routers. *See* Bechtelsheim, Tr. 5867, 5870-71 (RLDRAM is priced "several times higher than commodity DRAM"); McAfee, Tr. 7428-31 (showing that RLDRAM sales were very small); Prince, Tr. 9021-22 (omitting mention of RLDRAM when asked to name "any DRAM" that had not been standardized by JEDEC or IEEE). Given RLDRAM's niche nature, a willingness to absorb Rambus royalties for RLDRAM tells little about JEDEC members's preferences for high-volume, low-cost, main memory purposes.

[536] RB at 126-28.

of virtually the entire spectrum of economic actors who are directly impacted by JEDEC's standard-setting decisions. Courts and commentators long have recognized that a fair, honest, and consensus-based standard-setting process can be beneficial to consumers, while substantial competitive concerns may arise when the standard-setting choices of the SSO's participants are distorted[537]. Rambus offers no logical explanation, and cites no supporting precedent, for why the interests of JEDEC and its members would be inconsistent with a procompetitive result, or why we should overlook conduct that distorted the decisions of JEDEC.

Rambus also argues that because standard setting is a "winner-take-all" process, a "but for world" in which Rambus had disclosed its patent position would have been no better than the real world in which JEDEC adopted standards incorporating Rambus's patented technologies[538]. We reject this claim, too. Payment of royalties on memory interfaces has been very much the exception, rather than the rule, in the computer industry[539]. JEDEC could have turned to unpatented alternative technologies in each of the relevant product markets[540]. But even assuming,

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[537] *See, e.g.*, Allied Tube & Conduit Corp. v. Indian Head, Inc., 486 U.S. 492, 500-01, 510 (1988); II HOVENKAMP ET AL., IP AND ANTITRUST, §§ 35.4(a)(4), 35.5.

[538] RB at 126.

[539] *See, e.g.*, Heye, Tr. 3918 (AMD has not paid royalties on memory interfaces to anyone other than Rambus).

[540] *See supra* Section IV.C.3.b. For example, the record contains no suggestion that using fixed CAS latency or fixed burst length, setting CAS latency with fuses or pins, or setting burst length with fuses or burst terminate commands, would have raised patent issues. Nor does the record suggest that using double clock frequency or toggle mode, or relying on data strobes, or putting DLLs on the module or memory controller, would have involved proprietary technology.

arguendo, that JEDEC still would have been willing to adopt Rambus's patented technologies after disclosures had been made, JEDEC and EIA policies would have prohibited the standardization of those technologies unless Rambus committed to licensing on RAND terms[541]. If Rambus had refused to provide the requisite RAND assurances, JEDEC would have been bound by its rules to avoid Rambus's patented technologies.[542]

Alternatively, Rambus might have acceded to JEDEC's licensing policies, and JEDEC members then would have had the benefit of RAND terms. Moreover, JEDEC members at least would have had the opportunity to seek specific royalty

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[541] *See supra* note 285 and accompanying text (citing JEDEC and EIA rules that prohibited the standardization of patented technologies without first securing "all relevant technical information" and assurances that the patent holder will license on RAND terms).

[542] Rambus highlights the decision of a different EIA unit, the Consumer Electronics Association (CEA), to refrain from requiring a RAND assurance from Echelon Corporation. CEA chose not to invoke its licensing rule – potentially permitting Echelon to block a standard by non-compliance – but only after Echelon had announced its intention to block the standard; had engaged in a pattern of efforts over time to halt the standard development effort; and had "been unable to explain or document how the [CEA] standard refer[red] to or require[d] use of any of Echelon's patented technology." RX 2299 at 2; *see* J. Kelly, Tr. 2155-70 (EIA never received a response from Echelon as to how its patent related to the standard under development; CEA "could see no relevance whatsoever between the patent" and its standard-setting work); RX 2300.

Additionally, Rambus claims that JEDEC itself has adopted standards without seeking RAND assurances. Rambus cites only brief notations in JEDEC minutes, indicating that JEDEC approved ballots on which patent issues had been raised. The minutes – generally just one- or two-word notations – do not explain how the patent issues were resolved. They do not establish that the suspected patents actually existed, much less that they applied to the standards. Nor do the minutes indicate whether the patentee ever intended to enforce the patents against JEDEC-compliant products. The minutes do not even state that RAND assurances were not, in fact, offered. *See* JX 15 at 5-6, 8-9,14; JX 25 at 10. Rambus elicited no testimony to clarify these issues.

commitments from Rambus through *ex ante* negotiations; it was not up to Rambus to preclude that possibility[543]. No matter what

[543] Rambus nonetheless asserts that any incentive for the DRAM manufacturers to negotiate royalties *ex ante* would have been "very weak" because, under JEDEC's requirement of "non-discriminatory" terms, all DRAM manufacturers would have been affected uniformly. RB at 71-72. Rambus's sole record support is testimony from its economic expert, David Teece. *Id*. Teece, however, did not deny that DRAM manufacturers possessed incentives to negotiate *ex ante*. Rather, he characterized what he viewed as the practical difficulties of such negotiations as counter-incentives. *See* Teece, Tr. 10349, 10352-54 (stating that "firms have got incentives to do lots of things that they don't do"), 10360 ("because of these costs and difficulties, you're incented not to incur those costs and difficulties [associated with *ex ante* negotiation]"); Elsewhere, Teece has given credence to the incentive to seek *ex ante* negotiations. *See* David Teece & Edward Sherry, *The Interface Between Intellectual Property Law and Antitrust Law: Standards Setting and Antitrust*, 87 MINN. L. REV. 1913, 1993-94 (2003) ("one would expect that, at least when the royalty rates are negotiated ex ante (prior to the adoption of the standard), the patent holder would moderate its royalty demands").

Rambus further contends that an opportunity to negotiate would have been meaningless because it is "all but impossible" to negotiate licenses for patent applications, which are shrouded in uncertainty. RB at 72. If so, then the record demonstrates that Rambus itself achieved the unattainable. Rambus had entered into RDRAM license agreements with three firms by 1992 – despite having only patent applications at that time. *See* RX 538 at 9, 13, 42 (1991 Rambus license to NEC); CX 543a at 11 (1992 Rambus business plan referencing RDRAM licenses with Toshiba, Fujitsu, and NEC); Parties' First Set of Stipulations, Item 11 (Rambus's first issued patent was the '703 patent); CX 1460 at 1 (the '703 patent issued in 1993). Rambus also granted numerous RDRAM, SDRAM, and DDR SDRAM licenses that included patent applications. *See* CX 1600 at 3-4, 6-7 (Hyundai license covering all DRAMs using all or part of Rambus's interface technology); CX 1609 at 3, 6 (Mitsubishi RDRAM license); CX 1617 at 4, 7 (Siemens RDRAM license); CX 1646 at 3, 6 (Micron RDRAM license); CX 1680 at 12, 19, 24 (*in camera*) (Toshiba SDRAM/DDR SDRAM license); CX 1681 at 2-3, 10 (*in camera*) (Hitachi SDRAM/DDR SDRAM license); CX 1683 at 2, 7, 10 (*in camera*) (OKI SDRAM/DDR SDRAM license); CX 1685 at 2, 8, 12 (*in camera*) (NEC SDRAM/DDR SDRAM license); CX 1686 at 2, 7, 11 (*in camera*) (Elpida SDRAM/DDR SDRAM license); CX 1687 at 2, 8, 11-12 (*in camera*) (Samsung SDRAM/DDR SDRAM license); CX 1689 at 2, 7-8, 13-14 (*in camera*) (Mitsubishi SDRAM/DDR SDRAM license).

the specific outcome might have been, the consequences of incorporating Rambus's patented technologies into the standards would have been identified and weighed *before* the standards were adopted, *when Rambus's technologies were competing with the alternatives.* That "but for world" would have been more competitive than the current DRAM marketplace, in which Rambus has monopoly power and can charge whatever royalties it chooses.

d. Rambus's "No Lock-In" Claim

Rambus claims that, even if it did acquire any monopoly power by virtue of the incorporation of the four key patented Rambus technologies into the JEDEC standards, this monopoly power was not enduring because industry participants who practiced the standards were not "locked in." In effect, Rambus claims that there were no barriers to entry to rivals wishing to challenge its monopoly position[544]. The ALJ agreed with this argument, concluding that Complaint Counsel had failed to establish that the DRAM industry had become locked into the JEDEC standards.[545]

Our analysis necessarily is anchored by timing. Lock-in must be assessed as of the time that JEDEC members gained sufficient information to know that Rambus had relevant patents and could

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[544] In contrast, internal Rambus documents described the DRAM industry as susceptible to lock-in. *See, e.g.*, CX 533 at 15 ("Once a DRAM or vend[or] [has] committed to an architecture [it is] unlikely to change"). Rambus's principal engineer, Ware, similarly observed that once a DRAM controller manufacturer begins using a technology – even if not essential to the part – "it becomes more difficult [for that company] to not use it once you have put it in your design"). CX 2115 at 135 (deposition transcript at 134) (Ware FTC Dep.) (*in camera*). *See also* CX 5011 (designated R401155) (1998 Rambus Strategy Update stating, "We should not assert patents against Direct partners until ramp reaches a point of no return (TBD)").

[545] ID at 326-29.

have taken responsive action. JEDEC members lacked knowledge of Rambus's patent position until Rambus filed its first infringement suit against a producer of JEDEC-compliant DRAMs in early 2000. After that, it took some time for the information to be disseminated and evaluated. Each JEDEC member individually needed to explore alternatives – such as licensing and possible design changes – and to determine how it preferred to proceed. At that point, the JEDEC members could begin in earnest to try to agree on a revised standard.[546]

If the DRAM industry had become locked into Rambus's technology by the time that industry participants were apprised of, and able to take action in response to, Rambus's enforcement efforts, Rambus would have achieved durable monopoly power. If, however, the industry still had the practical ability to avoid Rambus's patents by switching to alternative technologies, Rambus would not have obtained durable monopoly power.[547]

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[546] *See, e.g.*, CX 1855 (January 2000 Rambus complaint alleging that Hitachi's SDRAM and DDR SDRAM products infringed four Rambus patents but not identifying the specific claims or technologies at issue). Rambus revealed the nature of its claims to additional JEDEC members during the second quarter of 2000. CX 1109 at 1; CX 1127; CX 1129; CX 1371; CX 2559 at 3; Crisp, Tr. 3435-36. Some JEDEC members quickly recognized the implications of Rambus's patent enforcement efforts. *See, e.g.*, Rhoden, Tr. 532-33; CX 2459 at 1 (indicating that initial work-around proposals regarding programmable CAS latency were presented in March 2000). Other JEDEC members needed additional time before they gained a detailed understanding of Rambus's claims. *See* Krashinsky, Tr. 2782 (stating that he learned that Rambus claimed a patent on programmable CAS latency "midyear or so" in 2000); Polzin, Tr. 3987 (stating that he learned that Rambus claimed patents on technologies used by AMD in "late summer 2000 " and that he conducted an analysis of the Rambus patents at that time). Discussions of possible ways to avoid Rambus's patents on dual-edge clocking for purposes of DDR2 SDRAM began in a JEDEC task group in late October 2000 and reached the JC 42.3 Committee in December 2000. Krashinsky, Tr. 2827-28; Lee, Tr. 6800-02; CX 426; JX 52 at 45-50.

[547] This issue also is one of causation. We could find that Rambus's deceptive course of conduct caused the ensuing anticompetitive effects because JEDEC members had become locked in before they could take effective countermeasures, and thus were unable to avoid Rambus's royalties. If, on the

We find that the DRAM industry was locked into the SDRAM and DDR SDRAM standards by 2000, by which time the JEDEC members were, in theory, in a position to take actions to avoid Rambus's patents. The record does not, however, establish a sufficient causal link between Rambus's exclusionary conduct and JEDEC's adoption of DDR2 SDRAM.

SDRAM. The SDRAM standard was first published by JEDEC in 1993. Rambus claims patent protection over technology from the latency and burst length product markets that was incorporated into the standard.

Complaint Counsel's economic expert, McAfee, described lock-in as "something that grows over time. It's certainly been accomplished by the time that ramp-up starts."[548] McAfee reasoned that before the time DRAM production ramps up, most of the sunk investments in complementary goods must have been made, because "in order to deploy the standardized [DRAM] product in volume, it requires those complementary goods."[549] The progressive accumulation of switching costs gradually contributes to lock-in,[550] and most of the switching costs for both

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other hand, JEDEC members had obtained the necessary knowledge of Rambus's patent position at a time when they still were economically capable of switching technologies – but deliberately chose not to switch – the chain of causation would have been broken, and Rambus's monopoly power would not be attributable to its deceptive course of conduct.

[548] McAfee, Tr. 7444-45. McAfee defined ramp-up as the time "when the volume [of DRAM production] starts to dramatically increase." *Id*. at 7445.

[549] McAfee, Tr. 7445-46 ("they're not going to produce the DRAM for inventory in any large volumes and just sit on them hoping that the complementary goods would be provided in the future").

[550] Switching costs accumulate for manufacturers of DRAMs and of compatible, complementary components as they move from the standard-setting process, to designing chips and products that conform to the standard;

DRAM manufacturers and producers of complements accrue by the time DRAM production ramps up.[551]

Manufacturers ramped up SDRAM production around 1996[552]. SDRAM represented 78.4 percent of DRAM revenues by 2000[553]. DRAM manufacturers, component manufacturers, and systems OEMs testified that changing SDRAM to work around Rambus's patents in 2000 would have presented significant financial and technical difficulties[554]. For example, a witness from

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testing and verifying those designs; building, testing, and qualifying prototypes; and ramping up production on a commercial scale. At each stage the manufacturers make sunk investments that have to be repeated in order to switch to an alternate design. *See* McAfee, Tr. 7444, 7453-54; Shirley, Tr. 4152-54.

[551] *See* Peisl, Tr. 4452-53 (a change to SDRAM that would have been "relatively easy" in 1992 would have been "near impossible" in 2000).

[552] McAfee, Tr. 7442 (ramp-up for SDRAM was "roughly 1995 or 1996"); *id*. at 7446 ("[T]he volume production start[ed] in the 1996-1997 time frame. And so that corresponds to the ramp-up."). SDRAM accounted for less than 2.9% of DRAM revenue in 1995, 4.3% in 1996, and 33.5% in 1997. Rapp, Tr. 10248. Revenues, of course, lag behind production. *See also* Rambus Inc.'s Response to Complaint Counsel's Proposed Findings of Fact, No. 577 (Oct. 1, 2003) ("Although SDRAM represented a relatively small percentage of the DRAM market in 1996, it was certainly 'volume' production.").

[553] Rapp, Tr. 10100-01.

[554] Witnesses from Infineon and Micron, respectively, stated that by 2000 the level of SDRAM development and implementation made substantial changes "very costly and . . . near impossible," Peisl, Tr. 4443-44, and "virtually impossible," Appleton, Tr. 6399. CPU manufacturer AMD stated that changing SDRAM to work around Rambus patents in 2000 would have introduced "a whole host of problems" and would have been "a major, major concern for AMD." Heye, Tr. 3731-34. Cisco Systems explained that changes to memory in 2000 would have imposed "tremendous cost to Cisco to redesign the existing boards and systems Cisco was shipping." Bechtelsheim, Tr. 5881-82. Graphics processor/chipset designer nVIDIA stated that changing SDRAM

HP testified that by the time he learned of Rambus's patent claims in 2000, changing SDRAM to avoid Rambus's patent enforcement efforts would have been "[w]ay too expensive" for HP, whose SDRAM-based server

> was already out, qualified and you know, we sold to customers and you cannot change something like this after it was designed and already shipped, and if you do change it, you're talking about millions and millions of dollars in expenses. It wasn't even going to be considered.[555]

Similarly, an IBM e-mail from April 2000 states, "we have gone way too far with SDR [SDRAM] to even consider talking about"

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in 2000 would have put it through a "painful process" of changing its development plan and redesigning its products. Wagner, Tr. 3862-63.

[555] Krashinsky, Tr. 2782-83. According to the HP witness, providing multiple latencies without using programmable CAS latency would have required changes to the memory module, the motherboard, and the memory controller. *Id.* at 2784-87. He characterized changing programmable CAS latency "a major change," *id*. at 2788, although he indicated that significantly less change would have been required if a fixed CAS latency would have sufficed. *Id*. at 2804-05. Joe Macri of ATI Technologies (ATI) stated that graphics system designer ATI would have incurred "a huge burden" if JEDEC had changed to fixed latency. Macri, Tr. 4764-65 (*in camera*). *See also* Jacob, Tr. 5377-78, 5569 (use of multiple fixed latencies would have caused compatibility problems absent either greater user understanding as to which latency value was needed or development of a more sophisticated memory controller).

switching to fixed latency[556]. Redesigning programmable burst length at that time would have presented similar difficulties[557].

The issue of timing was particularly critical in the DRAM market: the time it would take to redesign SDRAMs and their complements to avoid Rambus's claimed patents would have been prohibitive. Rambus's engineering expert, Geilhufe, indicated that the changes could have been implemented in six to eighteen months[558]. Most of the previous design projects cited in the record indicate that at least a year likely would have been needed[559].

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[556] RX 1626 at 3. When the possibility of changing the SDRAM standard regarding programmable CAS latency was discussed within JEDEC in March 2000, it was "very poorly received" because of lock-in concerns. *See* Rhoden, Tr. 533; Kellogg, Tr. 5196-200; RX 1626 at 2.

[557] *See* Peisl, Tr. 4450-53 (removing programmable burst length in 2000 would have been "nearly impossible," with a "huge impact" on DRAM customers). Using a burst terminate command to set burst length would have required "an enormous amount of redesign"; it may have required "almost a full redesign of the graphics pipeline" and at a minimum would have meant design modifications and a "big disruption of [ATI's] engineering plans." Macri, Tr. 4776-77 (*in camera*). *See also* Jacob, Tr. 5572-73 (switching to fixed burst length would introduce incompatibilities in some systems and would have design implications similar to those for switching to fixed CAS latency).

[558] *See* Geilhufe, Tr. 9615. *See also id*. at 9675 (stating that the changes could be accomplished in a six to twelve month time frame).

[559] *See* Bechtelsheim, Tr. 5884 (Cisco would need at least a year to redesign its products to accommodate new memory standards); Reczek, Tr. 4341-45, summarized in DX 45 (estimating "24 months plus" to design, assemble, test and qualify a new DRAM); Peisl, Tr. 4375-77 (Infineon's reworking of a flawed SDRAM design took approximately one year to repeat various steps); Heye, Tr. 3673-74, 3677-78, 3767-69 (it typically takes AMD between 15 months and two years to design and implement a new chipset and other complementary infrastructure for its microprocessors); Polzin, Tr. 4016-18 (AMD developed a chipset in 9 months and ushered a new motherboard to mass production in 18 months). Rambus cites testimony that Hyundai made the initial transition from SDRAM to DDR in nine months, *see* CX 2108 at 45 (deposition transcript at 237) (Oh FTC Dep.) (*in camera*), but Complaint

However, these estimates do not account for additional delays inherent in the standard-setting process itself. Even assuming perfect knowledge of Rambus's patent claims, manufacturers could not have begun immediately to design and implement responsive changes. The industry would have had to agree on how the standard would be changed[560]. This could have added a year or more to whatever time would have been required to make the changes[561]. Such delays would have meant missed opportunities, which firms in the industry found unacceptable.[562]

Counsel cite documentary evidence indicating that it actually took 15 months, *see* CX 2334 at 20.

[560] *See* Krashinsky, Tr. 2792 ("It has to be defined as a standard and be accepted by the industry as a standard before HP would adopt it and we'll start spending money on doing it."), 2817 (designing can begin once specifications are well enough settled that further changes will not affect the design). No individual DRAM or component manufacturer likely would have been able to adopt non-compliant technology. *See, e.g.*, Macri, Tr. 4768 (*in camera*) (explaining that if graphics system producer ATI changed its controller to conform to an alternative to programmable CAS latency, "we would essentially have a nice paperweight" absent "a device to talk to").

[561] *See* Krashinksy, Tr. 2792 (passing a revised SDRAM standard likely would take "a year or longer even"); Heye, Tr. 3736 ("it's hard to get a consensus of change . . . all of that takes time"); Peisl, Tr. 4453 ("JEDEC is traditionally a very slowly moving consortium . . . because there's so many companies involved . . . so to try to reach consensus at JEDEC, based on my experience, [would] have been incredibly hard and tough."). *See generally* Geilhufe, Tr. 9675 (stating that his time estimate included no allowance for JEDEC consideration).

[562] *See, e.g.*, Wagner, Tr. 3862-63 (explaining that eliminating programmable CAS latency and programmable burst length would have delayed introduction of its graphics products that were "aligned to the timelines" of new computer games: "If we can't release the chip because we have to go redesign for some new technology, then, you know we miss the opportunity to align with this new game . . . ."); Heye, Tr. 3736 ("all of that takes time, and time is something that you don't have in this market"); Shirley, Tr. 4208-09 (*in camera*); Macri, Tr. 4600 ("Time to market is extremely critical in this world"); Kellogg, Tr. 5199; Lee, Tr. 6635, 6684; McAfee, Tr. 7457 ("delay is in itself inherently costly").

We are unpersuaded by Rambus's argument that switching costs were insufficient to establish lock-in. Rambus attempted to quantify the switching costs for DRAM manufacturers to design around its patents on SDRAMs. Rambus's experts testified that a DRAM manufacturer would incur switching costs of $4.3 million to convert from programmable CAS latency and programmable burst length to fixed CAS latency and fixed burst length[563]. Rambus's economic expert, Rapp, argued that $4.3 million is small in relation to the royalties that are being charged by Rambus[564]. The ALJ accepted both Rambus's switching cost estimate and Rapp's conclusions about the economic impact of these costs.[565]

Rambus's $4.3 million figure substantially understates switching costs for three principal reasons. First, Rambus understates or omits certain individual switching cost elements,

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[563] According to Geilhufe, each fixed latency or burst length part would require $100,000 in design costs, $50,000 for photo tools (masks), and $250,000 for qualification. Geilhufe, Tr. 9575-79, 9594-95. Rapp calculated that matching the three latencies and four burst lengths found in JEDEC's SDRAM specifications would require seven new designs, twelve sets of tools, and twelve qualifications, for a total $4.3 million. Rapp, Tr. 9885-86. A lower estimate would flow from Rapp's methodology if the alternative supported fewer latencies or fewer burst lengths than SDRAM. Although we have suggested that two latencies and two burst lengths may have been a reasonable alternative at the time the SDRAM standard was adopted, *see supra* Section IV.C.3.b., subsequent commitments to particular latency or burst length values would have to have been considered in 2000. The Initial Decision, for example, identifies three latency values and three burst lengths in use for main memory or graphics purposes. *See* IDF 1146, 1220, 1223. *See also* RX 1626 at 3.

[564] Rapp, Tr. 9887 ("a small price to pay").

[565] IDF 1652-55.

including mask costs,[566] inventory costs,[567] and opportunity costs[568]. Second, Rambus's figure covers only the switching costs of a single manufacturer at a single plant for a single product. It overlooks – as Rapp acknowledged – that each DRAM manufacturer typically offers components with as many as three densities,[569] and would incur switching costs separately for each

[566] In contrast to Geilhufe's estimate of $50,000 to switch masks, Micron's Brian Shirley testified that the mask set for a specific DDR SDRAM revision design in 2001 cost $334,000, Shirley, Tr. 4205 (*in camera*); that the cost of Micron's mask sets in 2002 ranged from $162,000 to $950,000, *id*. at 4231-32 (*in camera*); that the $162,000 figure would have been the same in 1998-99, *id*. at 4279 (*in camera*); and that multiple mask sets typically were required to maintain full production. *Id*. at 4154 (high-volume products require 25-45 mask sets to run in production), 4234-35 (*in camera*). This last consideration may be very significant in a setting where production already has ramped up; the switching costs necessary to reach the same stage with an alternative technology would have to take production needs into account.

[567] Rambus's experts failed to consider any costs for inventory left unsold at the time of a transition. Such inventories could be substantial: Micron, for example, typically held three weeks of finished goods inventory, Shirley, Tr. 4238 (*in camera*), as well as significant quantities of stock in production. *See* Shirley, Tr. 4153 (estimating that it typically took 45-55 days to move from wafer start to completion). Although a phased transition to a new technology might reduce the loss of inventory, the failure to consider any inventory costs whatsoever appears to be a significant omission.

[568] To undertake a product redesign, DRAM or component manufacturers may need to divert resources, such as engineers, from other projects, potentially delaying the introduction of new products. *See, e.g*., Heye, Tr. 3745; Macri, Tr. 4769 (*in camera*); Appleton, Tr. 6402-03. Rambus takes no account of opportunity costs beyond the salaries of the affected engineers. *See* Rapp, Tr. 10156-58. This fails to consider that engineers' specialized knowledge or team arrangements could make their diversion to a different design project particularly disruptive and could give rise to opportunity costs in excess of their salaries. *See* Shirley, Tr. 4207-09 (*in camera*); McAfee, Tr. 11292-95. Even Rapp acknowledged the possibility that his analysis could miss some surplus value earned by the employer over an engineer's salary. *See* Rapp, Tr. 10158.

[569] *See* Rapp, Tr. 10144.

density[570]. The figure also ignores – as Rapp conceded – that manufacturers with multiple plants might incur some of these costs at each facility[571]. Moreover, Rapp agreed that each affected DRAM manufacturer separately would bear these switching costs and that, as of 1995, there were five to ten major DRAM manufacturers[572]. Multiplying Rambus's $4.3 million estimate – by the number of manufacturers, then by the average number of densities, and then by a figure reflective of the costs that would have to be duplicated in multiple plants – suggests that total costs to DRAM manufacturers could have reached hundreds of millions of dollars. Adjusting for understatements of cost elements would increase that total even more.

Most significantly, Rambus's $4.3 million figure focuses solely on DRAM manufacturers. If JEDEC changed SDRAM, OEMs and manufacturers of complementary components would face substantial switching costs in redesigning their own products[573]. Rambus's estimate omits these costs, although even

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[570] *See* Rapp, Tr. 10143-46 ("whatever the switching costs were . . . would be multiplied by the number of parts that they were starting off with").

[571] *See* Rapp, Tr. 10123. Many DRAM manufacturers own multiple manufacturing facilities. *See, e.g.*, Appleton, Tr. 6267-69 (Micron operates five fabrication facilities); CX 2466 at 2 (Infineon operates three manufacturing facilities).

[572] *See* Rapp, Tr. 10124 ("You could multiply this as needed by the number of manufacturers"), 10146. *See also* CX 2747 at 7 (Micron DRAM Update presenting market shares of 18 DRAM manufacturers in early 1999), 15 (showing 16 DRAM manufacturers remaining in September 1999); Gross, Tr. 2309 (8-10 was a "generous" estimate of DRAM manufacturers in 2003); Appleton, Tr. 6259, 6276-6277 (the DRAM industry had consolidated from approximately 20-25 DRAM manufacturers in the early 1980s to 5-6 major DRAM manufacturers and 2-3 smaller manufacturers as of 2003).

[573] Complementary components – such as memory controllers, memory modules, and motherboards – must be compatible with industry-standard DRAM. *See, e.g.*, Peisl, Tr. 4382, 4410, 4402-03; Macri, Tr. 4589 ("A DRAM alone doesn't really do anything. It needs to talk to other things . . . ."); Heye,

Rapp conceded that the switching costs of component manufacturers could exceed those of DRAM manufacturers[574]. As a consequence, Rambus's estimate wholly disregards a major source of lock-in. For all of the foregoing reasons, we find Rambus's switching cost estimates to be flawed.

Rambus also argues that the DRAM industry was not susceptible to lock-in because DRAM manufacturers "routinely redesign their products" and the entire industry "quickly and seamlessly" switches between sub-standards[575]. These sorts of changes, however, were not comparable to the revisions that would have been required to avoid patented Rambus technologies. The "redesigns" referenced by Rambus generally involved shrinking the dimensions or changing the density of DRAM chips[576]. The sub-standards were merely addenda to JEDEC standards[577]. The changes for most redesigns and for switches

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Tr. 3655-65, 3715; Polzin, Tr. 3954; CX 1075 at 1. For example, changing programmable CAS latency in SDRAM would require HP to redesign and generate "a whole new chip" for its proprietary memory controller. Krashinsky, Tr. 2786. Designing around Rambus's patents may have required changes to the memory controller, the motherboard, the memory module, and the BIOS (basic input/output system, *i.e.*, the built-in software that provides some computer functions without accessing programs from a disk). Heye, Tr. 3733-34, 3742-43; CA A-4.

[574] Rapp, Tr. 10130-31 (adding, however, that component manufacturers' switching costs were likely of the same order of magnitude as those of DRAM manufacturers).

[575] RB at 76-79. *See also* ID at 326-28.

[576] For example, Rambus cites its Proposed Finding 1292, which counts Infineon's various die shrinks and density changes. RB at 76 n. 36; *see also* IDF 1608 (relying on the same evidence). *See* Becker, Tr. 1141 (explaining that density refers to the capacity of a memory chip, the number of pieces or bits of memory it can hold), 1153-54, 1156-57; Reczek, Tr. 4304.

[577] Addenda were add-ons that filled some of the gaps that JEDEC had not specified. Peisl, Tr. 4411-12. They evolved in response to changes in

between sub-standards were more easily accomplished than changes in the DRAM technologies upon which the JEDEC standards were based[578]. More importantly, the types of changes

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speed of operation. *See* Becker, Tr. 1142; Heye, Tr. 3676-77. Large DRAM customers such as Intel sponsored addenda for varied reasons, such as preventing industry participants from developing incompatible parts, *see* MacWilliams, Tr. 4908-09 (explaining that different manufacturers had introduced "very subtle" differences because they had needed to draw upon a series of JEDEC ballots rather than a comprehensive specification) or to add details relevant to their design needs. *See* Shirley, Tr. 4138-40 (describing Intel's PC100 specification as adding "a low level of detail"); Peisl, Tr. 4411.

[578] *See, e.g.*, CX 2108 at 65-66 (deposition transcript at 257-58) (Oh FTC Dep.) (*in camera*) (describing additional design work required for changing circuitry as opposed to conducting a shrink); CX 2334 at 3 (April 1999 Hyundai presentation stating, "PC100 to PC133 – The Same Die as PC100"). An Infineon witness explained that changes in DRAM type took longer than shrinks and, with consideration of the need to make revisions and to repeat steps, often took longer than changes of density. Reczek, Tr. 4304, 4309, 4336-38, 4341-45, 4350-51 (noting that Infineon needed three major revisions to produce a satisfactory DDR SDRAM device). Although the difference in effort required for individual changes was not large, *id*. at 4341-45, a change to the JEDEC-standardized technologies would have required *multiple* revision projects – for example, revising each distinct density of SDRAM and DDR SDRAM – and the total cost would have been some multiple of the cost for an individual change. *See* Rapp, Tr. 10143-44 (agreeing that DRAM manufacturers would "need to make changes to each of the densities of SDRAM or DDR").

Rambus claims that Complaint Counsel's economics expert "admitted that switching cost to avoid Rambus's technologies would be no greater than those routinely absorbed by the industry." RB at 79. McAfee testified that transitions between sub-standards involved the same "categor[ies] of costs" as transitions between JEDEC standards but that "the size of those costs are substantially less" with the former. McAfee, Tr. 7715. He also testified that the cost of changing interface technologies exceeded the cost of die shrinks. *Id* at 7718-19. Rambus also relies on a 1996 Micron e-mail, RX 836 at 2-3, which does not establish that routine changes in chip size, density, and speed involved the same level of cost and difficulty as changes in JEDEC-standardized technologies.

cited by Rambus raised fewer compatibility issues and, therefore, fewer lock-in implications.[579]

Rambus further contends that a switch to alternatives for its technologies "could be "piggyback[ed]" on a redesign, and the ALJ agreed. *See* RB at 76; IDF 1656. The only support comes from Rambus's own expert witnesses. *See* Soderman, Tr. 9418; Geilhufe, Tr. 9615, 9675. Witnesses representing DRAM manufacturers, however, consistently testified that they would not normally combine interface technology changes with redesigns. Infineon's Henry Becker, for example, explained, "Typically when you do a shrink, you like to do it on a product that you're already producing so that you don't create – you don't change too many things at once." Becker, Tr. 1157-58. *See also* Reczek, Tr. 4304-05 (testifying that shrinks, density revisions, and changes to the type of DRAM generally were not combined "because if you mix up two different steps, you might run into severe problems, not finding out what the reason for not functioning in the chip is"); CX 2108 at 65 (deposition transcript at 257) (Oh FTC Dep.) (*in camera*) (stating that Hyundai normally did not change internal circuitry at the time of a shrink).

[579] Redesigns and transitions between sub-standards typically affected the dimensions, amount, and speed of main memory, but were less likely to affect compatibility between main memory and other computer components. The JEDEC interface standards, in contrast, were essential to compatibility. They governed, for example, the timing of release of data, the amount of data, and the speed and alignment of transmissions of data transferred between main memory and other computer components. *Compare* IDF 41; CX 1388 at 8; Peisl, Tr. 4382; Heye, Tr. 3769-71; Bechtelsheim, Tr. 5958; McAfee, Tr. 7718-19 (all highlighting the role of Rambus's technologies as part of an interface and describing the resulting compatibility requirements) *with* Becker, Tr. 1157 (from the customer perspective shrinks don't matter – different sizes "all function the same, he gets the same reliability, same performance"); MacWilliams, Tr. 4887 ("we [Intel] made sure [PC100] was backwards compatible with the 66 megahertz"); Polzin, Tr. CX 2334 at 3 (April 1999 Hyundai presentation stating, "PC100 to PC133 . . . – Using Existing Infrastructure of PC100"); CX 2728 at 2 (December 1998 Micron comments to Dell, stating, "PC133 are backwards compatible with PC100" but for DDR, companies are either "in progress with" or "looking to start" DDR chipset designs). *But cf.* Gross, Tr. 2351-53 (stating variously that she was "not sure," "d[id] not recall," and "believe[d] . . . probably" that PC100 was not backward compatible with PC66).

We find that high direct switching costs, combined with significant delays from revising standards and reworking products, rendered infeasible a change in SDRAM to avoid Rambus's patented technologies in 2000 and conferred durable monopoly power with respect to SDRAM.

DDR SDRAM. JEDEC first published the DDR SDRAM standard in 1999. Rambus claims patent protection over technology incorporated into the standard relating to dual-edge clocking and on-chip PLL/DLL, in addition to the programmable CAS latency and burst length technologies that carried over from SDRAM.

The DRAM industry was significantly locked in to DDR SDRAM by 2000. DRAM manufacturers had begun production of DDR SDRAMs by that time,[580] and their representatives

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[580] Hyundai began mass production of its first DDR chip by March 1999. *See* CX 2108 at 45 (deposition transcript at 237) (Oh FTC Dep.) (*in camera*); CX 2334 at 20. Infineon completed design of its 256-megabit DDR SDRAM at the end of 1999. Peisl, Tr. 4377-79 (explaining that enough was known about DDR SDRAM specifications to begin designing even before the standard was finalized, deferring some aspects until JEDEC made the last of its choices), 4454. Infineon was ramping production of its first DDR product by 2000. *Id.* at 4455. *See also* Crisp, Tr. 3432 (DDR SDRAM was in production in 1998); CX 2726 at 3 (64 Mb DDR SDRAM was available as early as 1998); RX 885A at 1 (Samsung planned to begin mass production of 64 Mb DDR in 1998, and Fujitsu was on a similar schedule). *See generally* CX 2158 at 2 ("Micron Demonstrated DDR in a PC in Fall 99"); CX 2387 (January 1998 IBM e-mail stating that engineering hardware would be available for IBM DDR SDRAMs by the second quarter of 1998, with qualification expected by the end of 1998); G. Kelley, Tr. 2589-91 (IBM began design of DDR SDRAM features selected by JEDEC in late 1996 or the first half of 1997); CX 957 at 2 (LG Semiconductor was working on DDR SDRAM by 1997 – it had assigned its SDRAM team to DDR tasks). DDR SDRAM revenues rose rapidly from .4% of DRAM revenue in 2000 to 5.3% in 2001. Rapp, Tr. 10248-49. Because revenues lag behind production, the market share data are consistent with a significant production ramp in 2000.

consistently testified that changes no longer were feasible[581]. Furthermore, the necessary complementary components had to be in place before substantial sales were possible[582]. AMD, for example, launched a DDR-based system in October 2000; the general manager of its microprocessor unit, Richard Heye, testified that product development had gone too far to change DDR SDRAM by the time that a response to Rambus's patents could have been considered:

> We were planning a launch in the fall of 2000, October. By that time frame, the chipset was for all intents and purposes complete, we were in the validation testing, the DDR, the DIMMs, the memory was done, the DIMMs were being manufactured, the memory folks were actually starting production and waiting for it to start . . . .[583]

Similarly, HP's Krashinsky testified that DDR SDRAM already had been installed in HP server prototypes by about the third

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[581] *See, e.g.*, Peisl, Tr. 4443-44; Appleton, Tr. 6386-87, 6399-401.

[582] *See* CX 2747 at 58-60 (September 1999 Micron DRAM Update stating that DDR controllers for graphics purposes were already available and that multiple chipset vendors were "developing support"); Peisl, Tr. 4455-57 (by 1999-2000 the "customers had progressed in their designing of platforms and have SDR and DDR quite a bit already. There were DDR chipsets available."); McAfee, Tr. 7445.

[583] Heye, Tr. 3737. *See also id.* at 3738 (stating that AMD by 2000 was in the midst of testing DDR memory from all the vendors to ensure that all combinations were going to work with its chipset); CX 2158 at 2 (June 2000 AMD e-mail stating, "AMD powered on the first K7 DDR chipset (IGD4) in Dec 99"). *But cf.* Heye, Tr. 3750 (noting that the infrastructure of DDR-based complements was still developing in 2000 and had not yet been established in the marketplace).

quarter of 2000[584]. Cisco's Bechtelsheim stated that a change in DRAM design in response to Rambus's assertion of patents in 2000 would have imposed "a tremendous cost to Cisco to redesign the existing boards and systems Cisco was shipping to accommodate this new type of memory."[585]

The adoption of programmable CAS latency and burst length in the DDR SDRAM standard raises the same issues as in SDRAM. The cost and delay associated with changing these technologies in SDRAM were equally applicable to DDR SDRAM[586]. Indeed, JEDEC rejected a March 2000 proposal to move to fixed latency in DDR SDRAM, and lock-in concerns were a significant factor.[587]

The DDR SDRAM standard adopted two additional technologies that Rambus now claims to have patented: dual-edge clocking and on-chip PLL/DLL. As to dual-edge clocking, Complaint Counsel's engineering expert testified that redesigning DDR SDRAM to avoid Rambus's patents would have required

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[584] Krashinsky, Tr. 2793. Krashinsky added that if HP had needed to change the chipset that was designed for use with DDR in this server, it would have had to change all of the other products that also used that chipset. *Id*. at 2797.

[585] Bechtelsheim, Tr. 5881. Bechtelsheim estimated that redesigning and requalifying its products in order to accommodate changes in DRAM technology would cost between $500,000 and $1 million for each distinct PC board assembly, so that total cost to Cisco "could approach or exceed $1 billion." *Id*. at 5882.

[586] *See, e.g.*, Wagner, Tr. 3862-63; Peisl, Tr. 4450-53; Macri, Tr. 4764-65 (*in camera*), 4775-77 (*in camera*); Kellogg, Tr. 5196-200. *See generally* Polzin, Tr. 3992-94 ("The problem was, we'd have to change everything in the middle of this production ramp.").

[587] *See* Rhoden, Tr. 532-33 (stating that his proposal to change to fixed latency "was very poorly received within the committee, because there were products shipping in pretty high volume at that time").

changes to the clock chip and the memory controller[588]. Producers of complements and OEMs voiced lock-in concerns. For example, AMD's Polzin testified that, by the summer of 2000, the firm was in the middle of a production ramp for DDR-based controllers and motherboards, and "[i]t would have been impossible for us to stop and change" the dual-edge clocking mechanism[589]. Likewise, Krashinsky explained that HP did not seek a change in JEDEC's DDR SDRAM standard, even after learning of Rambus's patent claims on dual-edge clocking, because HP already had developed a server prototype dependent on DDR SDRAM, HP was "counting on" that standard, and "HP does not want to support changes that will cause a lot of expenses to HP."[590]

The record also establishes that on-chip PLL/DLL was similarly locked-in at this time. AMI-2's Rhoden testified that a proposal in 2000 to change DDR SDRAM to replace on-chip DLL would have been a waste of time in view of "wide industry use and high volume production."[591] Joe Macri of ATI Technologies (ATI), speaking in terms of the subsequent DDR2 SDRAM standard, described removal of on-chip DLL as "not something you can change in a trivial manner," adding, "You really need a gun to your head."[592]

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[588] Jacob Tr. 5413, 5433, 5575-76.

[589] Polzin, Tr. 3980, 3989, 3995-96. *See also* Macri, Tr. 4649-51 (removing dual-edge clocking in 2000 would mean "you're shaking the foundations . . . of the standard and not changing a minor piece").

[590] Krashinsky, Tr. 2793-94.

[591] Rhoden, Tr. 533.

[592] Macri, Tr. 4649. *See also* Jacob, Tr. 5577-78 (compatibility dependent on system design), 5617-18 (compatibility dependent on data arriving at the controller in the appropriate timing window).

Consideration of DDR SDRAM also introduces concerns regarding backward compatibility, especially with reference to dual-edge clocking. Backward compatibility requires that it be economically feasible to produce complementary components capable of supporting both an old and a new generation of DRAM. As witnesses explained, it would have been difficult to design a memory controller that would be compatible both with existing DDR SDRAMs and with any revised version that avoided dual-edge clocking. Micron's Lee termed this "a very difficult design to accommodate,"[593] and ATI's Macri stated that switching to single-edge clocking would have had "a big impact" from "a design point of view."[594] Macri cited the need to retain backward compatibility as a reason why avoidance of Rambus's patents was not feasible.[595]

Rambus argues that, despite this evidence, the industry was not locked into DDR SDRAM in 2000. Rambus provides no estimates of the switching costs for changing dual-edge clocking and on-chip PLL/DLL. Rather, Rambus argues, and the ALJ agreed, that the fact that JEDEC actively considered alternatives for the Rambus technologies in 2000 shows that JEDEC could not have been locked in[596]. We disagree. JEDEC ultimately *rejected* all of the alternatives. In view of the record as a whole, the fact

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[593] *See* Lee, Tr. 6805-06.

[594] Macri, Tr. 4780-81 (*in camera*).

[595] Macri, Tr. 4765, 4767-68, 4773, 4780-81 (all *in camera*). *See generally* Krashinsky, Tr. 2829 (members deemed switching to a single-edge clock "too dramatic" a change).

[596] IDF 1585; RB at 75. The ALJ's finding of fact cited only Complaint Counsel's economic expert. McAfee, however, actually offered much more limited testimony – though he would not "take it as proof," he would not expect JEDEC members to "spend a lot of time discussing technologies in 2000" unless "at least some significant number of members" thought those technologies were commercially viable. McAfee, Tr. 7571.

that the industry was aware of alternatives, but did not switch to them after the adoption of the standard, supports our finding that JEDEC members decided that expenses and delays rendered switching infeasible.

Rambus asserts that switching from DDR SDRAM in 2000 would have been easy. In addition to arguments based on the relative ease of developing new DRAM sizes, densities, and speed grades,[597] Rambus cites an April 2000 Hitachi e-mail stating that "it's not too late for minor, carefully considered changes" to the DDR SDRAM standard[598]. We find that this single e-mail, which addressed only programmable CAS latency,[599] does not accurately reflect the costs and delays described by other industry participants.

In summary, we conclude that lock-in was significant by 2000 with regard to DDR SDRAM and gave rise to Rambus's durable monopoly power.

DDR2 SDRAM. The record does not support a finding that lock-in conferred durable monopoly power over DDR2 SDRAM by 2000. There is evidence that work on DDR2 SDRAM was

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[597] *See supra* notes 575 through 579 and accompanying text.

[598] RX 1626 at 4 (e-mail dated April 10, 2000 by Hitachi employee Bob Fusco stating "For DDR-1, it's not too late for minor, carefully considered changes, so I'm open to either proposal [for eliminating programmable CAS latency]"). At the time this e-mail was written, Rambus recently had commenced suit against Hitachi for willful infringement. CX 1855 at 6, 8-9, 11. It is possible that any post-complaint Hitachi documents memorializing an openness to explore non-infringing alternatives may have been influenced by Hitachi's litigation posture.

[599] The e-mail states nothing about changes to programmable burst length, dual-edge clocking, or on-chip PLL/DLL. RX 1626 at 4. Of course, programmable CAS latency was only one of multiple technologies included in the JEDEC standards and later subject to Rambus's patent claims.

underway by spring 1998[600]. Macri, the JEDEC representative from ATI and chairman of the task group responsible for developing a successor to DDR SDRAM, testified that in April 1998 the group began to engage in the "initial set of discussions on the DDR2 standard" and "things came in, things came out, but by June 2000, we, you know, we had hit a – kind of a stable point."[601] He added that the technical details for the proposed standard were fleshed out between June 2000 and June 2001[602]. JEDEC published the DDR2 SDRAM standard to its members in 2002, but final revisions still were being completed in June 2003.[603]

DDR2-based product design and development was in its early stages by 2000. For example, Micron started design work on DDR2 SDRAMs in late 1999,[604] and its first DDR2 design was "taped out" (*i.e.*, ready for initial transfer to masks) in January 2002[605]. The head of JEDEC's Future DRAM Task Group characterized JEDEC deliberations as fluid until first reaching a "stable point" in June 2000[606]. An April 2000 e-mail by Hitachi's

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[600] Macri, Tr. 4582; CX 376a (March 1998 e-mail announcing "Future dram task group kickoff"); CX 379a (April 1998 Future DRAM Task Group meeting notes).

[601] Macri, Tr. 4598.

[602] *See* Macri, Tr. 4598-99 ("during June of 2000 to June of 2001, we were adding the meat, you know, the real description that an engineer would need to truly understand these – these concepts").

[603] *See* Rhoden, Tr. 411-12; Polzin, Tr. 4046.

[604] Shirley, Tr. 4211 (*in camera*). IBM's Gordon Kelley explained that design work may begin on aspects of the DRAM that are not covered by JEDEC standards. G. Kelley, Tr. 2590.

[605] Shirley, Tr. 4228 (*in camera*).

[606] Macri, Tr. 4598.

Bob Fusco stated, "For DDR-2, we have no legacy to live with, so I like the Micron proposal [to avoid programmable CAS latency]."[607] Complaint Counsel point out that some firms had begun work on DDR2-based products by 2000[608]. However, the scope and extent of DDR2-related efforts is unclear, particularly when one contrasts the unambiguous statements that work had progressed too far to permit change to the SDRAM and DDR SDRAM standards. The evidence suggests that there would have been DDR2 switching costs by 2000, but provides little sense of their magnitude.

Some component manufacturers had started work on DDR2-based complements by 2000. For example, initial JEDEC-level work on the attributes of DDR2-based memory modules began as early as February 1999[609]. However, IBM's Bill Hovis wrote in April 2000 e-mail that, as to DDR2 SDRAM, "[o]bviously here, the situation with the system is that I am not currently locked in . . . ."[610] nVIDIA started work on the first product that it thought might prove DDR2-compatible in late 2000 or early 2001[611]. AMD's Polzin stated that, as of the time of his June 2003

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[607] RX 1626 at 4.

[608] *See*, *e.g.*, Macri, Tr. 4648 (by September 2000 "there were already companies in design on both the DRAM and the systems side"), 4649 (changes at this time would have affected "earliest adopters"), 4650-51; Kellogg, Tr. 5201 (in September 2000 IBM was "moving down the path" of designing its first DDR2-based memory controllers), 5204 (eliminating dual-edge clocking likely would mean "measurable schedule delay" for IBM's memory controller project).

[609] *See* Kellogg, Tr. 5194-95; CX 393.

[610] RX 1626 at 3. The e-mail addressed only issues regarding CAS latency. *Id*. at 3-4.

[611] Wagner, Tr. 3866-67.

testimony, AMD still had not started to develop an infrastructure for DDR2 SDRAM.[612]

Complaint Counsel stress the industry's desire to maintain backward compatibility. Several industry witnesses expressed concerns that changing DDR2 SDRAM to avoid Rambus's patents would have disrupted backward compatibility[613]. One witness testified that an effort to maintain backward compatibility after eliminating dual-edge clocking would have had "a big impact" from the perspective of design and that a desire to maintain backward compatibility was the reason that a sub-unit of JEDEC's task group in October 2000 chose to maintain dual-edge clocking[614]. Contemporaneous documents confirm that backward compatibility was a general goal, but do not conclusively establish that the decisions to retain Rambus's patented technology resulted from that factor[615]. One such example is the minutes of an

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[612] Polzin, Tr. 4043-44.

[613] *See, e.g.*, Macri, Tr. 4678 (changing to fixed latency would have been a disruptive departure from DDR SDRAM base), 4624 (on-chip DLL retained "to keep the backwards compatibility"), 4647-48 (similar), 4649 (Macri did not propose eliminating dual-edge clocking because of backward compatibility concerns), 4678-79 (JEDEC task group thought eliminating dual-edge clocking would have been "disruptive"); Kellogg, Tr. 5192-93 (describing consensus desire in 1998 to achieve an "evolutionary solution" that would sustain backward compatibility); Lee, Tr. 6805-06 (very difficult to design a controller that would be compatible with both dual-edge and single-edge clocking).

[614] *See* Macri, Tr. 4640-42, 4780-81 (*in camera*); *cf.* Krashinsky, Tr. 2829 (JEDEC task group rejected alternative to dual-edged clocking because of "the cost that it would be to implement one versus the other" and because the change in clocking rate would have been too "revolutionary").

[615] These documents show that the Future DRAM Task Group decided early on that the next generation of DRAM should "stay backward compatible if at all possible with DDR," CX 392 at 3, and reflect the desire to provide a "migration path" for producers of controllers, CX 379a at 9. The references, however, are too general to reveal how much those considerations shaped the group's specific technology choices. *See also* CX 132 at 4, CX 379a at 9, and

October 2000 conference call among members of a sub-unit of JEDEC's Future DRAM Task Group, in which elimination of dual-edge clocking was discussed. The minutes conclude, "Single data rate clock is preferred provided that we can make it work."[616] Although "mak[ing] it work" might have encompassed considerations of backward compatibility, the minutes do not expressly state this. Follow-on testimony from the proponent of the change indicated that ultimately "there was not a lot of support," but did not explain the underlying reasons why dual-edge clocking was retained[617]. Based on the existing record, it is difficult to assess how substantially backward compatibility concerns contributed to lock-in in 2000.

In summary, there certainly is evidence that eliminating Rambus's patented technologies from the DDR2 SDRAM standard would have entailed some switching costs for some stakeholders, including, but not limited to, switching costs associated with the desire to preserve backward compatibility[618].

CX 2745 at 7 (all indicating that DDR2 SDRAM should be based on DDR SDRAM); CX 2717 at 8, 13 (March 1998 Transmeta Corporation paper urging that change be "evolutionary" and that backward compatibility with DDR SDRAM be maintained).

[616] CX 426 at 4. Macri subsequently interpreted this to mean that "*if* we were to go and do . . . large-scale change" – which, presumably, would have sacrificed backward compatibility – the preference was for eliminating dual-edge clocking. Macri, Tr. 4690-91 (emphasis added).

[617] *See* Lee, Tr. 6802; JX 52 at 45-50.

[618] These considerations rebut the claim that JEDEC's inclusion of Rambus technologies in DDR2 SDRAM demonstrates that those technologies were superior to all alternatives. *See* RB at 52-59; ID at 322-23. Even Rambus recognizes that revealed preference arguments of this nature require that "all other things be[] equal." RB at 60 n.29. Yet in the case of DDR2 SDRAM, other things were *not* equal. Switching costs were present, and JEDEC's choice, at most, revealed a preference for Rambus technologies over alternatives handicapped by those switching costs. Moreover, uncertainties over the breadth and enforceability of Rambus's patents further blurred the

However, the record shows that JEDEC published the DDR2 SDRAM standard in 2002. The causal link between Rambus' course of conduct and the incorporation of its patented technology in the DDR2 SDRAM standard in 2002 is not as well-defined as it is for the SDRAM and DDR SDRAM standards for several reasons.

First, the record as to the magnitude of DDR2 switching costs is not clear; evidence is imprecise and mixed. On the whole, the record fails to establish that most stakeholders had invested heavily in the DDR2 standard by 2000, when Rambus's intentions and patents were disclosed. Second, the circumstances when JEDEC published the DDR2 standard in 2002 were materially different from what they were when the SDRAM and DDR SDRAM standards were adopted. To begin with, Rambus had disclosed both its patents and its intent to enforce them in 2000, at least two years before the DDR2 standard was published. By 2002, Rambus had largely lost the *Infineon* litigation in the trial court[619]. Consequently, the prospect of substantial royalty costs did not loom as the threat it likely would have posed in earlier years (or the threat that it later posed after the Federal Circuit reversed the *Infineon* district court in January 2003)[620]. Thus, it seems likely that the DDR2 decisions of JEDEC members would have been impacted by a then-current perception that incorporation of Rambus's allegedly patented technology in JEDEC's DDR2 standard would be relatively costless.

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comparisons on which Rambus relies. *See infra* notes 619-620 and accompanying text.

[619] The trial court granted Infineon judgment as a matter of law on May 2, 2001. *See* Rambus, Inc. v. Infineon Techs. AG, 318 F.3d 1081, 1086 (Fed. Cir. 2003).

[620] Even then, patent enforceability remained uncertain.

We conclude that the record does not establish a causal link between Rambus's exclusionary conduct and JEDEC's adoption of DDR2 SDRAM.[621]

4. Rambus' Claim that its Acquisition of Monopoly Power Did Not Matter

Finally, Rambus claims that even if its course of conduct enabled it to acquire monopoly power, it cannot be held liable because Complaint Counsel failed to prove competitive harm in the form of supracompetitive (or "unreasonable") prices for consumers. Rambus argues that the royalties paid by DRAM manufacturers are mere wealth transfers, suggesting that the royalties impose only private costs that are irrelevant to overall social welfare. We reject this argument. It fails to acknowledge any decline in DRAM output that might result from higher DRAM prices. Reduced output would constitute a deadweight loss that decreases overall social welfare and raises competitive concerns – as even Teece, Rambus' economic expert, has acknowledged elsewhere.[622]

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[621] Although we do not, on this record, find durable monopoly power as to DDR2 SDRAM, neither do we rule it out. It is possible that Rambus did, in fact, obtain durable monopoly power over DDR2 SDRAM. We might have found lock-in with respect to DDR2 SDRAM if the record had demonstrated, for example, that backward compatibility concerns were a substantial determinative factor in JEDEC's DDR2 SDRAM standard-setting decisions.

[622] *See* Teece & Sherry, *supra* note 543, at 1931 n.74 (deadweight loss must be weighed against any real-resource cost savings from use of a patented technology).

The ALJ carried that error one step farther. The Initial Decision relies on a purported admission by Complaint Counsel's economic expert, McAfee, that Rambus's conduct "has had no impact on DRAM prices, no effect on consumers, and no effect on the PC market as of the time of trial . . . ." IDF 1053; ID at 323-24. This misses the point of McAfee's testimony. McAfee actually testified that, although he did not believe there had been an impact on DRAM prices "as of today," (1) Rambus's conduct had substantially increased price in the relevant technology markets and (2) "in the long run . . . those

Rambus also argues that its conduct had no anticompetitive effect because its royalty rates have been reasonable[623]. Substantial record evidence shows that Rambus's royalty rates are *not* reasonable[624]. Ultimately, however, we need not rest on this

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royalty costs would be passed on to consumers" with "the effect of lowering output in the downstream DRAM market" and "the effect of increasing the price." McAfee, Tr. 7175-76, 7565-66. McAfee reasoned that, in the short run, DRAM manufacturers face such high fixed costs that they will maximize the output of their facilities irrespective of royalty levels, but in the long run, higher royalty costs will lead to less DRAM production capacity and higher DRAM prices. *Id*. at 7175-76, 7208, 7749-50; *see also* CX 839 at 2 (1995 Crisp e-mail indicating that Hyundai, a DRAM manufacturer, stated "that they pass on license fees and royalties to their customers"); CX 2107 at 140-41 (Oh FTC Dep.) (*in camera*) (Hyundai's DRAM prices to customers were a function of production costs). Neither the ALJ nor Rambus cite any authority for the proposition that a showing of long-run DRAM output reductions and price increases is insufficient to demonstrate competitive harm. Thus, we find no basis in McAfee's testimony for rejecting Complaint Counsel's showing of competitive harm.

[623] RB at 72-74.

[624] A comparison of Rambus royalty rates for DDR SDRAM and RDRAM strongly suggests that Rambus's DDR royalties have not been reasonable. Rambus has charged at least a 3.5% royalty on DDR SDRAM, *see, e.g.*, Rapp, Tr. 9853; CX 1680 at 4 (*in camera*), but generally has negotiated royalties between 1.0% and 2.0% for RDRAM. *See, e.g.*, CX 1592 at 21-23 (Samsung RDRAM License); CX 1646 at 10-11 (Micron RDRAM License); RX 538 at 20-22 (NEC RDRAM License); CX 1612 at 4-5 (Hyundai RDRAM License); CX 547 at 12; CX 1057. (RDRAM royalties cover all four of the technologies at issue in this proceeding, as well as additional proprietary technologies. *See, e.g.*, Horowitz, Tr. 8547-48*;* RX 2183; RX 81 at 8.) Thus, Rambus's 3.5% royalty for DDR SDRAM far exceeds the royalties that were negotiated for RDRAM in a setting in which licensees were aware of Rambus's patent position from the start and, consequently, were sheltered from hold-up.

Rambus attempts to establish the reasonableness of its royalties by comparing them to royalty rates charged for *other* technologies. *See* RB at 73; Teece, Tr. 10422-51. Rambus CEO Tate, however, testified that comparing royalty rates for different technology licenses mixes "apples and oranges" because "[t]he royalty rate for one patent and the royalty rate for another

evidence. Deceptive conduct that confers durable market power by its very essence harms competition, and claims that the offender has not yet behaved like a monopolist provide no shelter[625]. We therefore reject this argument as a matter of law.

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patent, even in the [semiconductor] industry, can vary tremendously based on the value of the patent and the applications involved." CX 2060 at 158 (Tate *Infineon* Dep.) (*in camera*). Rambus fails to provide a basis for treating the referenced licensing arrangements as comparable to licenses for the technologies at issue in the present case. *See* Teece, Tr. 10465-66 (unable to identify any comparative data that involved royalties on DRAM interface technologies), 10644-46, 10659-60 (acknowledging "a lot of heterogeneity" in royalty rates).

Both Rambus and the ALJ highlight a comparison to IBM's patent licensing policy. They state that IBM charged royalties of 1-5% and that Rambus's rates fit well within this range. RB at 73-74; IDF 1548-53; ID at 324-25. The record contains no evidence, however, that IBM's rates reflected royalties for DRAM technologies, or even that the rates stated in IBM's policy ever actually applied. *See* Teece, Tr. 10638-40 (acknowledging that IBM usually cross-licensed without a cash rate). Indeed, even the IBM policy cited by Rambus gave licensees a potentially much less costly option: licensees could choose an 8% royalty based solely on the portion of the selling price attributable to the patented portions of the licensee's product. JX 9 at 24. For a DRAM, in which the four relevant interface technologies are only a small part, the IBM policy might result in only a minimal royalty.

[625] *See* United States v. Microsoft Corp., 253 F.3d 34, 56-58, 76-77 (D.C. Cir.), *cert. denied*, 534 U.S. 952 (2001), quoting Berkey Photo, Inc. v. Eastman Kodak Co., 603 F.2d 263, 274 (2d Cir. 1979), *cert. denied*, 444 U.S. 1093 (1980) ("[I]f monopoly power has been acquired or maintained through improper means, the fact that the power has not been used to extract [a monopoly price] provides no succor to the monopolist."); American Tobacco Co. v. United States, 328 U.S. 781, 809, 811 (1946); *see also* III AREEDA & HOVENKAMP, ANTITRUST LAW, ¶ 651d1 at 80 ("Properly defined monopolizing conduct harms consumers by creating monopoly, increasing its amount, or extending its duration. Thus, an expectation of consumer harm must always be at the logical end of any determination that a particular act 'monopolizes,' and thus satisfies § 2's conduct requirement.").

V. SPOLIATION

Allegations that Rambus engaged in the spoliation of evidence have permeated these proceedings, as well as several private actions relating to Rambus's patent enforcement efforts[626]. Many of the basic facts are not in dispute[627]. Rambus began formulating its document retention policy in early 1998 with the assistance of outside counsel,[628] and adopted a document retention policy in July 1998[629]. Rambus then conducted company-wide "shred days" in September 1998 and August 1999 that involved the destruction of significant quantities of documents[630]. Rambus destroyed a similarly large volume of documents in December 2000 when it moved to a new office building[631]. As part of its document destruction efforts, Rambus deleted e-mails,[632] erased computer

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[626] *See supra* Section II.B. (discussing the relevant procedural history).

[627] Our discussion draws upon evidence developed in the *Infineon* litigation, pertaining to the nature and extent of Rambus's document destruction effort. This evidence was admitted in this proceeding by a reopening of the record. *See* CX 5000-85; DX 500-07; RX 2500-53; *see also supra* Section II.B.1.d.

[628] *See* CX 5005 at 3; CX 5006 (designated R401111); CX 5007; CX 5069 at 11 (deposition transcript at 376) (Karp 2004 *Infineon* Dep.); CX 5068 at 4-5 (deposition transcript at 26-33) (Savage 2004 *Infineon* Dep.); RX 2502 (March 1998 Rambus memorandum regarding "Document Retention Policy Guidance"; RX 2521 at 11-12 (Johnson *Infineon* Dep.).

[629] *See* RX 2503; CX 2102 at 362 (Karp *Micron* Dep.).

[630] Rambus destroyed 185 burlap bags and 60 boxes full of documents on September 3, 1998. CX 5023 (designated R401307); CX 5050 (designated R400812). Rambus destroyed approximately 150 burlap bags of documents on August 26, 1999. CX 5052 (designated R400819).

[631] *See* CX 5053 (designated R400787) (Rambus destroyed 410 burlap bags) .

[632] *See* CX 1264 at 1 ("EMAIL – THROW IT AWAY"); Diepenbrock, Tr. 6230-32.

backup tapes,[633] and instructed its outside patent counsel, Lester Vincent, to clean out his law firm's patent prosecution files so that they mirrored the PTO's file.[634]

The record shows that key Rambus executives and lawyers – including Richard Crisp,[635] Joel Karp,[636] Billy Garrett,[637] Anthony Diepenbrock,[638] and Lester Vincent[639] – destroyed documents. The record also shows that some of these documents related to subject matter pertinent to this proceeding, such as documents regarding Rambus's participation in JEDEC,[640] and Rambus's patent prosecution files[641]. Indeed, Rambus's document destruction efforts were so thorough and effective that neither

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633 *See, e.g.*, CX 5018.

634 *See* CX 5033; CX 5036; CX 5037 (designated BSTZ 41); CX 5069 at 49 (deposition transcript at 540-41) (Karp 2004 *Infineon* Dep.). (BSTZ refers to Bates stamp numbers that appear on this and other exhibits admitted into this record from the *Infineon* litigation.)

635 *See* Crisp, Tr. 3425, 3427-30; CX 2082 at 157-59 (deposition transcript at 841-43) (Crisp *Infineon* Dep.) *(in camera)* ("anything that I had on paper, I basically threw away"); CX 5059 (designated GCWF 3456). (GCWF refers to Bates stamp numbers that appear on this and other exhibits admitted into this record from the *Infineon* litigation.)

636 *See* CX 2059 at 62 (Karp *Infineon* Dep.) (*in camera*); CX 2102 at 115 (deposition transcript at 378) (Karp *Micron* Dep.).

637 *See* CX 5062 (designated GCWF 3422).

638 *See* CX 5064 (designated GCWF 3439); Diepenbrock, Tr. 6235-36.

639 *See* CX 5033; CX 5036; CX 5037 (designated BSTZ 41).

640 *See* CX 5062 (designated GCWF 3416); CX 5078 at 14 (trial transcript at 124), 20 (trial transcript at 146).

641 *See* CX 5033; CX 5036; CX 5037 (designated BSTZ 41); CX 5069 at 49 (deposition transcript at 540-41) (Karp 2004 *Infineon* Dep.).

Crisp nor Rambus's attorneys were able to find certain JEDEC-related documents when they subsequently searched for them.[642]

In order to establish pre-litigation spoliation, Complaint Counsel must show that Rambus destroyed potentially relevant documents at a time when litigation was reasonably foreseeable[643]. The destruction must have occurred with a culpable state of mind[644]. The appropriate remedy in any particular case typically will vary, depending on the spoliating party's degree of fault as well as the extent to which the other party is prejudiced.[645]

In the present case, we need not resolve whether Rambus engaged in spoliation because the record shows, by a preponderance of the evidence, that Rambus engaged in exclusionary conduct. Our findings stand firmly on the evidence that has survived. No remedy for the alleged spoliation is

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[642] *See* CX 1079 at 1 (Crisp October 1999 email: "I'm looking for a copy (paper or electronic) of one of the original DDR datasheets from the 1996/1997 timeframe. Hopefully someone here has one that hasn't fallen victim to the document retention policy :-)"); CX 5078 at 20 (trial transcript at 146).

[643] *See* Silvestri v. General Motors Corp., 271 F.3d 583, 590 (4th Cir. 2001); Byrnie v. Town of Cromwell, 243 F.3d 93, 107-112 (2nd Cir. 2001). *See also* MARGARET M. KOESEL ET AL., SPOLIATION OF EVIDENCE: SANCTIONS AND REMEDIES FOR DESTRUCTION OF EVIDENCE IN CIVIL LITIGATION 4-5 (Am. Bar Ass'n 2000).

[644] Courts have articulated this requirement in varying terms. *See, e.g.*, *Silvestri*, 271 F.3d at 590 ("some degree of fault"), 593 ("deliberate or negligent"); *Byrnie*, 243 F.3d at 108 ("intentional[]," "in bad faith," or "based on gross negligence"), 109 ("knowingly . . . or negligently").

[645] *See* Residential Funding Corp. v. DeGeorge Financial Corp., 306 F.3d 99, 107 (2d Cir. 2002); Schmid v. Milwaukee Electric Tool Corp., 13 F.3d 76 (3d Cir. 1994).

necessary, and we therefore do not undertake the inquiry required to resolve the spoliation issue.[646]

We stress, however, that Rambus's extensive document destruction campaign had the potential to deny the Commission an opportunity to examine thoroughly Rambus's conduct. In some instances, the Commission has relied on evidence that was preserved only fortuitously[647]. If the record in this case had been marginal, while simultaneously containing evidence that Rambus had destroyed potentially relevant documents, we would have pursued the spoliation inquiry to its conclusion and, if appropriate, imposed a remedy. The Commission has a broad range of remedies available to address spoliation, ranging from drawing adverse inferences to ordering that a proceeding be decided against the spoliating party. If spoliation were proven in a future case, the Commission would not hesitate to impose warranted sanctions, in keeping with its fundamental interest in preserving the integrity of its administrative proceedings.

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[646] Accordingly, Complaint Counsel's pending motion for sanctions is denied. Complaint Counsel's Motion for Sanctions Due to Rambus's Spoliation of Documents (Aug. 10, 2005), *available at* http://www.ftc.gov/os/adjpro/d9302/050810ccmosanctions.pdf.

[647] For example, the only sources of Crisp's JEDEC-related e-mails were a hard drive found in Crisp's attic, *see* CX 5075 at 3-5 (deposition transcript at 296-302) (Crisp 2004 *Infineon* Dep.), and an old Rambus server that Crisp had used to transfer e-mails between his Macintosh and PC office computers. *See* Crisp, Tr. 3572-76, 3588-92; CX 5078 at 14 (trial transcript at 124). Likewise, although Rambus's outside patent counsel, Vincent, destroyed most of his Rambus-related files, he retained certain relevant correspondence in his personal files. *See* CX 5066 (designated GCWF 3448). In addition, records that Rambus failed to produce in the normal course of discovery were retrieved from corrupted back-up files in the subsequent *Hynix* litigation, and the Commission was able to add this evidence to this proceeding's record on appeal. *See* CX 5100-16; *see also supra* Section II.B.

VI. CONCLUSION

We find that Rambus engaged in exclusionary conduct that significantly contributed to its acquisition of monopoly power in four related markets. By hiding the potential that Rambus would be able to impose royalty obligations of its own choosing, and by silently using JEDEC to assemble a patent portfolio to cover the SDRAM and DDR SDRAM standards, Rambus's conduct significantly contributed to JEDEC's choice of Rambus's technologies for incorporation in the JEDEC DRAM standards and to JEDEC's failure to secure assurances regarding future royalty rates – which, in turn, significantly contributed to Rambus's acquisition of monopoly power.

Rambus claims that the superiority of its patented technologies was responsible for their inclusion in JEDEC's DRAM standards. These claims are not established by the record. Nor does the record support Rambus's argument that, even after two JEDEC standards were adopted and substantial switching costs had accrued, JEDEC and its participants were not locked into the standards. Rambus now claims that we can and should blind ourselves to the link between its conduct and JEDEC's adoption of the SDRAM and DDR SDRAM standards, as well as to the link between JEDEC's standard-setting process and Rambus's acquisition of monopoly power. These claims fail, both as a matter of fact and as a matter of law. To hold otherwise would be to allow Rambus to exercise monopoly power gained through exclusionary conduct. We cannot abide that result, given the substantial competitive harm that Rambus's course of deceptive conduct has inflicted.

VII. REMEDY

Complaint Counsel seek an order preventing Rambus from enforcing, against JEDEC-compliant products, (1) any patents that claim priority based on applications filed before Rambus withdrew from JEDEC and (2) any existing licensing

agreements[648]. Rambus argues that the Commission lacks authority to impose such a remedy and that the royalty rates set by its existing licenses already satisfy all remedial concerns.[649]

Both parties' arguments regarding remedy have been scant and, for the most part, reflective of opposing extremes[650]. Now that the Commission has found, and determined the scope of, liability, the Commission believes it would exercise its broad remedial powers most responsibly after additional briefing and, if necessary, oral argument devoted specifically to remedial issues.

The accompanying order establishes a briefing schedule. The parties' written presentations directed by the accompanying order will be confined to remedy; re-argument of issues of liability will not be permitted in those presentations. The Commission is most interested in the parties' views regarding possibilities for establishing reasonable royalty rates for JEDEC-compliant products affected by Rambus's exclusionary conduct. The parties should address, without limitation: (1) means for the Commission to determine, based on the existing record, reasonable royalty rates for licensing all technologies applicable to JEDEC-compliant products and covered by relevant Rambus patents; (2)

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[648] CCAB at Attachment 2; CCRB at 95-100.

[649] RB at 128-33.

[650] *See generally* United States v. National Lead Co., 332 U.S. 319 (1947) (rejecting the imposition of compulsory, royalty-free licenses when they were not "necessary in order to enforce effectively the Anti-Trust Act," and finding that "licenses at uniform, reasonable royalties" would be sufficient to accomplish the discontinuance and prevention of the illegal restraints). For discussion of Rambus's existing royalty rates, *see supra* Section IV.C.4.

alternative mechanisms and procedures for determining reasonable royalty rates, such as an independent arbitrator, a special master, or an ALJ; (3) qualitative characteristics descriptive of appropriate relief, against which specific royalty proposals might be evaluated; and (4) appropriate injunctive and other provisions that should be incorporated in the Final Order in this proceeding.

CONCURRING OPINION OF COMMISSIONER JON LEIBOWITZ

I. INTRODUCTION

Rambus's deception of JEDEC and its members injured competition and consumers alike. The company exploited the DRAM standard-setting process for its own anticompetitive ends. JEDEC's members – including Rambus – understood that this information was to be gathered and shared to benefit the industry and its consumers as a whole, yet Rambus effectively transmogrified JEDEC's procompetitive efforts into a tool for monopolization. As detailed in the Commission's Opinion, such conduct meets all the requisite elements of a Section 2 violation.

It would be equally apt, though, to characterize Rambus's conduct as an "unfair method of competition" in violation of Section 5 of the FTC Act. Section 5 was intended from its inception to reach conduct that violates not only the antitrust laws[1] themselves, but also the policies that those laws were

[1] 15 U.S.C. § 12 (a) (2006). The antitrust laws include the Sherman Act and the Clayton Act (as modified by the Robinson-Patman Act). The FTC Act is not an antitrust law.

intended to promote. At least three of these policies are at issue here. From the FTC's earliest days, deceitful conduct has fallen within Section 5's province for its effects on competition, as well as on consumers.[2] Innovation – clearly at issue in this case – is indisputably a matter of critical antitrust interest.[3] In addition, joint standard-setting by rivals has long been an "object[] of antitrust scrutiny" for its anticompetitive uses, notwithstanding its great potential also to yield efficiencies.[4] In this case, Rambus's

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[2] *Cal. Dental Ass'n v. F.T.C.*, 526 U.S. 756, 772 n.9 (1999) ("That false or misleading advertising has an anticompetitive effect, as that term is customarily used, has been long established"). *Cf. F.T.C. v. Algoma Lumber Co.*, 291 U.S. 67, 79-80 (1934) (finding a false advertisement to be unfair competition); *F.T.C. v. Winsted Hosiery*, 258 U.S. 483 (1922) (per Brandeis, J.) (holding that false labeling that misled consumers constituted unfair competition against competitors). *See also F.T.C. v. Gratz*, 253 U.S. 421, 427 (1920) (holding that "unfair methods of competition" do not apply to practices that were "never heretofore regarded as opposed to good morals because characterized by deception, bad faith, fraud, or oppression, or as against public policy because of their dangerous tendency unduly to hinder competition or create monopoly"). Notably, the *Gratz* view of Section 5's scope was later abandoned as *too narrow*. *F.T.C. v. R.F. Keppel & Bros., Inc.*, 291 U.S. 304 (1934).

[3] *See generally* FED. TRADE COMM'N, TO PROMOTE INNOVATION: THE PROPER BALANCE OF COMPETITION AND PATENT LAW AND POLICY (Oct. 2003), *available at* http://www.ftc.gov/os/2003/10/innovationsrpt.pdf.

[4] *See, e.g., Allied Tube & Conduit Corp. v. Indian Head, Inc.*, 486 U.S. 492, 500-01 (1988) (holding that "private standard-setting associations have traditionally been objects of antitrust scrutiny" because of their potential use as a means for anticompetitive horizontal agreements, but that the associations' "potential for procompetitive benefits" has influenced "most lower courts to apply rule-of-reason analysis to product standard-setting by private associations"). *See also* TIMOTHY J. MURIS, BUREAU OF CONSUMER PROT., FED. TRADE COMM'N, STAFF REPORT ON THE STANDARDS AND CERTIFICATION RULE 9 (1983) ("Standard setting can be misused to exclude competitors unreasonably, injuring consumers. The Commission can pursue anticompetitive restraints as unfair methods of competition, using a rule of reason approach, or as unfair acts or practices under the Commission's

deceptive conduct distorted joint standard-setting decisions and innovation investments in ways that seriously injured the operations of the competitive market to the detriment of consumers; it thereby transgressed the policies and spirit of the antitrust laws in all three respects. While respondent's behavior before JEDEC might well have been challenged solely as a pure Section 5 violation, Complaint Counsel did not litigate this theory before the administrative law judge. Thus, I write separately to discuss and reemphasize the broad reach and unique role of Section 5.

I also address the scope of Section 5 because some commentators have misperceived the Commission's authority to challenge "unfair methods of competition," incorrectly viewing it as limited, with perhaps a few exceptions, to violations of the Sherman and Clayton Acts.[5] Others are unclear just how far Section 5 can reach beyond the antitrust laws.[6] Regardless of the reasons for these cramped or confused views, a review of Section 5's legislative history, statutory language, and Supreme Court interpretations reveals a Congressional purpose that is unambiguous and an Agency mandate that is broader than many realize.

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unfairness protocol, in each case weighing the benefits and costs of the challenged activity.").

[5] *See, e.g.*, Richard A. Posner, *The Federal Trade Commission: A Retrospective*, 72 ANTITRUST L.J. 761, 765-66 (2005) ("It used to be thought that 'unfair methods of competition' swept further than the practices forbidden by the Sherman and Clayton Acts, and you find this point repeated occasionally even today . . . .").

[6] Antitrust Law Special Comm., Am. Bar Ass'n, REPORT ON THE ROLE OF THE FEDERAL TRADE COMMISSION, 58 ANTITRUST L.J. 53, 63-64 n.11 (1989) (observing that "[a]lthough it is well established that Section 5's ban on 'unfair methods of competition' permits the FTC to proscribe conduct not reached by prevailing interpretations of the Sherman and Clayton Acts, there is a debate about how far Section 5 reaches beyond those Acts.").

The Commission, in my view, should place greater emphasis on developing the full range of its jurisdiction and making it more clear to the bar, the public, the business community, and potential antitrust malefactors what Section 5 embraces and what it does not. Although the Commission has not left fallow its Section 5 jurisdiction to challenge conduct outside the antitrust laws, neither has the Agency fully exercised or explained it. In discussing Section 5 in the context of Rambus, I hope to encourage the Commission (and its staff) to develop further and employ more fully this critical and unique aspect of our statutory mandate. If we do, benefit will accrue both to consumers and to competition.

II. THE MANDATE UNDERLYING SECTION 5

A Legislative History

Debates regarding the need for, and nature of, a "federal trade commission" roiled for more than a decade prior to its creation in 1914.[7] These debates involved four of the most brilliant minds of the time – Roosevelt, Taft, Wilson, and Brandeis – and coalesced into a significant issue in the election of 1912.[8] One of the flashpoint events that led Congress to act was the *Standard Oil* case, in which the Supreme Court in 1911 adopted "rule of reason" analysis for the Sherman Act's prohibition on "restraints

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[7] The FTC's predecessor, the Bureau of Corporations, was created in 1903.

[8] Marc Winerman, *The Origins of the FTC: Concentration, Cooperation, Control, and Competition*, 71 ANTITRUST L.J. 1 (2003) (providing the most thorough examination of the FTC's creation and the competing forces and philosophies that gave the agency its ultimate form and powers). *See also* Robert Lande, *Wealth Transfers as the Original and Primary Concern of Antitrust: The Efficiency Interpretation Challenged*, 34 HASTINGS L.J. 65 (1982); Neil Averitt, *The Meaning of 'Unfair Methods of Competition' in Section 5 of the Federal Trade Commission Act*, 21 B.C. L. REV. 229 (1980).

of trade."[9] Many within and outside of Congress viewed the Supreme Court's reasonableness test as judicial invention – what some more recently would term "legislat[ing] from the bench"[10] – that threatened both to undermine Congress's aim in passing the Sherman Act and to yield inconsistent applications from court to court.[11]

Congress's bipartisan reaction was to create an administrative agency with antitrust expertise, an enforcement mandate *more expansive than that of the antitrust laws*, and the structure and flexibility to identify, analyze, and challenge new forms of "unfair methods of competition" as they developed.[12] Legislators in the Congressional debates repeatedly expressed these goals. Senator Robinson, for example, indicated that "unfair methods of competition" encompassed practices that constituted "unjust, inequitable, or dishonest competition."[13] Senator Pomerene and Senator Thomas both stated that the proposed Act would authorize the Commission to determine whether certain forms of business conduct constituted unfair methods of competition, regardless of whether that conduct involved a restraint of trade.[14]

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[9] *Standard Oil Co. v. U.S.*, 221 U.S. 1 (1911).

[10] *See, e.g.*, 140 CONG. REC. 10,109 (1994) (statement of Sen. Thurmond during Senate hearing on nomination of Justice Breyer).

[11] *See, e.g.*, 47 CONG. REC. 1,225 (1911) (statement of Sen. Newlands).

[12] Another, related Congressional response, also in 1914, was passage of the Clayton Act, 15 U.S.C. § 12, which, *inter alia*, contained specific provisions regarding discriminatory pricing, tying, stock acquisitions, and interlocking directorates.

[13] 51 CONG. REC. 12,153 (1914) (statement of Sen. Robinson).

[14] 51 CONG. REC. 12,161 (1914) (statement of Sen. Pomerene); 51 CONG. REC. 12,197 (1914) (statement of Sen. Thomas). In Senator Cummins's view, the discretion and judgment of the Commission should not even be subject to judicial review. 51 CONG. REC. 12,151 (1914) (statement of Sen. Cummins).

Senator Newlands, the Chairman of the Senate Commerce Committee, responded to concerns about this process by explaining that "[y]ou can not [sic] take a body of five men, intelligent men, composed as this body will be of lawyers, economists, publicists, men engaged in industry, who will not be able to determine justly whether the practice is contrary to good morals or not."[15]

Section 5 was not enacted merely to mirror the antitrust laws. Senator Cummins, one of the bill's main proponents, squarely addressed this issue on the Senate floor when he responded to the question, "why, if unfair competition is in restraint of trade, [are we] attempting to add statute to statute and give a further remedy for the violation of the [Sherman Act]?" Senator Cummins replied that the concept of "unfair competition" seeks:

> to go further [than "restraints of trade"] and make some things offenses that are not now condemned by the antitrust law. That is the only purpose of Section 5 – to make some things punishable, to prevent some things, that can not [sic] be punished or prevented under the antitrust law.[16]

Echoing this point, he later described Section 5 as new substantive law that would involve the Commission in activities beyond the simple enforcement of antitrust law.[17] Many other

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[15] 51 CONG. REC. 12,154 (1914) (statement of Sen. Newlands). Had he made his comment in more recent times, Senator Newlands doubtlessly would have phrased it to apply to a body of five men and women.

[16] 51 CONG. REC. 12,454 (1914) (statement of Sen. Cummins). Senator Cummins, an "insurgent" Republican, was a member both of the Commerce Committee, which prepared the Commission bill, and the Judiciary Committee, which prepared the bill that became the Clayton Act. He authored the "Cummins Report," which provided critical support for the Commission bill and helped influence its ultimate content.

[17] 51 CONG. REC. 12,613 (1914) (statement of Sen. Cummins).

legislators similarly expressed their intent and understanding that Section 5 would extend beyond the Sherman Act.[18]

While the Act's legislative history makes its "sweep and flexibility . . . crystal clear,"[19] the plain language of the statute further bolsters this conclusion. If Congress had wanted Section 5's reach to be merely coterminous with that of the Sherman Act, it easily could have written the statute accordingly. There would have been no logic in doing so, of course, since the Sherman Act already existed.

In drafting Section 5, Congress did not mimic the Sherman Act or try to enumerate a list of unfair practices. Rather, the Senate Report explains, Congress left it to the Commission "to determine what practices were unfair" because "there were too many unfair practices to define, and after writing 20 of them into law it would be quite possible to invent others."[20] To ensure there would be no misunderstanding, Congress carefully crafted the

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[18] *See, e.g.*, 51 CONG. REC. 14,333 (1914) (statement of Sen. Kenyon, remarking that the proposed federal trade commission "can take hold of matters that not in themselves are sufficient to amount to a monopoly or to amount to restrain [sic] of trade"); 51 CONG. REC. 14,329 (1914) (statement of Sen. Nelson, stating that the FTC Act "can be used in a lot of cases where there is no trust or monopoly"); 51 CONG. REC. 12,135 (1914) (statement of Sen. Newlands, observing that although "[a]ll agree that while the Sherman law is the foundation stone of our policy on [appropriate business conduct], additional legislation is necessary").

[19] *F.T.C. v. Sperry & Hutchinson Co.*, 405 U.S. 233, 241 (1972). *See also F.T.C. v. Cement Inst.*, 333 U.S. 683, 693 (1948) ("All of the committee reports and the statements of those in charge of the Trade Commission Act reveal an abiding purpose to vest both the Commission and the courts with adequate powers to hit at every trade practice, then existing or thereafter contrived, which restrained competition or might lead to such restraint if not stopped in its incipient stages."); *Id.* at 693 n.6 (offering many citations to the Congressional Record).

[20] S. Rep. No. 63-597, at 13 (1914) (internal quote omitted).

term "unfair methods of competition" to distinguish it from the narrower common-law concept of "unfair competition."[21] Thus, Congress made clear its intent, both to those who would later enforce Section 5 and those who would be subject to its strictures, that this provision was not confined to the collection of violations then-recognized in antitrust or common law, but rather conferred a broader and more adaptable authority on the Commission.[22] Now, as more fully developed by the courts and Commission, Section 5 permits the FTC to challenge conduct outside the bounds of the antitrust law that (a) violates the policies that underlie the antitrust laws or (b) constitutes incipient violations of those laws.

B Supreme Court Interpretations

The FTC's statutory mandate comes not just from the legislature of almost a century ago. For more than 70 years, an unbroken line of Supreme Court opinions has interpreted Section 5 as encompassing a broader array of behavior than the antitrust laws.[23]

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[21] H.R. Rep. No. 63-1142, at 19 (1914) (Conf. Rep.) ("There is no limit to human inventiveness in this field. . . . If Congress were to adopt the method of definition, it would undertake an endless task."); *Keppel*, 291 U.S. at 310-12, n.2 (stating that the Conference Committee substituted the phrase "unfair methods of competition" for "unfair competition" to ensure that the scope of the FTC Act would not be "restricted to those forms of unfair competition condemned by the common law.").

[22] *See Keppel*, 291 U.S. at 310 ("It would not have been a difficult feat of draftsmanship to have restricted the operation of the Trade Commission Act to those methods of competition in interstate commerce which are forbidden at common law or which are likely to grow into violations of the Sherman Act, if that had been the purpose of the legislation.").

[23] *See Sperry & Hutchinson*, 405 U.S. at 244 (commenting that, after *Keppel*, "unfair competitive practices were not limited to those likely to have anticompetitive consequences after the manner of the antitrust laws; nor were unfair practices in commerce confined to purely competitive behavior."). Prior to the 1934 *Keppel* case, Supreme Court opinions tended to articulate a

Most recently, the Court in *Indiana Federation of Dentists* ("*IFD*") observed that the standard for "unfairness" under the FTC Act is, "by necessity, an elusive one, encompassing not only practices that violate the Sherman Act and the other antitrust laws, but also practices that the Commission determines are against public policy for other reasons."[24]

The Court in *IFD* relied on *Sperry & Hutchinson*, the Court's most recent, substantive analysis of Section 5's history and breadth. In *Sperry*, the Court answered two critical questions:

> First, does § 5 empower the Commission to define and proscribe an unfair competitive practice, even though the practice does not infringe either the letter or the spirit of the antitrust laws? Second, does § 5 empower the Commission to proscribe practices as unfair or deceptive in their effect upon consumers regardless of their nature or quality as competitive practices or their effect on competition? We think the statute, its legislative history, and prior cases compel an affirmative answer to both questions.[25]

Drawing on its review of Section 5's legislative history and other authority, the Court concluded that the Commission:

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narrower view of Section 5's range. *See, e.g.*, *F.T.C. v. Raladam Co.*, 283 U.S. 643 (1931); *Gratz*, 253 U.S. 421. Notably, however, even *Gratz*, which was authored only six years after the FTC's creation, emphasized Section 5's use to redress conduct such as that at issue in the present case, namely, "deception, bad faith, fraud, or oppression, or [practices that are] against public policy because of their dangerous tendency unduly to hinder competition or create monopoly." *Id.* at 427.

[24] *F.T.C. v. Ind. Fed'n of Dentists*, 476 U.S. 447, 454 (1986) (citations omitted).

[25] *Sperry & Hutchinson*, 405 U.S. at 239.

> does not arrogate excessive power to itself if, in measuring a practice against the elusive, but congressionally mandated standard of fairness, it, like a court of equity, *considers public values beyond simply those enshrined in the letter or encompassed in the spirit of the antitrust laws*.[26]

Supreme Court opinions prior to *IFD* expressed similar views. In *F.T.C. v. Brown Shoe Company*, the Court stated:

> [t]his broad power of the Commission is particularly *well established with regard to trade practices which conflict with the basic policies of the Sherman and Clayton Acts* even though such practices may not actually violate these laws. . . .[27]

and further quoted *F.T.C. v. Motion Picture Advertising Service Company* for the proposition:

> [i]t is . . . clear that the Federal Trade Commission Act was designed to supplement and bolster the Sherman Act and the Clayton Act . . . *to stop in their incipiency acts and practices which, when full blown, would violate those Acts* . . . as well as to condemn as "unfair methods of competition" existing violations of them.[28]

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[26] *Id.* at 244 (emphasis added).

[27] *F.T.C. v. Brown Shoe Co.*, 384 U.S. 316, 321 (1966) (emphasis added).

[28] *Id.* at 322 (quoting *F.T.C. v. Motion Picture Adv. Serv. Co.*, 344 U.S. 392, 394-95 (1953) (emphasis added)). *See also F.T.C. v. Texaco*, 393 U.S. 223, 225-26 (1968).

I know of no Supreme Court case in the past 70 years that disagrees with these goals, contracts this scope, or disputes the flexibility and elasticity inherent in Section 5.[29]

C Important Appellate Cases

In the early 1980s, courts of appeals rebuffed FTC efforts to apply Section 5 in three frequently-cited cases: *Official Airline Guides*, *Boise Cascade*, and *Ethyl*.[30] Each of these cases was decided before *IFD*, with its reliance on *Sperry & Hutchinson's* reiteration of Section 5's breadth. These appellate opinions support the propositions that Section 5 does not condemn pure conscious parallelism (*i.e.*, unaccompanied by any "plus factors") or conduct justified by an independent, legitimate business purpose. The decision in each, however, turns primarily on an evidentiary failure to demonstrate that the challenged conduct

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[29] *See, e.g., Atl. Ref. Co. v. F.T.C.*, 381 U.S. 357, 369 (1965) ("As our cases hold, all that is necessary in § 5 proceedings to find a violation is to discover conduct that 'runs counter to the public policy declared in the' Act."); *Cement Inst.*, 333 at 694 ("[A]lthough all conduct violative of the Sherman Act may likewise come within the unfair trade practice prohibitions of the Trade Commission Act, the converse is not necessarily true. It has long been recognized that there are many unfair methods of competition that do not assume the proportions of Sherman Act violations."); *Fashion Originators' Guild of Am. v. F.T.C.*, 312 U.S. 457, 466 (1941) ("Nor is it determinative in considering the policy of the Sherman Act that petitioners may not yet have achieved a complete monopoly. For 'it is sufficient if it really tends to that end and to deprive the public of the advantages which flow from free competition.' . . . [I]t was the object of the Federal Trade Commission Act to reach not merely in their fruition but also in their incipiency combinations which could lead to these and other trade restraints and practices deemed undesirable."); *Keppel*, 291 U.S. at 312 n.2 (concluding from a detailed review of the legislative history that Congress wanted "unfair methods of competition" to confer a broad, flexible mandate that would exceed the "forms of unfair competition condemned by the common law").

[30] *Official Airline Guides, Inc. v. F.T.C.*, 630 F.2d 920 (2d Cir. 1980); *Boise Cascade Corp. v. F.T.C.*, 637 F.2d 573 (9th Cir. 1980); and *E.I. du Pont de Nemours & Co. v. F.T.C.*, 729 F.2d 128 (2d Cir. 1984) [hereinafter *Ethyl*].

constituted an effort to acquire market power, tacitly collude, or manipulate price for anticompetitive purposes. *None* of these cases significantly constrains the FTC's authority to apply Section 5 to violations of the policies that underlie the antitrust statutes or that cause actual or incipient antitrust injury.

In *Official Airline Guides ("OAG")*, the FTC challenged the refusal by a monopolist/publisher of airline schedules to include in its compendium schedules of commuter airlines. This refusal to deal was discriminatory, unjustified, and injurious to commuter airlines in their competition with certificated airlines. The monopolist, however, did not act coercively, did not compete in the commuter airlines' market, where the antitrust injury occurred, and did not seek or have any prospect of gaining power in that market. Although the court acknowledged that FTC determinations as to what practices constitute an "unfair method of competition" deserve great weight,[31] it declined to uphold the Commission's order. Rather, it opted to characterize the respondent's action as a unilateral refusal to deal protected by *United States v. Colgate & Company*.[32] In explaining its decision, the court expressed concern that declaring such conduct unlawful would give the Commission too much latitude to substitute its own judgment for a respondent's independent business decisions that were taken without any anticompetitive purpose or prospect. In essence, although the challenged conduct was discriminatory and harmful, it did not violate the policies underlying the antitrust laws. The opinion does not discuss Section 5's jurisdictional breadth, and the facts of the case are so unusual that the case has little import for that legal issue.[33]

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[31] *Official Airline Guides*, 630 F.3d at 927 (citing *Cement Inst.*, 333 U.S. at 692-93, and *Atl. Ref.*, 381 U.S. at 367-68).

[32] *U.S. v. Colgate & Co.*, 250 U.S. 300 (1919).

[33] In *In re General Motors*, 99 F.T.C. 464, 580 n.45 (1982), the Commission declared its position that the Second Circuit's decision was incorrect and that "unless it is repudiated by the Supreme Court we hold to our

Boise Cascade involved the use of an industry-wide delivered pricing system. Industry members effected this system by including an artificial freight factor in the price charged to customers. The Commission contended that this practice tended to stabilize prices and therefore violated the Sherman and FTC Acts. The Ninth Circuit disagreed, however, concluding that the use of delivered pricing in this instance was a natural and independent, albeit consciously parallel, response to customer preferences. The court found no need to opine whether consciously parallel conduct, without more, could ever violate Section 5; it declined, however, to hold such behavior illegal *per se* where, as here, persuasive evidence of an anticompetitive effect was lacking. Although the court acknowledged "the unique features of the FTCA,"[34] it held that delivered pricing warranted the same legal assessment under both the FTC and Sherman Acts, since the relevant case law had been well-developed in both court and Commission litigation, as well as through prior Commission statements and practices on the issue. The court concluded that this history had resulted in a requirement that "the Commission must find either collusion or actual effect on competition to make out a § 5 violation for use of delivered pricing."[35] The court was

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interpretation of the case law on arbitrary refusals to deal by monopolists. . . ." Nonetheless, a 2003 Commission letter observed that "the Commission has not issued a decision [since *OAG*] holding that a monopolist violated the FTC Act by using unfair methods of competition that affected customers in an adjacent market in which the monopolist did not operate." Letter from Fed. Trade Comm'n, to the U.S. Dep't of Transp. (Jun. 6, 2003) (on file with FTC Office of General Counsel).

[34] *Boise Cascade*, 637 F.2d at 581.

[35] *Id.* at 582. Much of this history is based on a series of delivered and base-point pricing cases that reached their doctrinal limits in *Cement Institute.* 333 U.S. at 721 n.19 (holding that "[w]hile we hold that the Commission's findings of combination were supported by evidence, that does not mean that the existence of a 'combination' is an indispensable ingredient of an 'unfair method of competition' under the Trade Commission Act."). *See also Triangle Conduit & Cable Co. v. F.T.C.*, 168 F.2d 175 (7th Cir. 1948). Shortly thereafter, the Commission declared that the use of base point pricing could

clear, however, to confine this requirement to situations involving delivered pricing; consequently, it does not materially affect the well-recognized scope of Section 5.

In *Ethyl* – perhaps the most misunderstood and frequently mis-cited case regarding the scope of Section 5 – the Commission challenged four producers of gasoline anti-knock compounds for their use of delivered pricing, most-favored nation clauses, 30-day advance notice to customers of price changes, and announcement of price increases in the press. The producers did not act collusively in adopting and employing these practices; rather, they followed industry tradition and responded to customer demand. The FTC concluded that the practices nonetheless violated Section 5 because they constituted interdependent conduct that substantially reduced competition in the market. The appellate court disagreed, however, because it did not find substantial evidence that the challenged practices led to an adverse competitive impact.[36] Thus, this case, like *Boise Cascade*, was not

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violate Section 5, even when not adopted or implemented as part of a combination or conspiracy. INTERIM REPORT ON STUDY OF FEDERAL TRADE COMMISSION PRICING POLICIES, S. Doc. No. 27, 81st Cong., 1st Sess. 41 (1949) [hereinafter "Interim Report"]. In Congress, however, legislation was introduced to reverse this position, and FTC Commissioners were subjected to "demanding" questioning in Senate Committee hearings. The legislation was abandoned only "after a majority of the commissioners recanted and testified that Section 5 prohibits only conspiracies to adopt base point pricing." Mary Azcuenaga, FTC Comm'r, *Shimmers in the Penumbra of Section 5 and Other News*, Address Before the 13th Annual Antitrust and Trade Regulation Seminar XX (Jul. 9, 1992) at 9-11(on file with FTC Office of General Counsel); S. Doc. No. 27 at 59-63.

[36] *Ethyl*, 729 F.2d at 140-41. The court noted that the FTC's majority opinion observed that non-collusive facilitating practices violate Section 5 only where the evidence demonstrates that they substantially lessen competition and reveal a "clear nexus" between the practices and the competitive harm. The court found such evidence lacking in this case. *Id*.

decided on grounds of statutory interpretation but evidentiary sufficiency.[37]

Despite the outcome, the court engaged in a significant analysis of Section 5 and reconfirmed that it extends to conduct that does not fall within the antitrust laws. In particular, the court noted that "Congress' aim was to protect society against oppressive anticompetitive conduct and thus assure that the conduct prohibited by the Sherman and Clayton Acts would be supplemented as necessary and any interstices filled."[38] Subsequently the court elaborated that:

> [a]lthough the Commission may under § 5 enforce the antitrust laws, including the Sherman and Clayton Acts, it is not confined to their letter. It may bar incipient violations of those statutes, and conduct which, although not a violation of the letter of the antitrust laws, is close to a violation or is contrary to their spirit. In prosecuting violations of the spirit of the antitrust laws, the Commission has, with one or two exceptions, confined itself to attacking collusive, predatory, restrictive or deceitful conduct that substantially lessens competition.[39]

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[37] For a detailed discussion of the Commission analysis in *Ethyl* regarding facilitating practices, *see* Donald S. Clark, *Price-Fixing Without Collusion: An Antitrust Analysis of Facilitating Practices After Ethyl Corp.*, 1983 WISC. L. REV. 887 (1983).

[38] *Ethyl*, 729 F.2d at 136 (quoting Report of the Conference Committee, H.R.Rep. No. 1142, 63d Cong., 2d Sess. 19 (1914)).

[39] *Id.* at 136-37 (citations and footnote omitted). *See also F.T.C. v. Abbott Lab.*, 853 F. Supp. 526 (D.D.C. 1994) (relying on *Ethyl* and *Sperry & Hutchinson*).

Section 5's intentionally unparticularized phrase, "unfair methods of competition" is not, therefore, an all-encompassing, unfocused warrant as some would claim. Rather, it is a flexible and powerful Congressional mandate to protect competition from unreasonable restraints, whether long-since recognized or newly discovered, that violate the antitrust laws, constitute incipient violations of those laws, or contravene those laws' fundamental policies.[40]

III. LIMITING ATTRIBUTES OF SECTION 5

Congress had good reasons for leaving Section 5's metes and bounds unspecified. Any effort in the name of "guidance" to provide a detailed plat defining its coverage would undermine Congress's clear intent to create a statute with sufficient scope,

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[40] This same period, 1980-1984, also yielded significant FTC efforts to rein in the use of Section 5. The most important of these is *In re General Foods Co.*, 103 F.T.C. 204, 364-66 (1984). In this case the Commission rejected application of Section 5 to an alleged attempt to monopolize where the evidence did not reveal a dangerous probability of success, an element that had long been required under Section 2 of the Sherman Act. In the Commission's view, the concept of an incipient attempt to monopolize was simply beyond parsing. Moreover:

> [w]hile Section 5 may empower the Commission to pursue those activities which offend the "basic policies" of the antitrust laws, we do not believe that power should be used to reshape those policies when they have been clearly expressed and circumscribed.

Id. at 352. The Commission expressly limited its holding in this regard to the dangerous probability issue and declined to comment whether Section 5 required the same measure of intent as did Section 2 of the Sherman Act. Other significant Commission actions from this period that bear on Section 5 jurisdiction regarding competition policy enforcement include: *In re Kellogg Co.*, 99 F.T.C. 8 (1982) (summarily dismissing the appeal of an initial decision rejecting allegations that non-collusive efforts to maintain shared monopoly control of the ready-to-eat cereal market violated Section 5); and *In re Exxon Co.*, 98 F.T.C. 453 (1981) (terminating an investigation into shared monopoly in the petroleum industry).

elasticity, and adaptability to accomplish its purpose. Thus, the influential treatise, Antitrust Law, observes, that:

> [i]t is now commonly said that Federal Trade Commission § 5 is not confined by the prohibitions of the Sherman Act or the Clayton Act. Indeed, § 5 is not confined by antitrust concepts at all. It allows the Commission to condemn conduct that is "unfair" in senses "beyond simply those enshrined in the letter or encompassed in the spirit of the antitrust laws." Or as the Supreme Court more recently put it, the "standard of 'unfairness' under the FTC Act is, by necessity, an elusive one, encompassing not only practices that violate the Sherman Act and the other antitrust laws but also practices that the Commission determines are against public policy for other reasons."
>
> We have no general quarrel with these holdings; our own concern is limited to § 5 holdings that follow "the letter or ... spirit" of the antitrust laws.[41]

My concerns here are also confined to matters implicating "the letter or spirit" of the antitrust laws. Section 5's "standard of unfairness" in this regard may yet strike some as "elusive," but it is far from unknowable or unbounded. Congress's mandate is that Section 5 should supplement and bolster the antitrust laws by challenging conduct that not only violates the antitrust laws but that also falls within the "penumbra"[42] of those statutes. Two

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[41] PHILLIP AREEDA, HERBERT HOVENKAMP & ROGER BLAIR, II ANTITRUST LAW ¶ 302h, p.21 (2d ed.) (Aspen Law and Business, 2000) (footnotes omitted).

[42] *Sperry & Hutchinson*, 405 U.S. at 244 n.5 (quoting Unfair or Deceptive Advertising and Labeling of Cigarettes in Relation to the Health Hazards of Smoking, 29 Fed. Reg. 8324, 8355 (Jul. 2, 1964) (codified at 15

critical attributes of Section 5 – the limited consequences of a Section 5 violation, and the inherent relationship between Section 5's reach and the scope of the antitrust laws – help ensure that respondents find enforcement efforts under this mandate to be neither punitive nor overreaching.

A. The Consequences of a Section 5 Violation Are More Limited than Those Resulting from a Violation of the Antitrust Laws

Section 5 violations involving conduct outside the antitrust statutes entail far more limited consequences than do violations of the Sherman or Clayton Acts. The FTC nearly always brings such cases as administrative litigation, and violations generally result only in cease-and-desist orders designed to prevent future violations and, on occasion, injunctive measures to help preserve or restore conditions for vigorous competition in the market.[43] In addition, although the Commission may seek disgorgement or restitution in competition matters, it must do so from a court. Moreover, the Agency's policy is to request equitable monetary relief in such matters only where the violation is relatively clear.[44]

C.F.R. pt. 408)). *See also Chuck's Feed & Seed Co., Inc. v. Ralston Purina Co.*, 810 F.2d 1289, 1292-93 (4th Cir. 1987); Mary Azcuenaga, FTC Comm'r, *FTC Enforcement: An Idiosyncratic Journey*, Address Before the 15th Annual Antitrust and Trade Regulation Seminar 5 (Jul. 7, 1994) (on file with FTC Office of General Counsel); Mary Azcuenaga, *Shimmers in the Penumbra of Section 5 and Other News*, *supra* note 35; William E. Kovacic, *The Federal Trade Commission and Congressional Oversight of Antitrust Enforcement*, 17 TULSA L.J. 587, 625-627 (1982).

[43] *But see e.g., In re Xerox*, 86 F.T.C. 364 (1975) (consent order compelling limited royalty free licensing of patents for dry paper copier technology).

[44] FED. TRADE COMM'N, POLICY STATEMENT ON MONETARY EQUITABLE REMEDIES IN COMPETITION CASES (2003), *available at* http://www.ftc.gov/ow/2003/07/disgorgementfrn.htm. *See also F.T.C. v. Mylan Lab., Inc.*, 62 F. Supp. 2d 25, 36-37 (D.D.C. 1999) (mem.), *aff'd in pertinent part*, 99 F. Supp. 2d 1, 4-5 (D.D.C. 1999).

The FTC Act contains no provisions for private enforcement. A Commission action brought under Section 5 has little value in subsequent "follow-on" treble-damage litigation,[45] and proof of Section 5 violations, standing alone, provide no basis for seeking criminal penalties under the Sherman Act or comparable state provisions.

Because of these relatively mild consequences, Section 5 can fairly extend more broadly than the antitrust laws. This characteristic makes Section 5 especially well designed to apply in circumstances where exposing the respondent to treble damage jeopardy might be unfair or inappropriate, even though the conduct itself may warrant prohibition. Such circumstances might arise in situations involving unseasoned legal or economic theories, innovative business strategies, new or complex markets, or a substantially altered regulatory context.

The FTC Act also provides a right of review in the courts of appeals. Respondents are protected from both unfairness and surprise, especially because the review becomes increasingly searching as the violation becomes more novel. As the Second Circuit declared:

> As the Commission moves away from attacking conduct that is either a violation of the antitrust laws or collusive, coercive, predatory, restrictive or deceitful, and seeks to break new ground by enjoining otherwise legitimate practices, the closer must be our scrutiny upon judicial review.[46]

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[45] *See* 15 U.S.C. § 16(a) (1984). "[I]n any action or proceeding brought under the antitrust laws, collateral estoppel effect shall not be given to any finding made by the Federal Trade Commission under the antitrust laws or under section 45 [*i.e.*, Section 5]." *See also Pool Water Prods. v. Olin Corp.*, 258 F.3d 1024, 1030 (9th Cir. 2001).

[46] *Ethyl*, 729 F.2d at 137.

Although courts sometimes have overturned Commission determinations or remedies – typically on grounds that the evidence does not establish the offense or the order is broader than necessary – appellate courts have almost always reaffirmed the breadth of the FTC's Section 5 jurisdiction.[47]

Finally, the Agency does not enforce Section 5 in a vacuum. Congress also plays an active role, especially in oversight regarding the Commission's authority and statutory interpretations. FTC officials frequently appear before Congressional committees or meet with Congressional staff to describe or defend its policies or practices. Put differently, there are no secrets as to what the Commission is doing or what Congress wants us to do; insufficient, excessive, or misdirected zeal commonly invites scrutiny and correction.[48]

For example, Congressional reaction to the *Cement Institute* and *Triangle Conduit* decisions, as well as to the Commission's declaration that base point pricing could violate Section 5 even when not part of a conspiracy, induced a majority of the commissioners to reverse their position on this issue.[49] It was also Congressional uncertainty regarding the scope of the Commission's Section 5 authority to challenge "unfair acts or practices" that led the Commission to issue a "consumer unfairness statement" in 1980.[50] Then, in 1994, Congress went

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[47] *See, e.g., id*. at 136-137.

[48] *See* Kovacic, 17 TULSA L.J. 587 (1982).

[49] *See Boise Cascade*, 637 F.2d at 582; *see also Cement Inst.*, 333 U.S. at 721 n.19; Kovacic, 17 TULSA L.J. at 625-27. *See generally Triangle Conduit*, 168 F.2d at 176; Interim Report, S. Doc. No. 27; Azcuenaga, *Shimmers in the Penumbra of Section 5 and Other News*, *supra* note 35, at 9-11.

[50] Commission Statement of Policy on the Scope of the Consumer Unfairness Jurisdiction, *included in* Letter from Chairman Pertschuk and

further and codified this statement, in substance, as Section 5(n) of the FTC Act.[51]

Agency officials have regularly incorporated the lessons of appellate and Congressional review into FTC practice, as they should. The Commission has long since put to rest the issues at the center of its most controversial Section 5 matters. It has not, for example, held unlawful the unilateral adoption or use of delivered or base point pricing since the Second Circuit issued its opinion in *Ethyl* 22 years ago. Nor, since that time, has the FTC condemned consciously parallel pricing in the absence of evidence of "oppressiveness" or some "plus factor" suggesting overt or tacit collusion. The Commission also terminated its two controversial shared monopoly matters.[52] This history gives me confidence that the FTC will be equally responsive in the future, even if we employ Section 5 more expansively, as we should.

B. Section 5's Scope Is Hinged to That of the Antitrust Laws

As noted previously, when using Section 5 to enforce competition policy, the Commission and courts have largely

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Commissioners Dixon, Clanton, Pitofsky and Bailey to the Honorable Wendell H. Ford and the Honorable John C. Danforth (Dec. 1, 1980) (available as appendix to *Int'l Harvester Co.*, 104 F.T.C. 949, 1071 (1984)). This statement was based, in significant part, on Unfair or Deceptive Advertising and Labeling of Cigarettes in Relation to the Health Hazards of Smoking, 29 Fed. Reg. 8324, 8355 (Jul. 2, 1964) (codified at 15 C.F.R. pt. 408), as quoted in *Sperry & Hutchinson*, 405 U.S. at 244 n.5. The Commission issued a companion policy statement regarding "deception" in 1983. Policy Statement on Deception, contained in Commission letter on deception to the Honorable John D. Dingell, Chairman, Subcommittee on Oversight and Investigations, Committee on Energy & Commerce, Oct. 14, 1983, appended to *In re Cliffdale Assoc's.*, 103 F.T.C. 110, 174 (1984).

[51] 15 U.S.C. § 45(n) (2006).

[52] *In re Kellogg Co.*, 99 F.T.C. at 269 (summarily dismissing further appeal); *In re Exxon Co.*, 98 F.T.C. at 461 (dismissing the complaint without prejudice).

confined Section 5's reach beyond the antitrust laws to incipient violations of those laws, and violations of those laws' underlying purposes. Because each of these categories finds its touchstone in the antitrust laws themselves, the application of Section 5 is necessarily hinged to the goals, interpretations, and analysis of conduct pursuant to those laws. These sources influence both the content and constraints for "unfair methods of competition," just as they provide both sense and substance for the Sherman Act's equally non-specific phrase, "restraint of trade."

The economic principles and analysis that guide application of the antitrust laws also guides competition policy enforcement under Section 5, notwithstanding the statutory differences. As the antitrust laws expand, shift, or contract, so too does Section 5 adjust and adapt. For example, antitrust analysis has lessened its concern with firm size and market concentration in recent decades and focused more on consumer welfare, innovation, and efficiency. Section 5 jurisprudence has traveled the same path, sometimes leading and sometimes learning. In my view, despite the important differences in breadth and effects, competition policy enforcement under Section 5 appears on balance to be as wise and well-reasoned – no more and no less – as under the antitrust laws.

Section 5's connection with the antitrust laws has led the Agency to rely on antitrust jurisprudence – the cases, principles, and associated economic analysis – as its most significant source of guidance. The Supreme Court articulated the nature of this reliance more than 40 years ago in *Atlantic Refining Company*, when it observed that:

> [i]t has long been recognized that there are many unfair methods of competition that do not assume the proportions of antitrust violations. *Federal Trade Comm'n v. Motion Picture Advertising Service Co.*, 344 U.S. 392, 394 (1953). When conduct does bear the [central competitive]

> characteristics of recognized antitrust violations it becomes suspect, and the Commission may properly look to cases applying those laws for guidance.[53]

Or, as the Fourth Circuit expressed more recently:

> In the area of anticompetitive practices, the FTC Act functions as a kind of penumbra around the federal antitrust statutes. An anticompetitive practice need not violate the Sherman Act or the Clayton Act in order to violate the FTC Act. However, the scope of the FTC is nonetheless linked to the antitrust laws. . . . The federal [sic] Trade Commission itself looks to antitrust principles in deciding whether § 5 of the FTC Act has been violated.[54]

Section 5 does not replicate the antitrust laws; the relationship between the provisions is better described as complementary rather than as congruent. In many instances, Section's 5's unique coupling of broad scope with modest consequences may prove to be the most apt enforcement tool. The critical connection between Section 5 and antitrust law and analysis, however, helps ensure that Section 5 remains in harmony with the laws it was designed to bolster and support.

IV. THE ELEMENTS OF A SECTION 5 VIOLATION

If we are to use Section 5 to enforce competition policy in a manner consistent with the intent of its framers, I suggest that there should be two requisite elements for a violation. The first is

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[53] *Atl. Ref.*, 381 U.S. at 369-70.

[54] *Chuck's Feed*, 810 F.2d at 1292-93 (citations omitted).

that the respondent must have engaged in identifiable, culpable conduct. The second is evidence of actual or incipient injury to competition.

Conduct. The conduct aspect of this test ensures that the respondent recognizes – or should have recognized – in advance that its conduct was inappropriate. This requirement is met where the respondent engages in actions that are "collusive, coercive, predatory, restrictive, or deceitful,"[55] or otherwise oppressive, and does so without a justification grounded in its legitimate, independent self-interest.[56] Unlike Section 2 of the Sherman Act, which requires proof of specific intent to prove the offense of attempted monopolization,[57] stand-alone applications of Section 5 do not require that element to establish an unfair method of competition. Nonetheless, firms are almost always aware of, and intend, the anticompetitive implications of the types of conduct that would be sufficient for a Section 5 violation. Significantly, although "unfair methods of competition" is not limited to the categories of conduct noted above, Rambus's conduct in this matter could easily have been characterized as falling within several of them.[58]

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[55] *Ethyl*, 729 F.2d at 137.

[56] *See generally Boise Cascade*, 637 F.2d at 573 (finding independent, legitimate reasons for *Boise Cascade's* use of a delivered pricing system).

[57] In contrast, Section 2 does not require a showing of specific intent to prove unlawful monopolization; for this offense, proof of general intent to engage in the challenged anticompetitive conduct will suffice. *U.S. v. Grinnell Corp.*, 384 U.S. 563, 570-71 (1966); *Berkey Photo, Inc. v. Eastman Kodak Co.*, 603 F.3d 263 274 (2d Cir. 1979).

[58] Significant information regarding the Commission's prosecutorial policies is available not only through the Commission's cases, but also its consent agreements and the testimony, speeches, and public communications of FTC officials.

Injury. Section 5 does not require proof of an actual injury to competition. Rather, established precedent holds that:

> a showing of an actual anticompetitive effect is unnecessary to prove a violation of Section 5 because that section was designed to stop [in] their incipiency acts and practices that could lead to violations of the Sherman or Clayton Acts.[59]

For conduct within the penumbra of the antitrust laws, it is sufficient if the competitive injury is only suspected or embryonic. While conduct violating Section 5 must bear a realistic potential for causing competitive harm, more manifest injury should not be required.

Other Section 5 standards. Other formulations of Section 5's requirements are worded differently, yet they are strikingly similar in substance. For example, the Second Circuit stated in *Ethyl* that:

> [i]n our view, before business conduct in an oligopolistic industry may be labeled "unfair" within the meaning of § 5 a minimum standard demands that, absent a tacit agreement, at least some indicia of oppressiveness must exist such as (1) evidence of anticompetitive intent or purpose on the part of the producer charged, or (2) the absence of an independent legitimate business reason for its conduct. If, for instance, a seller's conduct, even absent identical behavior on the part

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[59] *In re Coca Cola Co.*, 117 F.T.C. 795, 970 n.25 (1994) (citing *Sperry & Hutchinson*, 405 U.S. at 244, and *In re Dean Foods Co.*, 70 F.T.C. 1146, 1289-90). The FTC also expressly "disagree[d] with respondent's legal premise" that it must demonstrate "an anticompetitive purpose or effect to find a violation of Section 5 where there is no violation of the Clayton or Sherman Acts." *Id.* at 915.

> of its competitors, is contrary to its independent self-interest, that circumstance would indicate that the business practice is "unfair" within the meaning of § 5. In short, in the absence of proof of a violation of the antitrust laws or evidence of collusive, coercive, predatory, or exclusionary conduct, business practices are not "unfair" in violation of § 5 unless those practices either have an anticompetitive purpose or cannot be supported by an independent legitimate reason.[60]

In essence, the Second Circuit held that a Section 5 cause of action may be predicated on: (a) evidence of tacit agreement, or collusive, coercive, predatory, or exclusionary conduct;[61] *or* (b) evidence of an anticompetitive intent or purpose; *or* (c) lack of an independent, legitimate reason for the conduct. Any of these characteristics will suffice as a predicate. Although *Ethyl* does not expressly require actual or incipient injury to competition, each of the three indicia mentioned above raises the prospect that the challenged conduct will harm competition.

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[60] *Ethyl*, 729 F.2d at 139-40. *See also Abbott Lab.*, 853 F. Supp. at 536 (quoting, with apparent approval, the footnoted passage from *Ethyl*). The holding in *Boise Cascade*, 637 F.2d at 577, is not inconsistent with the quoted view. *Boise Cascade*'s holding that the FTC must demonstrate that the parallel pricing system helped to fix or rigidify market prices if proof of overt collusion is lacking merely reflects the court's view that a Section 5 challenge to non-collusive parallel pricing requires evidence suggesting that the conduct injured competition.

[61] "Restrictive" and "deceitful" conduct probably also belong in this listing as well, since the court included them when noting the categories of conduct ("collusive, predatory, restrictive, and deceitful") to which the Commission has usually confined its Section 5 efforts, and the types of conduct ("collusive, coercive, predatory, restrictive, or deceitful") beyond which, efforts to apply Section 5 tend to be more novel and therefore to warrant more searching scrutiny on appellate review. *Ethyl*, 729 F.2d at 136-137.

Elaborating in a footnote, the court observed that "[t]he requirement [of oppressiveness] is comparable to the principle that there must be a 'plus factor' before conscious parallelism may be found to be conspiratorial in violation of the Sherman Act."[62] As examples, the court suggested that this "plus factor" requirement could be satisfied by conduct that "is contrary to the defendants' independent self-interest," that reflects a "strong motive on a defendant['s] part to enter an alleged conspiracy," or that may result in the "artificial standardization of products."[63]

The appellate court in *Ethyl* was discussing conduct in oligopolistic markets. Nonetheless, factors such as the ones mentioned – the list is not exhaustive – can help flag "unfairness" in other situations as well. Conduct contrary to a firm's legitimate, independent self-interest has frequently been a hallmark of predatory or exclusionary conduct by a dominant firm.[64] The presence of "oppressiveness" or an "anticompetitive intent or purpose," may help distinguish anticompetitive from vigorously competitive conduct.[65] Conduct that leads to the artificial standardization of products – often due to misuse of the

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[62] *Id.* at 140 n.10.

[63] *Id.* (citations omitted).

[64] *Brooke Grp. Ltd. v. Brown & Williamson Tobacco Corp.*, 509 U.S. 209 (1993) (observing that predatory pricing is unlikely, because it is contrary to a firm's *independent* self interest except when it has the ability to recoup its investment in the strategy); James Hurwitz & William E. Kovacic, *Judicial Standards of Predation: The Emerging Trends*, 35 VAND. L.REV. 63 (1982) (examining theories of predatory pricing and circumstances when pricing below various measures of cost will be contrary to a firm's legitimate self-interest and thus warrant legal condemnation).

[65] In *Official Airlines Guide*, the court was swayed by the appellant's apparent lack of an anticompetitive motive or purpose for its refusal to deal, since OAG did not compete in the market where its conduct had its anticompetitive impact.

standard-setting process – may serve to deter entry, exploit rivals, secure market power, or preserve dominance.[66]

The Areeda treatise offers a comparable formulation. It recommends that:

> [t]he Commission should feel free to "enjoin" any unjustified behavior that tends to impair competition and is capable of being differentiated adequately from permissible behavior.[67]

I agree.

In sum, where there is no identifiable, culpable conduct, there is no violation. "Culpable" in this respect does not require specific intent or actual antitrust injury. It must, however, display sufficient anticompetitive attributes – *e.g.*, oppressiveness, lack of

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[66] *See, e.g., Allied Tube*, 486 U.S. at 500-01. In the present case, Rambus's deceptive conduct *artificially* misdirected JEDEC's standard to one that fell within the respondent's secretly expanded patent claims, contrary to the organization's clear goals to avoid standards that would subject members to substantial royalty payments. The FTC has also challenged misdirection of standard-setting efforts in *In re Union Oil Co. of Cal.*, 2005 WL 2003365 (2005) (consent resolving both Unocal's proposed merger with Chevron and a separate administrative case alleging that Unocal misrepresented to the California Air Resources Board that Unocal's research regarding low-emissions gasoline was non-proprietary) and *In re Dell Computer Corp.*, 121 F.T.C. 616 (1996) (consent regarding FTC's allegation that Dell Computer failed to disclose its patent rights to the Video Electronics Standards Association despite the group's "affirmative disclosure requirements.").

[67] AREEDA, HOVENKAMP, & BLAIR, *supra* note 41, at ¶ 302h3. The treatise offers this statement in criticizing the concepts of "incipient violations" and "policy violations" of the antitrust laws, as they are presented in *Brown Shoe*, 384 U.S. 316, which expressly does not require proof of anticompetitive effects. Although I find these categories useful and well supported in Section 5's history, I agree that the use of Section 5 to enforce competition policy should require at least the tendency to impair competition.

an independent business justification, anticompetitive intent, predation, collusion, deceit, a tendency to impair competition – to warrant characterizing it as unfair, and be at least potentially injurious. Where such qualities are present, it is neither inappropriate nor unwise to find Section 5 liability.[68]

V. RAMBUS'S CONDUCT

Such anticompetitive attributes are clearly present here and, sadly, in abundance. Indeed, Rambus's attempts to deceptively subvert JEDEC's laudable standard-setting efforts is precisely the type of behavior that Congress envisioned would fall within Section 5's mandate.

In considering the application of a "stand-alone" Section 5 cause of action to this behavior, it is not necessary to restate the Commission's findings regarding Rambus's deception since these have been detailed elsewhere in the Commission Opinion. Nonetheless, a brief review of some of the most salient facts demonstrates that finding liability under a "stand-alone" Section 5 cause of action would have been fully appropriate in this matter.

Rambus's conduct occurred in the context of a standard-setting effort involving rivals. In most situations involving direct competitors, one might expect, and even encourage, bare-knuckled competition, including strategies based on secrecy,

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[68] The Commission, on occasion, has used Section 5 in recent years to address conduct beyond the scope of the antitrust laws, usually in the context of invitations to collude. *See e.g., In re Valassis Communications, Inc.* (FTC File No. 051 008) (Mar. 16, 2006), *available at* http://www.ftc.gov/os/caselist/051008/051008.htm. In my view, of course, Section 5 offers far greater potential and should be used more fully. While this concurrence discusses the limiting attributes of Section 5 and the predicates of a violation, it does not attempt to prescribe future generic or specific applications of the statute. That, hopefully, will be done by the Commission in future cases.

misinformation, and misdirection.[69] But standard-setting is not a typical "everyone for himself" competitive situation. It is one in which collaboration can yield a valuable result – in this case, the establishment of a useful foundation for future, competitive and innovative efforts. But it is also a setting in which a participant's deceptive strategies can usurp the group's efforts – and industry-wide force supporting them – to serve its own anticompetitive ends. Participants must play by the rules if the joint goal is to be achieved. If competition policy permits easy subversion of these joint efforts, however, then there is little justification in the first place for risking the collaboration among rivals that effective standard-setting often requires. From a competition policy perspective, standard-setting efforts such as JEDEC's are "high risk/high gain" activities. They can be particularly valuable, on balance, if procedures ensuring fairness are adopted and followed in good faith.[70]

In this instance, Rambus violated any reasonable conception of good faith and fairness, and the proximate, competitive impact of its conduct is clear. Rambus misled the standard-setting body with regard to its own intellectual property interests, while simultaneously participating in JEDEC to learn about the organization's developing standards. Based on this wolf-in-sheep's-clothing pose, Rambus was in a position to, and did, amend its own patent claims in order to secretly convert what was intended to be an openly available industry-standard into a private source of revenues.

For example, early during its participation in JEDEC, Rambus's JEDEC representative, Richard Crisp, learned what technologies were being considered for the SDRAM standard. Crisp related that knowledge to Rambus's patent counsel, and

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[69] *Berkey Photo*, 603 F.2d at 281 (2d Cir. 1979).

[70] *Allied Tube*, 486 U.S. at 500-01.

together they considered how to amend Rambus's patent claims so that they would cover the emerging JEDEC standard. Rambus even assigned an engineer to provide technical assistance and ensure the amendments would do their job. Rambus continued to use the knowledge gained at JEDEC to amend its patents in this manner. As noted in a December 1992 Rambus planning document, Rambus sought to "get a copy of the SDRAM spec and check it for features we need to cover as well as features which violate our patents."[71] Crisp's September 1995 statement to Rambus management further sums up Rambus's strategy. He urged that Rambus:

> should redouble our efforts to get the necessary amendments completed, the new claims added and make damn sure this ship is watertight before we get too far out to sea.[72]

Rambus's patent strategy relating to the JEDEC standard clearly had the imprimatur of its management. This strategy was known to senior executives at the company in 1992, implemented by an executive vice president, and approved by its CEO Geoff Tate.[73] Finally, Rambus's 1996 withdrawal letter further misled JEDEC members by omitting the only issued patent that Rambus believed covered JEDEC's DRAM standards, and including a patent that Rambus knew (or should have known) was entirely irrelevant.[74]

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[71] *See supra*, Commission Opinion, at 36-39.

[72] CX 837 at 2.

[73] *See supra*, Commission Opinion, at 37-42.

[74] CX 887 (withdrawal letter); CX 5013 at 2 (Rambus memorandum noting that the '327 patent covered dual edged clocking).

Rambus did not merely take advantage of the knowledge it gained at JEDEC to ensure it would cover the relevant DRAM standards in its own patent applications; it also did so in direct contravention of JEDEC's broadly-acknowledged purpose: to create consensus-based standards that reflect the interests of all of its members.[75] JEDEC participants' testimony at trial consistently emphasized the wish of JEDEC members to either avoid patented technologies or to secure protections against the unrestricted exercise of patent rights.[76] Even Richard Crisp understood that "[t]he job of JEDEC is to create standards which steer clear of patents which must be used to be in compliance with the standard whenever possible."[77]

While the Commission does not object to covert maneuvers and non-disclosure in typical head-to-head market competition, Rambus's end run around the standard-setting process goes too far. It undermines the policies of the antitrust laws that seek to promote useful innovation and permit joint efforts by rivals that may enhance competition and efficiency. As such, Rambus's conduct would be an unfair method of competition in violation of Section 5 of the Federal Trade Commission Act.

Indeed, Rambus's behavior epitomizes what Senator Robinson in 1914 viewed to be the essence of unfair competition, namely "oppression or advantage obtained by deception or some questionable means. . . .".[78] Or, turning to more modern expressions, Rambus's behavior contravenes "public values beyond simply those enshrined in the letter or encompassed in the

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[75] *See, e.g.*, Becker, Tr. 1152; J. Kelly, Tr. 1784-85; CX 2767 at 1.

[76] *See, e.g.*, Sussman, Tr. 1333; Landgraf, Tr. 1693-94; G. Kelley, Tr. 2393-96; Lee, Tr. 6598.

[77] CX 903; Crisp, Tr. 2941-42.

[78] 51 CONG. REC. 12,248 (1914) (statement of Sen. Robinson).

spirit of the antitrust laws."[79] It likewise runs afoul of the Second Circuit's statement in *Ethyl* that the Commission's role under Section 5 is to "protect society against oppressive anticompetitive conduct."[80] Indeed, that court expressly noted that one attribute of "oppressiveness" could be the "artificial standardization of products."[81] It is fair to say that, through its deceptive and exploitative conduct, Rambus effectively co-opted JEDEC's standard-setting process and rendered the JEDEC outcome "artificial."

VI. CONCLUSION

Rambus's abuse of JEDEC's standard-setting process was intentional, inappropriate, and injurious to competition and consumers alike. The Commission Opinion finds that these deceptive practices violate Section 2. Even if this conduct did not violate the Sherman Act, it would have fallen within Section 5's broader province had this claim been argued at trial.

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[79] *Sperry & Hutchinson*, 405 U.S. at 244.

[80] *Ethyl*, 729 F.2d at 136.

[81] *Id.* at 139 n.10.

As for our future enforcement efforts, the framers of the FTC Act gave the Agency a mandate – one unique to the Commission – to use Section 5 to supplement and bolster the antitrust laws by providing, in essence, a jurisdictional "penumbra" around them. The framers also gave the FTC deliberative processes for examining suspected incipient or policy violations of the antitrust laws, and provided remedial measures dedicated more to protecting and restoring competition than to punishing malfeasors. Although the Agency has not ignored its Congressional mandate entirely, we need to build on this foundation and further develop this aspect of our enforcement responsibility – and to use all the arrows in our jurisdictional quiver to ensure that competition is robust, innovative, and beneficial to consumers.

ORDER REVERSING AND VACATING INITIAL DECISION AND ACCOMPANYING ORDER, SCHEDULING SUPPLEMENTAL BRIEFING ON ISSUES OF REMEDY, AND DENYING COMPLAINT COUNSEL'S MOTION FOR SANCTIONS

This matter having been heard by the Commission upon the appeal of Counsel Supporting the Complaint and the cross-appeal of Respondent, and upon the respective briefs and oral arguments in support of such positions, and the Commission having determined that Respondent has violated Section 5 of the Federal Trade Commission Act – for the reasons stated in the accompanying Opinion – the Commission has therefore determined to reverse and vacate the Initial Decision, to vacate the Order accompanying the Initial Decision, and to direct supplemental briefing on issues of remedy. The Commission has also determined to deny Complaint Counsel's Motion for

Sanctions Due to Rambus's Spoliation of Documents (Aug. 10, 2005) ("Motion for Sanctions").

Accordingly,

IT IS ORDERED THAT the Initial Decision dismissing the Complaint in this proceeding be, and it hereby is, **REVERSED** and **VACATED**;

IT IS FURTHER ORDERED THAT all findings and conclusions in the Initial Decision, other than those expressly cited and relied upon in the Opinion accompanying this Order, be, and they hereby are, **SET ASIDE**;

IT IS FURTHER ORDERED THAT the Order accompanying the Initial Decision and dismissing the Complaint in this proceeding be, and it hereby is, **VACATED**;

IT IS FURTHER ORDERED THAT:

1. On or before September 15, 2006, Rambus and Complaint Counsel each shall file a brief, not to exceed 7,500 words – as measured pursuant to Commission Rule 3.52(b)(2) – addressing appropriate issues relating to remedy in this proceeding;[1] and

[1] These briefs shall discuss, without limitation: (1) means for the Commission to determine, based on the existing record, reasonable royalty rates for licensing all technologies applicable to JEDEC-compliant products and covered by relevant Rambus patents; (2) alternative mechanisms and procedures for determining reasonable royalty rates, such as an independent arbitrator, a special master, or an administrative law judge; (3) qualitative characteristics descriptive of appropriate relief, against which specific royalty proposals might be evaluated; and (4) appropriate injunctive and other provisions that should be incorporated in the Final Order in this proceeding.

2. On or before September 29, 2006, each party may file a responding brief, not to exceed 5,000 words, as measured pursuant to Commission Rule 3.52(b)(2);

IT IS FURTHER ORDERED THAT additional oral argument relating to remedy will be scheduled by further order of the Commission after the receipt of the briefs directed by this Order; and

IT IS FURTHER ORDERED THAT the Motion for Sanctions be, and it hereby is, **DENIED.**

By the Commission.

Complaint

IN THE MATTER OF

HOLOGIC, INC.

CONSENT ORDER, ETC., IN REGARD TO ALLEGED VIOLATIONS OF SEC. 7 OF THE CLAYTON ACT AND SEC. 5 OF THE FEDERAL TRADE COMMISSION ACT

Docket C-4165; File No. 051 0263
Complaint, August 9, 2006 – Decision, August 9, 2006

This consent order addresses the acquisition by respondent Hologic, Inc., of the intellectual property and other assets of Fischer Imaging Corporation relating to its mammography and breast biopsy businesses. As a result of the acquisition, Hologic would lose its only significant competitor in the U.S. market for prone stereotactic breast biopsy systems ("prone SBBS"). The order requires Hologic to divest to Siemens AG, or another Commission-approved acquirer, all assets it acquired from Fischer relating to Fischer's prone SBBS business, ensuring the prompt competitive viability of Siemens or another acquirer as an additional supplier of prone SBBSs in the United States. Hologic will retain a license to Fischer's prone SBBS patents to ensure that Hologic can continue to compete in the U.S. market after the divestiture. If Hologic fails to divest within the time frames given, the Commission may appoint a trustee to divest the prone SBBS assets.

Participants

For the *Commission*: *Stephanie C. Bovee, Richard H. Cunningham, Tammy L. Imhoff, Randall A. Long,* and *Jeffrey H. Perry.*

For the *Respondent*: *Robert C. Jones* and *Phillip A. Proger, Jones Day.*

COMPLAINT

Pursuant to the provisions of the Federal Trade Commission Act and the Clayton Act, and by virtue of the authority vested in it by said Acts, the Federal Trade Commission (hereinafter "Commission"), having reason to believe that Respondent